LM1881 Video Sync Separator

Check for Samples: LM1881

FEATURES

- **AC Coupled Composite Input Signal**
- **>10 kΩ Input Resistance**
- **<10 mA Power Supply Drain Current**
- **Composite Sync and Vertical Outputs**
- **Odd/Even Field Output**
- **Burst Gate/Back Porch Output**
- **Horizontal Scan Rates to 150 kHz**
- **Edge Triggered Vertical Output**
- **Default Triggered Vertical Output for Non-standard Video Signal (Video Games-Home Computers)**

DESCRIPTION

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL (1) and SECAM video signals with amplitude from 0.5V to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case for a non-standard video signal.

(1) PAL in this datasheet refers to European broadcast TV standard “Phase Alternating Line”, and not to Programmable Array Logic.

Connection Diagram

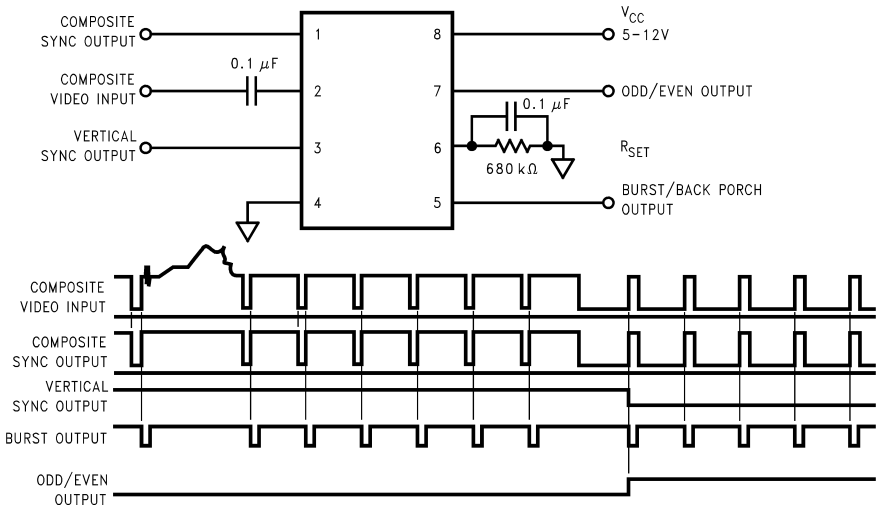

Figure 1. LM1881N
See Package Number D0008A or P0008E

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Absolute Maximum Ratings (1)(2)

Supply Voltage			13.2V
Input Voltage			3 V_{P-P} (V_{CC} = 5V) 6 V_{P-P} (V_{CC} ≥ 8V)
Output Sink Currents; Pins, 1, 3, 5			5 mA
Output Sink Current; Pin 7			2 mA
Package Dissipation (3)			1100 mW
Storage Temperature Range			−65°C to +150°C
ESD Susceptibility (4)			2 kV
ESD Susceptibility (5)			200 V
Soldering Information	PDIP Package (10 sec.)		260°C
	SOIC Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110°C/W, junction to ambient.
(4) ESD susceptibility test uses the “human body model, 100 pF discharged through a 1.5 kΩ resistor”.
(5) Machine Model, 220 pF – 240 pF discharged through all pins.

Electrical Characteristics LM1881

V_{CC} = 5V; R_{SET} = 680 kΩ; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A=25°C

Parameter	Conditions		Min	Typ (1)	Max	Units
Supply Current	Outputs at Logic 1	V_{CC} = 5V V_{CC} = 12V		5.2 5.5	10 12	mA
DC Input Voltage	Pin 2		1.3	1.5	1.8	V
Input Threshold Voltage	(2)		55	70	85	mV
Input Discharge Current	Pin 2; V_{IN} = 2V		6	11	16	µA
Input Clamp Charge Current	Pin 2; V_{IN} = 1V		0.2	0.8		mA
R_{SET} Pin Reference Voltage	Pin 6; (3)		1.10	1.22	1.35	V
Composite Sync. & Vertical Outputs	I_{OUT} = 40 µA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.0 11.0	4.5		V
	I_{OUT} = 1.6 mA Logic 1	V_{CC} = 5V V_{CC} = 12V	2.4 10.0	3.6		V
Burst Gate & Odd/Even Outputs	I_{OUT} = 40 µA; Logic 1	V_{CC} = 5V V_{CC} = 12V	4.0 11.0	4.5		V
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1			0.2	0.8	V
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3			0.2	0.8	V
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5			0.2	0.8	V
Odd/Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7			0.2	0.8	V
Vertical Sync Width			190	230	300	µs
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}		2.5	4	4.7	µs
Vertical Default Time	(4)		32	65	90	µs

(1) Typicals are at T_J = 25°C and represent the most likely parametric norm.
(2) Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.
(3) Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5 and 7) to the R_{SET} pin (Pin 6).
(4) Delay time between the start of vertical sync (at input) and the vertical output pulse.

Typical Performance Characteristics

R_{SET} Value Selection vs Vertical Serration Pulse Separation

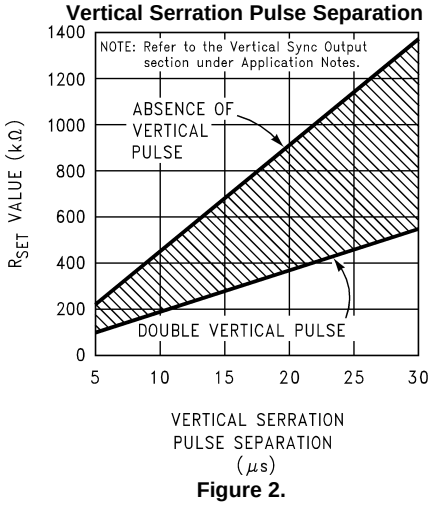


Figure 2.

Vertical Default Sync Delay Time vs R_{SET}

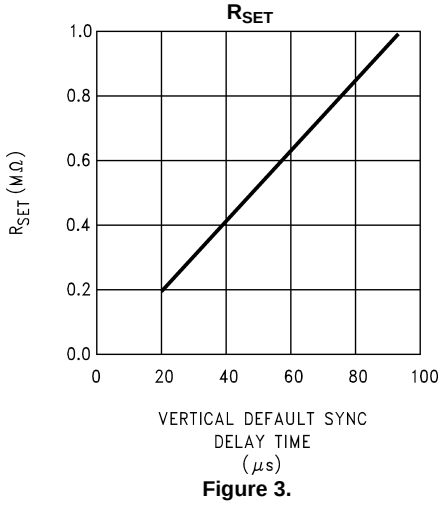


Figure 3.

Burst/Black Level Gate Time vs R_{SET}

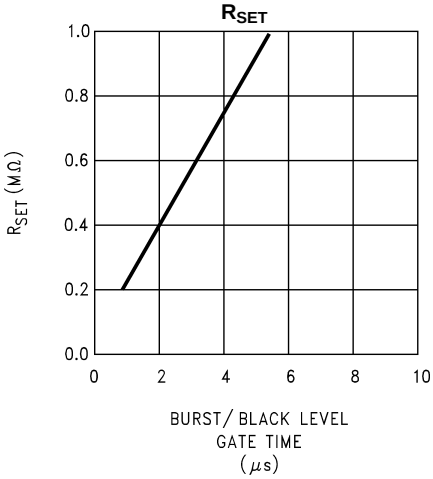


Figure 4.

Vertical Pulse Width vs R_{SET}

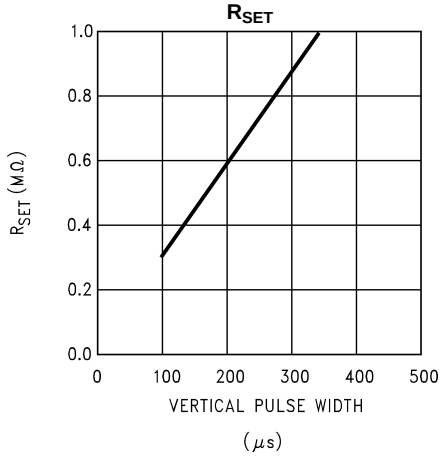


Figure 5.

Vertical Pulse Width vs Temperature

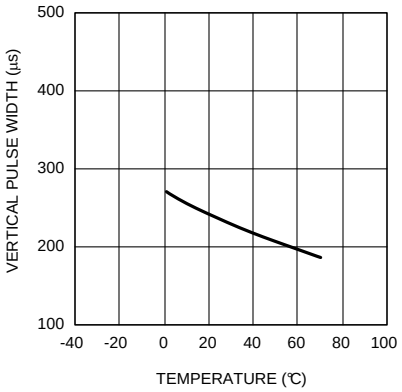


Figure 6.

Supply Current vs Supply Voltage

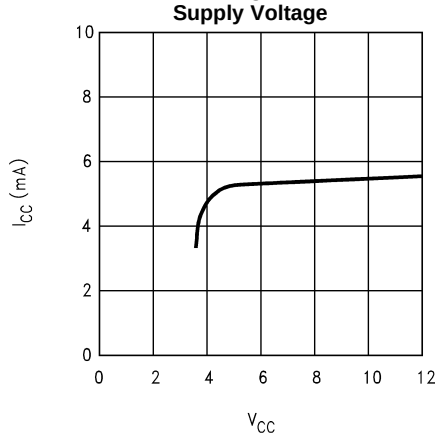


Figure 7.

APPLICATION NOTES

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The LM1881 operates from a single supply voltage between 5V DC and 12V DC. The only required external components besides a power supply decoupling capacitor at pin 8 and a set current decoupling capacitor at pin 6, are the composite input coupling capacitor at pin 2 and one resistor at pin 6 that sets internal current levels. The resistor on pin 6 (i.e. R_{set}) allows the LM1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C; composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The odd/even output level identifies which video field of an interlaced video source is present at the input. The outputs from the LM1881 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

To better understand the LM1881 timing information and the type of signals that are used, refer to Figure 8*(a-e)* which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

COMPOSITE SYNC OUTPUT

The composite sync output, Figure 8*(b)*, is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on Figure 8*(a)*. This threshold separation is independent of the signal amplitude, therefore, for a 2V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA,

Normally the signal source for the LM1881 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75Ω, a 620Ω resistor in series with the source and a 510 pF capacitor to ground will form a low pass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform (Figure 9). To understand the generation of the vertical sync pulse, refer to the lower left hand section Figure 9. Note that there are two comparators in the section. One comparator has an internally generated voltage reference called V_1 going to one of its inputs. The other comparator has an internally generated voltage reference called V_2 going to one of its inputs. Both comparators have a common input at their noninverting input coming from the internal integrator. The internal integrator is used for integrating the composite sync signal. This signal comes from the input side of the composite sync buffer and are **positive** going sync pulses. The capacitor to the integrator is internal to the LM1881. The capacitor charge current is set by the value of the external resistor R_{SET}. The output of the integrator is going to be at a low voltage during the normal horizontal lines because the integrator has a very short time to charge the capacitor, which is during the horizontal sync period. The equalization pulses will keep the output voltage of the integrator at about the same level, below the V_1. During the vertical sync period the narrow going positive pulses shown in Figure 8 is called the serration pulse. The wide negative portion of the vertical sync period is called the vertical sync pulse. At the start of the vertical sync period, before the first Serration pulse occurs, the integrator now charges the capacitor to a much higher voltage. At the first serration

pulse the integrator output should be between V_1 and V_2. This would give a high level at the output of the comparator with V_1 as one of its inputs. This high is clocked into the "D" flip-flop by the falling edge of the serration pulse (remember the sync signal is inverted in this section of the LM1881). The "Q" output of the "D" flip-flop goes through the OR gate, and sets the R/S flip-flop. The output of the R/S flip-flop enables the internal oscillator and also clocks the ODD/EVEN "D" flip-flop. The ODD/EVEN field pulse operation is covered in the next section. The output of the oscillator goes to a divide by 8 circuit, thus resetting the R/S flip-flop after 8 cycles of the oscillator. The frequency of the oscillator is established by the internal capacitor going to the oscillator and the external R_{SET}. The "$\overline{Q}$" output of the R/S flip-flop goes to pin 3 and is the actual vertical sync output of the LM1881. By clocking the "D" flip-flop at the start of the first serration pulse means that the vertical sync output pulse starts at this point in time and lasts for eight cycles of the internal oscillator as shown in Figure 8.

How R_{SET} affects the integrator and the internal oscillator is shown under the Typical Performance Characteristics. The first graph is "R_{SET} Value Selection vs Vertical Serration Pulse Separation". For this graph to be valid, the vertical sync pulse should last for at least 85% of the horizontal half line (47% of a full horizontal line). A vertical sync pulse from any standard should meet this requirement; both NTSC and PAL do meet this requirement (the serration pulse is the remainder of the period, 10% to 15% of the horizontal half line). Remember this pulse is a positive pulse at the integrator but negative in Figure 8. This graph shows how long it takes the integrator to charge its internal capacitor above V_1.

With R_{SET} too large the charging current of the integrator will be too small to charge the capacitor above V_1, thus there will be no vertical synch output pulse. As mentioned above, R_{SET} also sets the frequency of the internal oscillator. If the oscillator runs too fast its eight cycles will be shorter than the vertical sync portion of the composite sync. Under this condition another vertical sync pulse can be generated on one of the later serration pulse after the divide by 8 circuit resets the R/S flip-flop. The first graph also shows the minimum R_{SET} necessary to prevent a double vertical pulse, assuming that the serration pulses last for only three full horizontal line periods (six serration pulses for NTSC). The actual pulse width of the vertical sync pulse is shown in the "Vertical Pulse Width vs R_{SET}" graph. Using NTSC as an example, lets see how these two graphs relate to each other. The Horizontal line is 64 µs long, or 32 µs for a horizontal half line. Now round this off to 30 µs. In the "R_{SET} Value Selection vs Vertical Serration Pulse Separation" graph the minimum resistor value for 30 µs serration pulse separation is about 550 kΩ. Going to the "Vertical Pulse Width vs R_{SET}" graph one can see that 550 kΩ gives a vertical pulse width of about 180 µs, the total time for the vertical sync period of NTSC (3 horizontal lines). A 550 kΩ will set the internal oscillator to a frequency such that eight cycles gives a time of 180 µs, just long enough to prevent a double vertical sync pulse at the vertical sync output of the LM1881.

The LM1881 also generates a default vertical sync pulse when the vertical sync period is unusually long and has no serration pulses. With a very long vertical sync time the integrator has time to charge its internal capacitor above the voltage level V_2. Since there is no falling edge at the end of a serration pulse to clock the "D" flip-flop, the only high signal going to the OR gate is from the default comparator when output of the integrator reaches V_2. At this time the R/S flip-flop is toggled by the default comparator, starting the vertical sync pulse at pin 3 of the LM1881. If the default vertical sync period ends before the end of the input vertical sync period, then the falling edge of the vertical sync (positive pulse at the "D" flip-flop) will clock the high output from the comparator with V_1 as a reference input. This will retrigger the oscillator, generating a second vertical sync output pulse. The "Vertical Default Sync Delay Time vs R_{SET}" graph shows the relationship between the R_{SET} value and the delay time from the start of the vertical sync period before the default vertical sync pulse is generated. Using the NTSC example again the smallest resistor for R_{SET} is 500 kΩ. The vertical default time delay is about 50 µs, much longer than the 30 µs serration pulse spacing.

A common question is how can one calculate the required R_{SET} with a video timing standard that has no serration pulses during the vertical blanking. If the default vertical sync is to be used this is a very easy task. Use the "Vertical Default Sync Delay Time vs R_{SET}" graph to select the necessary R_{SET} to give the desired delay time for the vertical sync output signal. If a second pulse is undesirable, then check the "Vertical Pulse Width vs R_{SET}" graph to make sure the vertical output pulse will extend beyond the end of the input vertical sync period. In most systems the end of the vertical sync period may be very accurate. In this case the preferred design may be to start the vertical sync pulse at the end of the vertical sync period, similar to starting the vertical sync pulse after the first serration pulse. A VGA standard is to be used as an example to show how this is done. In this standard a horizontal line is 32 µs long. The vertical sync period is two horizontal lines long, or 64 µs. The vertical default sync delay time **must be longer** than the vertical sync period of 64 µs. In this case R_{SET} must be larger than 680 kΩ. R_{SET} must still be small enough for the output of the integrator to reach V_1 before the end of the vertical period of the input pulse. The first graph can be used to confirm that R_{SET} is small enough for the integrator.

Instead of using the vertical serration pulse separation, use the actual pulse width of the vertical sync period, or 64 µs in this example. This graph is linear, meaning that a value as large as 2.7 MΩ can be used for R_{SET} (twice the value as the maximum at 30 µs). Due to leakage currents it is advisable to keep the value of R_{SET} under 2.0 MΩ. In this example a value of 1.0 MΩ is selected, well above the minimum of 680 kΩ. With this value for R_{SET} the pulse width of the vertical sync output pulse of the LM1881 is about 340 µs.

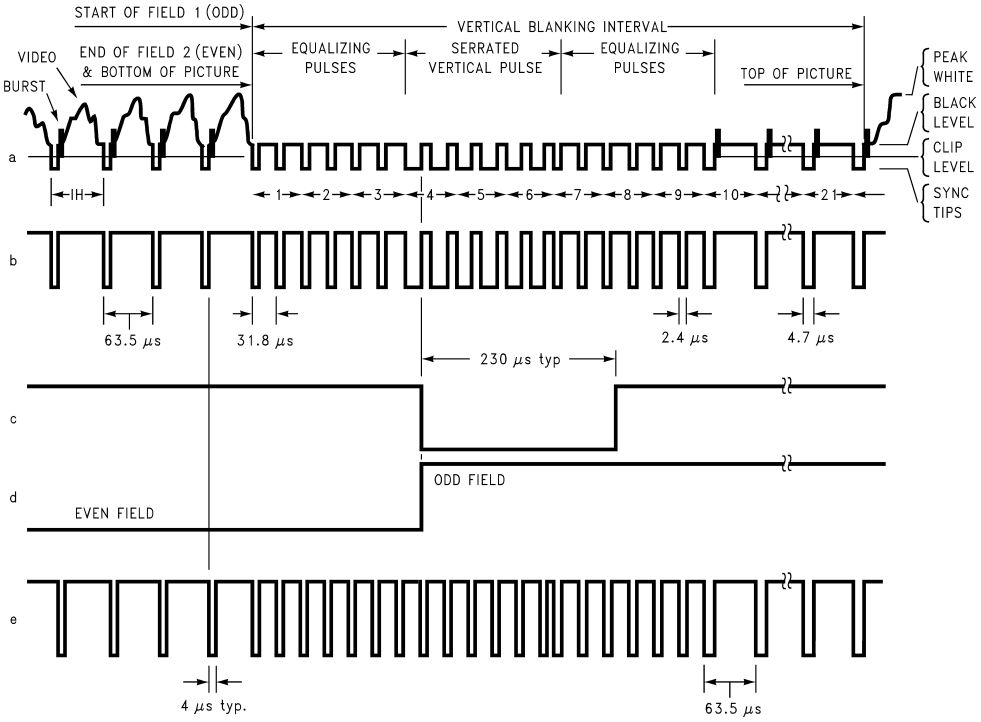
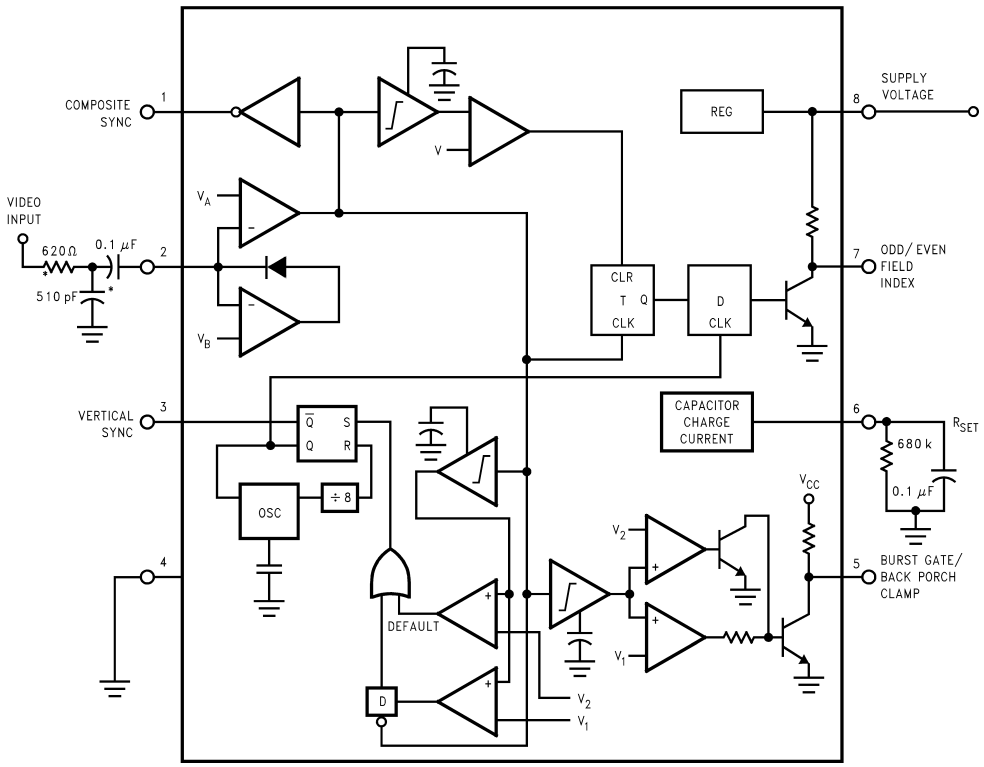


Figure 8. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp



*Components Optional, See Text

Figure 9.

ODD/EVEN FIELD PULSE

An unusual feature of LM1881 is an output level from Pin 7 that identifies the video field present at the input to the LM1881. This can be useful in frame memory storage applications or in extracting test signals that occur in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the “odd field” or “even field”. The “even field” or “field 2” has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. Figure 8*(a)* shows the end of the even field and the start of the odd field.

To detect the odd/even fields the LM1881 again integrates the composite sync waveform (Figure 9). A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flip-flop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

BURST/BACKPORCH OUTPUT PULSE

In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 µs long, is also the black level reference for the subsequent video scan line. The LM1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 µs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60 Hz–120 Hz) vertical scan rates.

APPLICATIONS

Apart from extracting a composite sync signal free of video information, the LM1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate/backporch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd/even field lever allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Since the vertical output pulse from the LM1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

VIDEO LINE SELECTOR

The circuit in Figure 10 puts out a singe video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the LM1881's vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (CD4066BC) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd/even field index output must be used instead of the vertical output pulse (invert the field index output to select the odd field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

MULTIPLE CONTIGUOUS VIDEO LINE SELECTOR WITH BLACK LEVEL RESTORATION

The circuit in Figure 11 will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the LM1881 is used to gate the video input's black level through a low pass filter (10 kΩ, 10 µF) providing black level restoration at the video output when the output selected line(s) is not being gated through.

Typical Applications

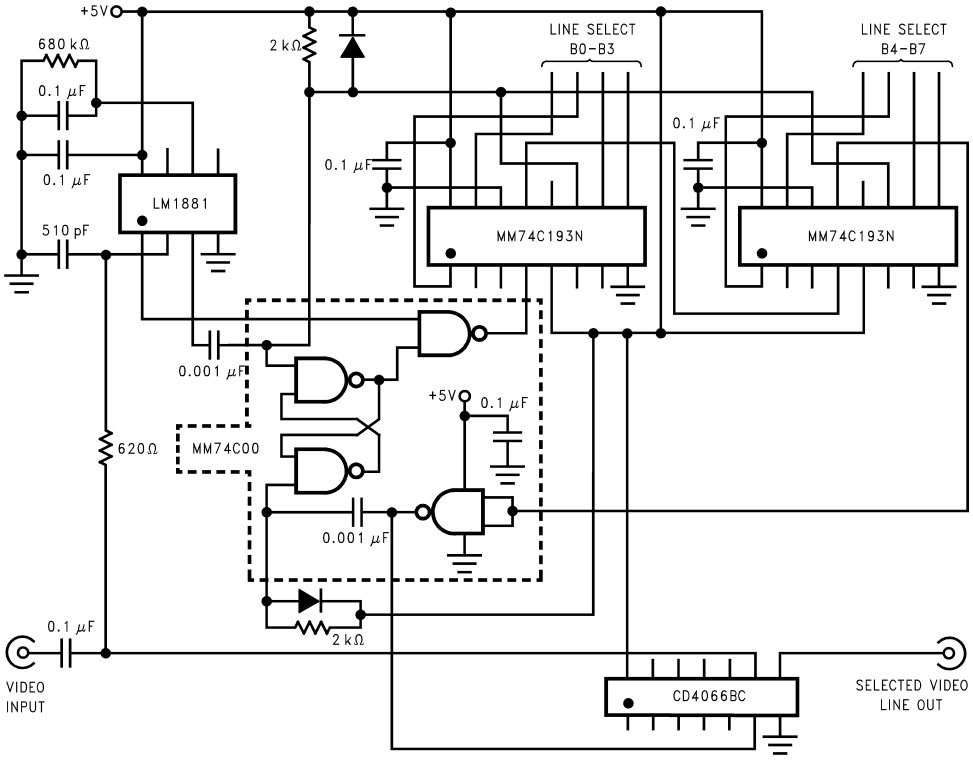


Figure 10. Video Line Selector

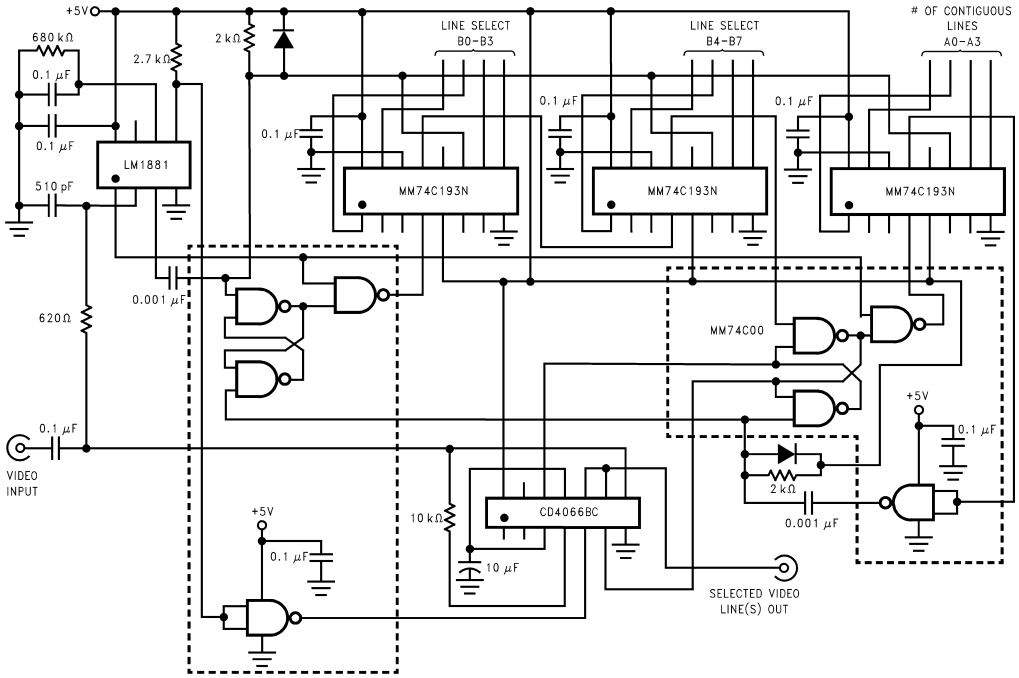


Figure 11. Multiple Contiguous Video Line Selector with Black Level Restoration

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM1881M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 1881M	
LM1881M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 1881M	Samples
LM1881MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM 1881M	Samples
LM1881N	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	0 to 70	LM1881N	
LM1881N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM1881N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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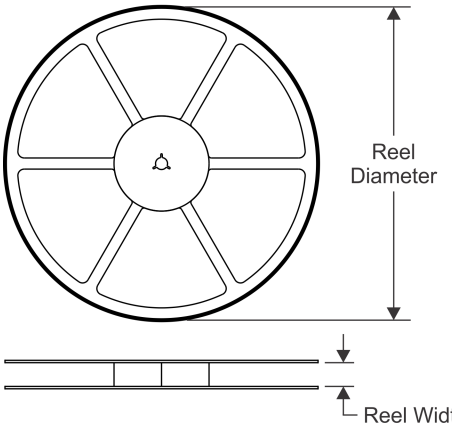
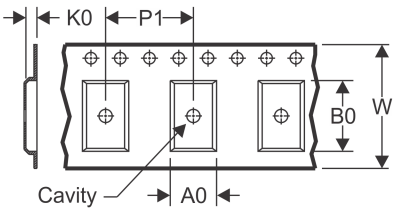
TAPE AND REEL INFORMATION

REEL DIMENSIONS

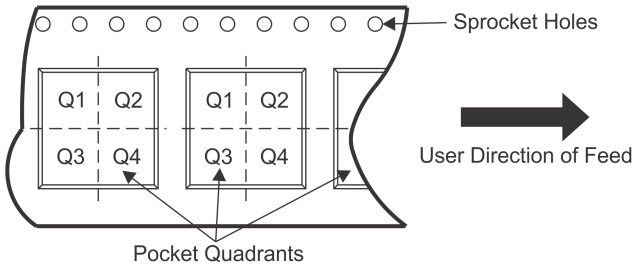


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

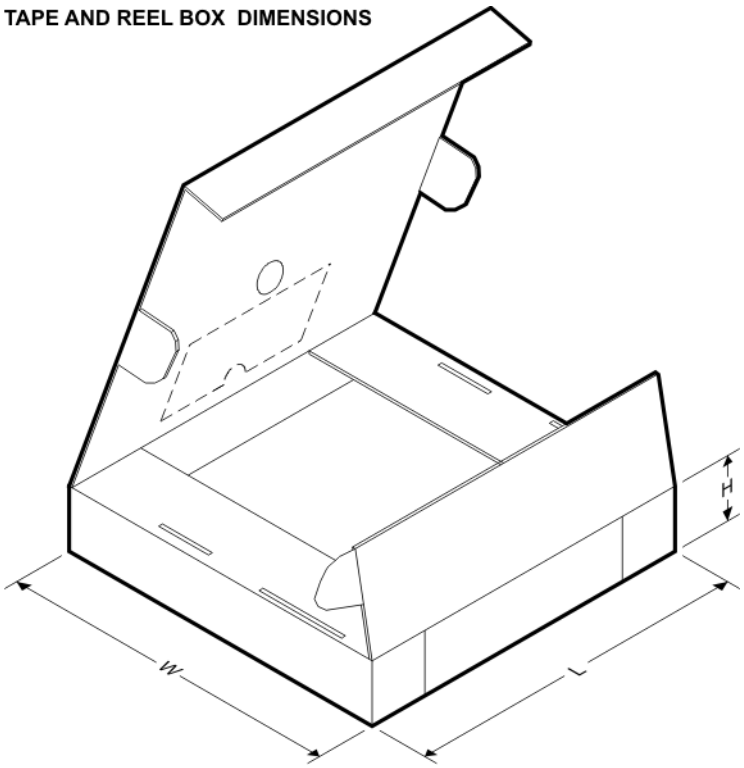
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM1881MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

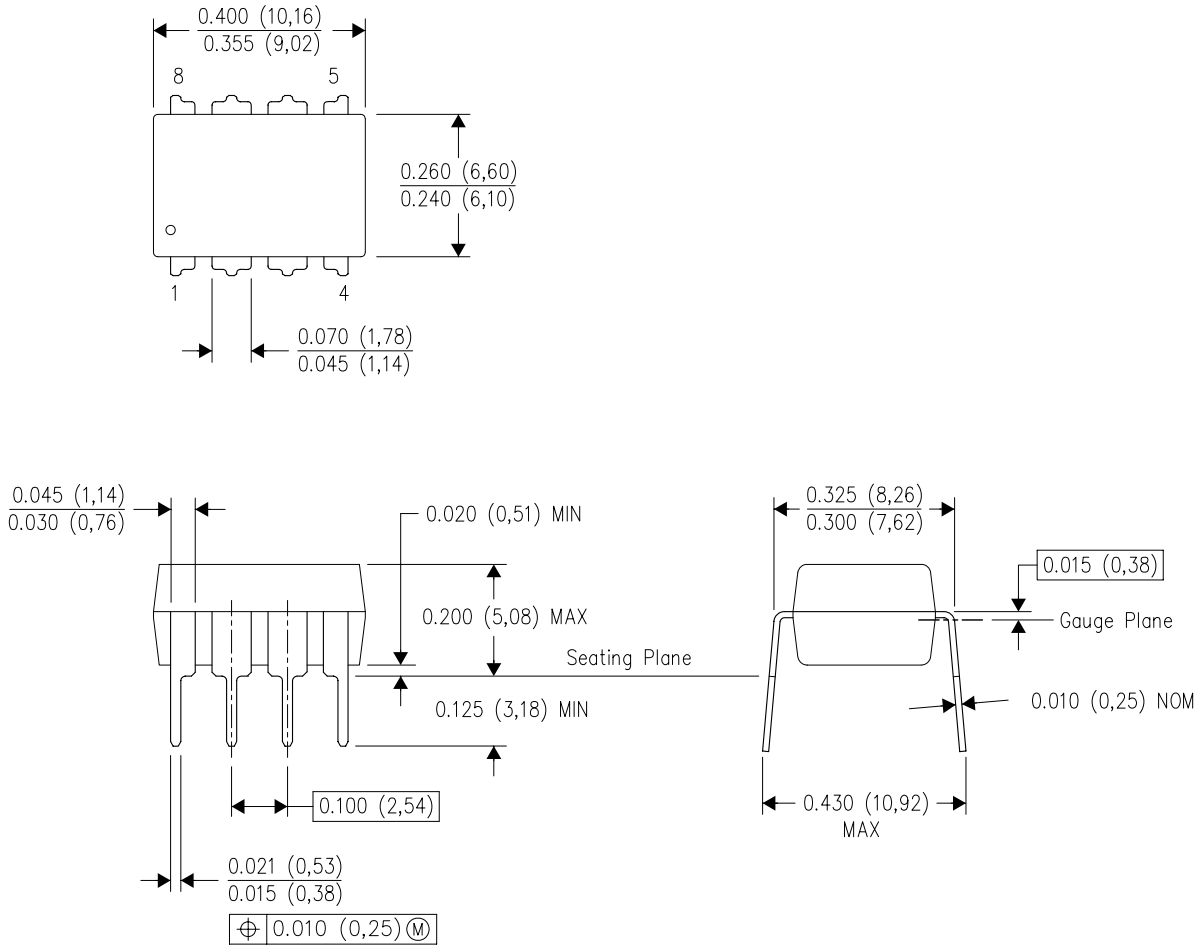
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

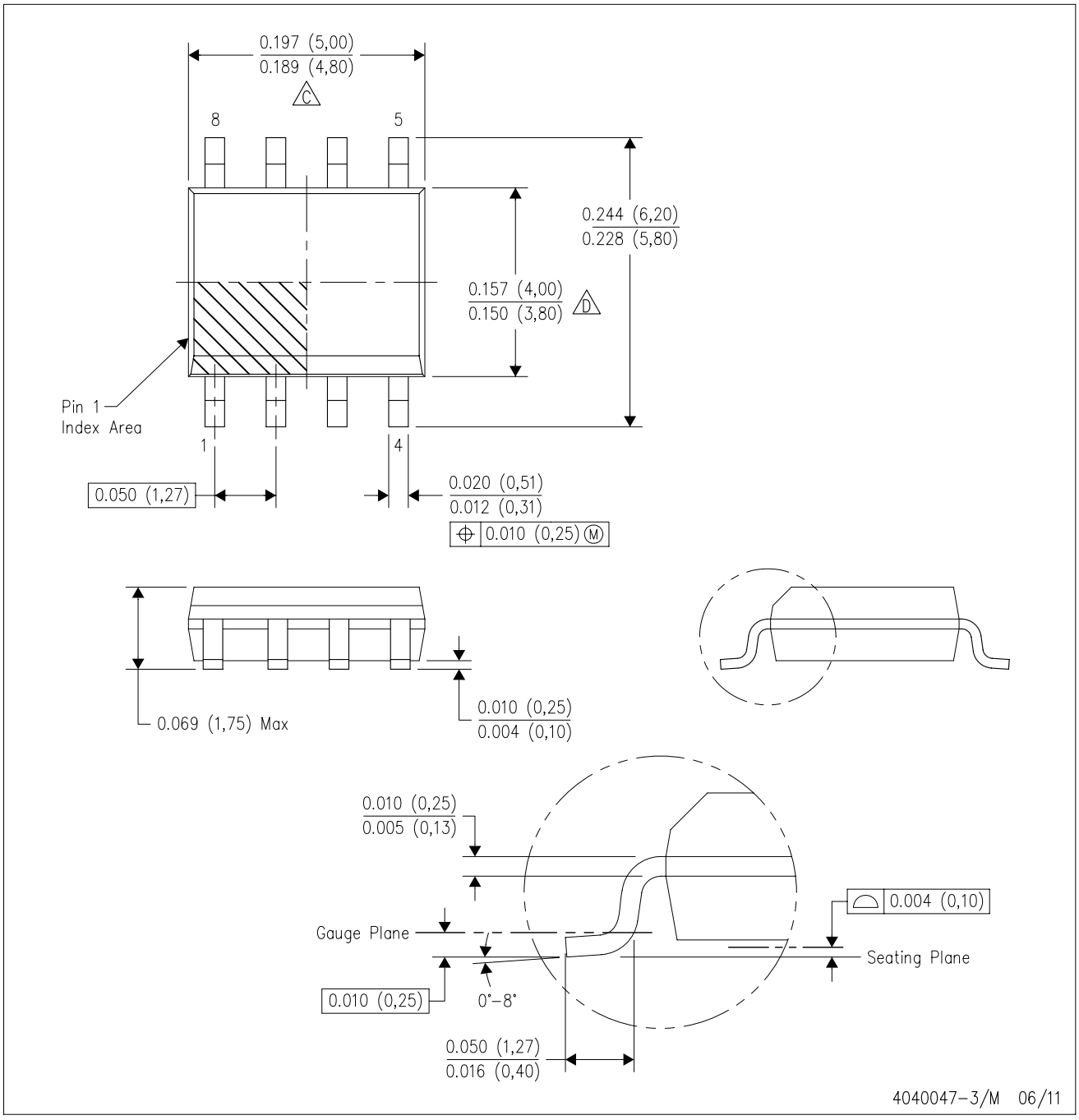
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM1881MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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