

## 74LCX16501

### 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

#### General Description

The LCX16501 is an 18-bit universal bus transceiver combining D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable ( $\overline{\text{OEAB}}$  and  $\overline{\text{OEBA}}$ ), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs.

The LCX16501 is designed for low voltage (2.5V or 3.3V)  $V_{\text{CC}}$  applications with capability of interfacing to a 5V signal environment.

The LCX16501 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power.

#### Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V  $V_{\text{CC}}$  specifications provided
- 6.0 ns  $t_{\text{PD}}$  max ( $V_{\text{CC}} = 3.3\text{V}$ ), 20  $\mu\text{A}$   $I_{\text{CC}}$  max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm 24$  mA Output Drive ( $V_{\text{CC}} = 3.0\text{V}$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model < 200V

**Note 1:** To ensure the high-impedance state during power up or down  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  and OE tied to GND through a resistor the minimum value of the resistor is determined by the current-sourcing capability of the driver

#### Ordering Code:

Order Number	Package Number	Package Description
74LCX16501MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX16501MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available on Tape and Reel. Specify by appending the suffix letter 'X' to the ordering code.

74LCX16501 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs



Absolute Maximum Ratings (Note 5)						
Symbol	Parameter	Value	Conditions	Units		
$V_{CC}$	Supply Voltage	-0.5 to +7.0		V		
$V_I$	DC Input Voltage	-0.5 to +7.0		V		
$V_O$	DC Output Voltage	-0.5 to +7.0 -0.5 to $V_{CC} + 0.5$	Output in 3-STATE Output in HIGH or LOW State (Note 6)	V		
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA		
$I_{OK}$	DC Output Diode Current	-50 +50	$V_O < GND$ $V_O > V_{CC}$	mA		
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA		
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$		mA		
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA		
$T_{STG}$	Storage Temperature	-65 to +150		°C		
Recommended Operating Conditions (Note 7)						
Symbol	Parameter	Min	Max	Units		
$V_{CC}$	Supply Voltage	Operating	2.0	3.6	V	
		Data Retention	1.5	3.6		
$V_I$	Input Voltage	0	5.5	V		
$V_O$	Output Voltage	HIGH or LOW State	0	$V_{CC}$	V	
		3-STATE	0	5.5		
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0V - 3.6V$		$\pm 24$	mA	
		$V_{CC} = 2.7V - 3.0V$		$\pm 12$		
		$V_{CC} = 2.3V - 2.7V$		$\pm 8$		
$T_A$	Free-Air Operating Temperature	-40	85	°C		
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V		
<p><b>Note 5:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The 'Recommended Operating Conditions' table will define the conditions for actual device operation.</p> <p><b>Note 6:</b> <math>I_O</math> Absolute Maximum Rating must be observed.</p> <p><b>Note 7:</b> Unused (inputs or I/Os) must be held HIGH or LOW. They may not float.</p>						
DC Electrical Characteristics						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^\circ C$ to $+85^\circ C$		Units
				Min	Max	
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
$V_{IL}$	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8 mA$	2.3	1.8		
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6		0.2	V
		$I_{OL} = 8 mA$	2.3		0.6	
		$I_{OL} = 12 mA$	2.7		0.4	
		$I_{OL} = 16 mA$	3.0		0.4	
		$I_{OL} = 24 mA$	3.0		0.55	
$I_I$	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE I/O Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 - 3.6		$\pm 5.0$	$\mu A$
$I_{OFF}$	Power-Off Leakage Current	$V_I$ or $V_O = 5.5V$	0		10	$\mu A$

## DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		20	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 8)	2.3 – 3.6		±20	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V	2.3 – 3.6		500	μA

**Note 8:** Outputs disabled or 3-STATE only

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF		
		Min	Max	Min	Max	Min	Max	
t <sub>MAX</sub>	Maximum Clock Frequency	170						MHz
t <sub>PHL</sub>	Propagation Delay	1.5	6.0	1.5	7.0	1.5	7.2	ns
t <sub>PLH</sub>	Bus to Bus	1.5	6.0	1.5	7.0	1.5	7.2	
t <sub>PHL</sub>	Propagation Delay	1.5	6.7	1.5	8.0	1.5	8.4	ns
t <sub>PLH</sub>	Clock to Bus	1.5	6.7	1.5	8.0	1.5	8.4	
t <sub>PHL</sub>	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t <sub>PLH</sub>	LE to Bus	1.5	7.0	1.5	8.0	1.5	8.4	
t <sub>PZL</sub>	Output Enable Time	1.5	7.2	1.5	8.2	1.5	9.4	ns
t <sub>PZH</sub>		1.5	7.2	1.5	8.2	1.5	9.4	
t <sub>PLZ</sub>	Output Disable Time	1.5	7.0	1.5	8.0	1.5	8.4	ns
t <sub>PHZ</sub>		1.5	7.0	1.5	8.0	1.5	8.4	
t <sub>S</sub>	Setup Time	2.5		2.5		3.0		ns
t <sub>H</sub>	Hold Time	1.5		1.5		2.0		ns
t <sub>W</sub>	Pulse Width	3.0		3.0		3.5		ns
t <sub>OSHL</sub>	Output to Output Skew (Note 9)		1.0					ns
t <sub>OSLH</sub>			1.0					

**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction: either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

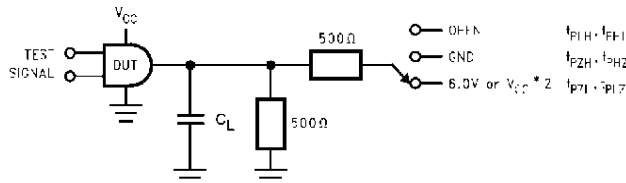
## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C	Units
				Typical	
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6	
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8	V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	-0.6	

## Capacitance

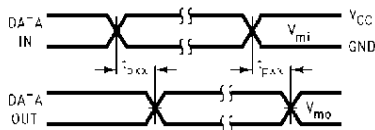
Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	20	pF

**AC LOADING and WAVEFORMS** Generic for LCX Family

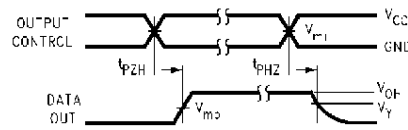


**FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)**

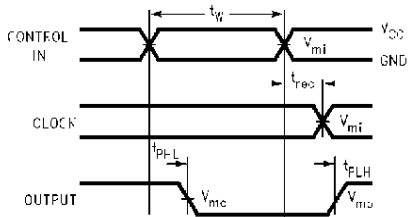
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



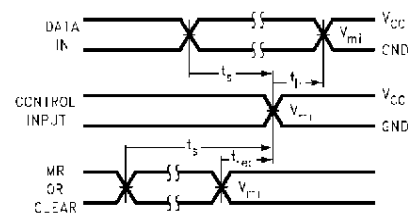
**Waveform for Inverting and Non-Inverting Functions**



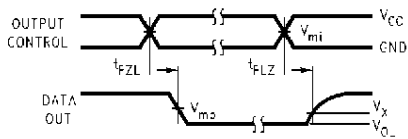
**3-STATE Output High Enable and Disable Times for Logic**



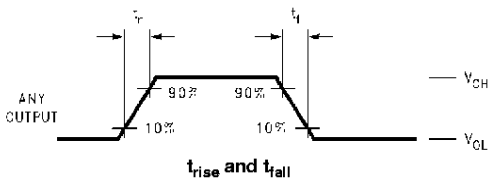
**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**Setup Time, Hold Time and Recovery Time for Logic**



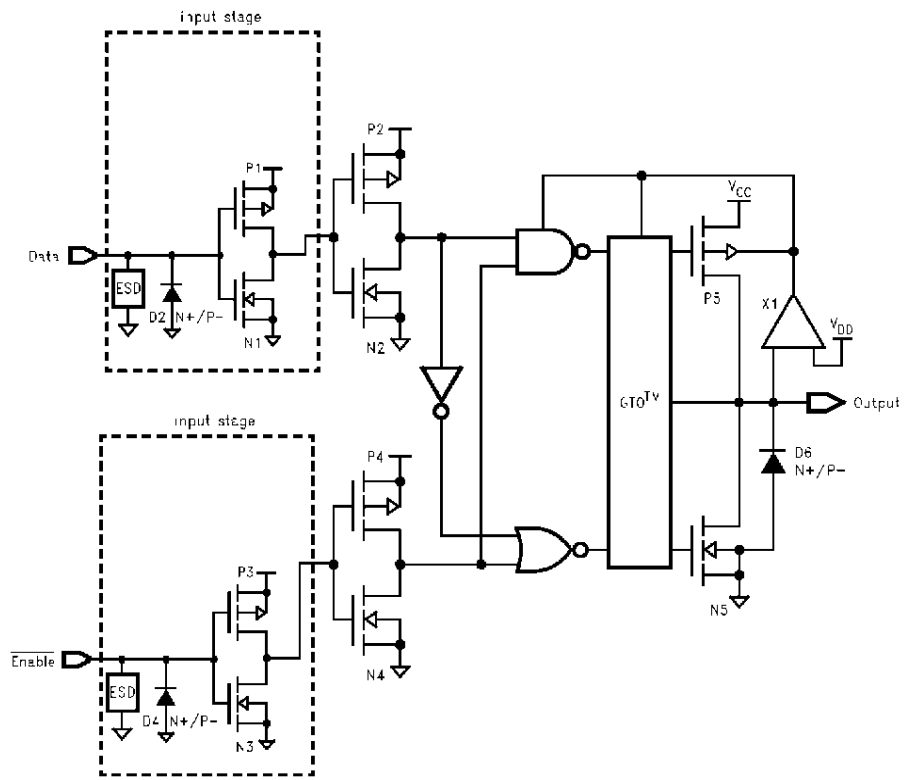
**3-STATE Output Low Enable and Disable Times for Logic**



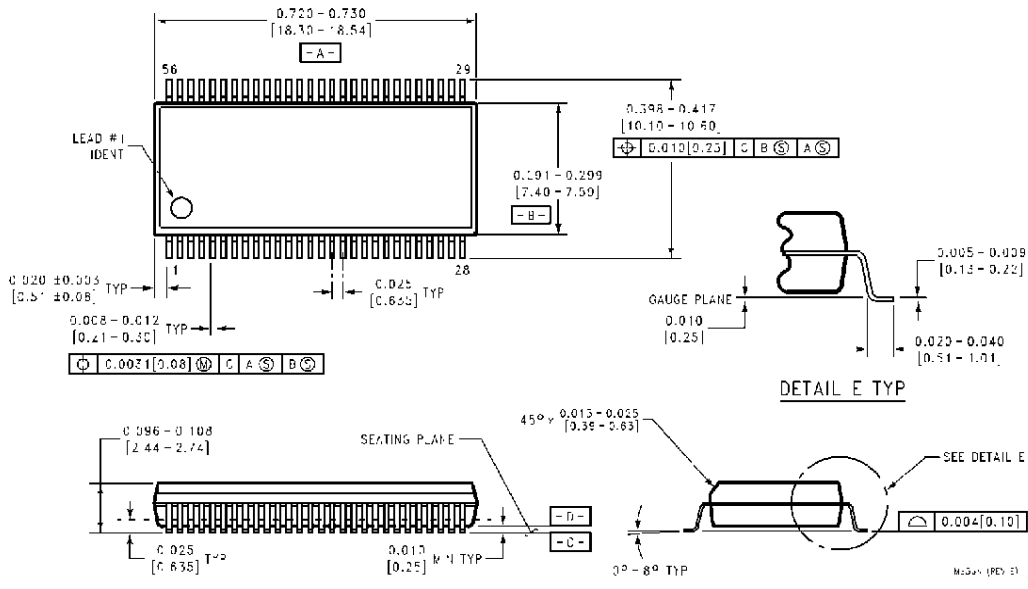
**FIGURE 2. Waveforms**  
(Input Characteristics;  $f = 1MHz$ ,  $t_R = t_F = 3ns$ )

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

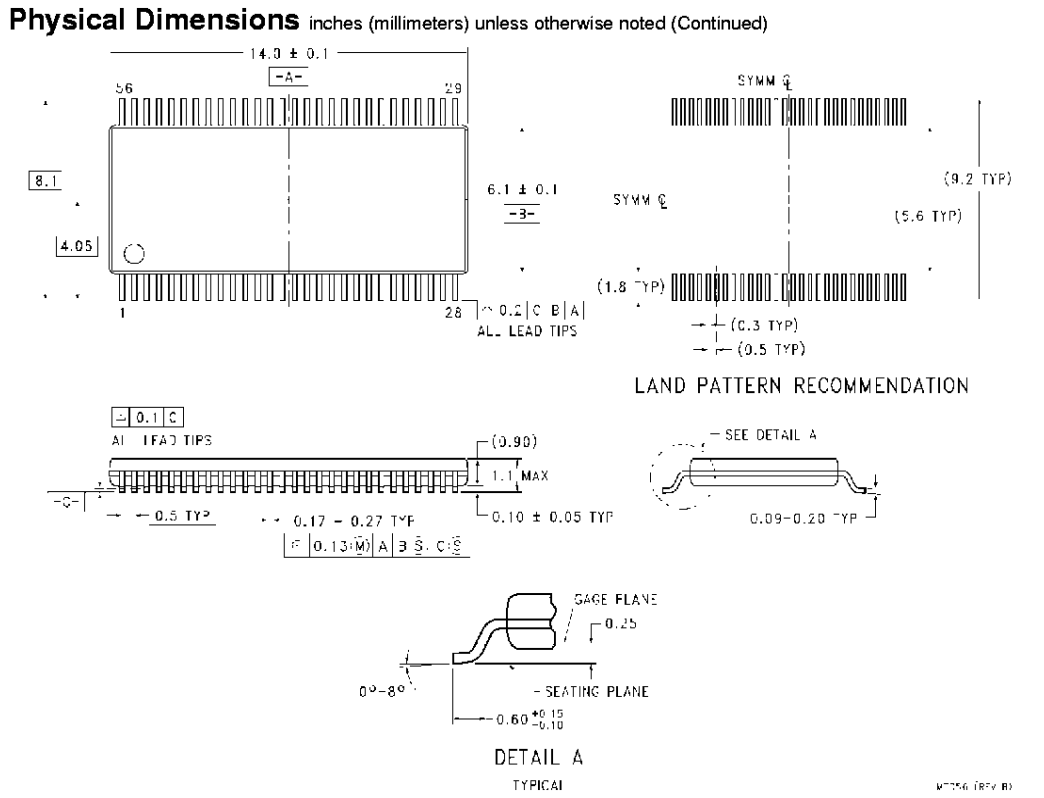


**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS56A**

MS56A (REV. 21)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56

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