FAIRCHILD SEMICONDUCTOR™

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GTLP18T612
18-Bit LVTTL/GTLP Universal Bus Transceiver

General Description

The GTLP18T612 is an 18-bit universal bus transceiver which provides LVTTL to GTLP signal level translation. It allows for transparent, latched and clocked modes of data transfer. The device provides a high speed interface for cards operating at LVTTL logic levels and a backplane operating at GTLP logic levels. High speed backplane operation is a direct result of GTLP's reduced output swing (< 1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transistor logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated. Its function is similar to BTL or GTL but with different output levels and receiver thresholds. GTLP output LOW level is less than 0.5V, the output HIGH is 1.5V and the receiver threshold is 1.0V.

Features

- Bidirectional interface between GTLP and LVTTL logic levels
- Designed with edge rate control circuitry to reduce output noise on the GTLP port
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustibility
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- TTL compatible driver and control inputs
- Designed using Fairchild advanced BiCMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- D-type flip-flop, latch and transparent data paths
- A Port source/sink –24mA/+24mA
- B Port sink +50mA
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Ordering Code:

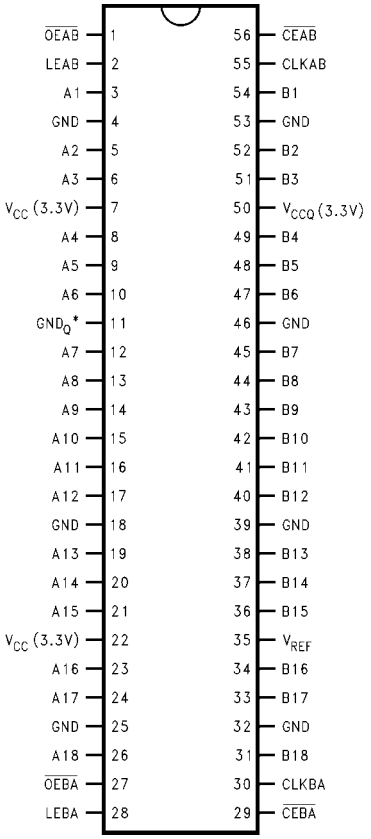
Order Number	Package Number	Package Description
GTLP18T612G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
GTLP18T612MEA (Note 2)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
GTLP18T612MTD (Note 2)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 1: Ordering code "G" indicates Trays.

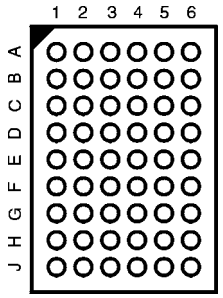
Note 2: Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for SSOP and TSSOP



Pin Assignments for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable (Active LOW) (LVTTL Level)
$\overline{OEBA}$	B-to-A Output Enable (Active LOW) (LVTTL Level)
$\overline{CEAB}$	A-to-B Clock/LE Enable (Active LOW) (LVTTL Level)
$\overline{CEBA}$	B-to-A Clock/LE Enable (Active LOW) (LVTTL Level)
LEAB	A-to-B Latch Enable (Transparent HIGH) (LVTTL Level)
LEBA	B-to-A Latch Enable (Transparent HIGH) (LVTTL Level)
V_{REF}	GTLP Input Threshold Reference Voltage
CLKAB	A-to-B Clock (LVTTL Level)
CLKBA	B-to-A Clock (LVTTL Level)
A1–A18	A-to-B Data Inputs or B-to-A 3-STATE Outputs
B1–B18	B-to-A Data Inputs or A-to-B Open Drain Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	A_2	A_1	OEAB	CLKAB	B_2	B_1
B	A_4	A_3	LEAB	CEAB	B_4	B_3
C	A_6	A_5	V_{CC}	V_{CC}	B_6	B_5
D	A_8	A_7	GND	GND	B_8	B_7
E	A_{10}	A_9	GND	GND	B_{10}	B_9
F	A_{12}	A_{11}	GND	GND	B_{12}	B_{11}
G	A_{14}	A_{13}	V_{CC}	V_{REF}	B_{14}	B_{13}
H	A_{16}	A_{15}	OEBA	CEBA	B_{16}	B_{15}
J	A_{18}	A_{17}	LEBA	CLKBA	B_{18}	B_{17}

Functional Description

The GTLP18T612 is an 18 bit registered transceiver containing D-type flip-flop, latch and transparent modes of operation for the data path. Data flow in each direction is controlled by the clock enables ($\overline{CEAB}$ and $\overline{CEBA}$), latch enables (LEAB and LEBA), clock (CLKAB and CLKBA) and output enables ($\overline{OEAB}$ and $\overline{OEBA}$). The clock enables ($\overline{CEAB}$ and $\overline{CEBA}$) and the output enables ($\overline{OEAB}$ and $\overline{OEBA}$) control the 18 bits of data for the A-to-B and B-to-A directions respectively.

For A-to-B data flow, when $\overline{CEAB}$ is LOW, the device operates on the LOW-to-HIGH transition of CLKAB for the flip-flop and on the HIGH-to-LOW transition of LEAB for the latch path. That is, if $\overline{CEAB}$ is LOW and LEAB is LOW the A data is latched regardless as to the state of CLKAB (HIGH or LOW) and if LEAB is HIGH the device is in transparent mode. When $\overline{OEAB}$ is LOW the outputs are active. When $\overline{OEAB}$ is HIGH the outputs are HIGH impedance. The data flow of B-to-A is similar except that $\overline{CEBA}$, $\overline{OEBA}$, LEBA, and CLKBA are used.

Truth Table

(Note 3)

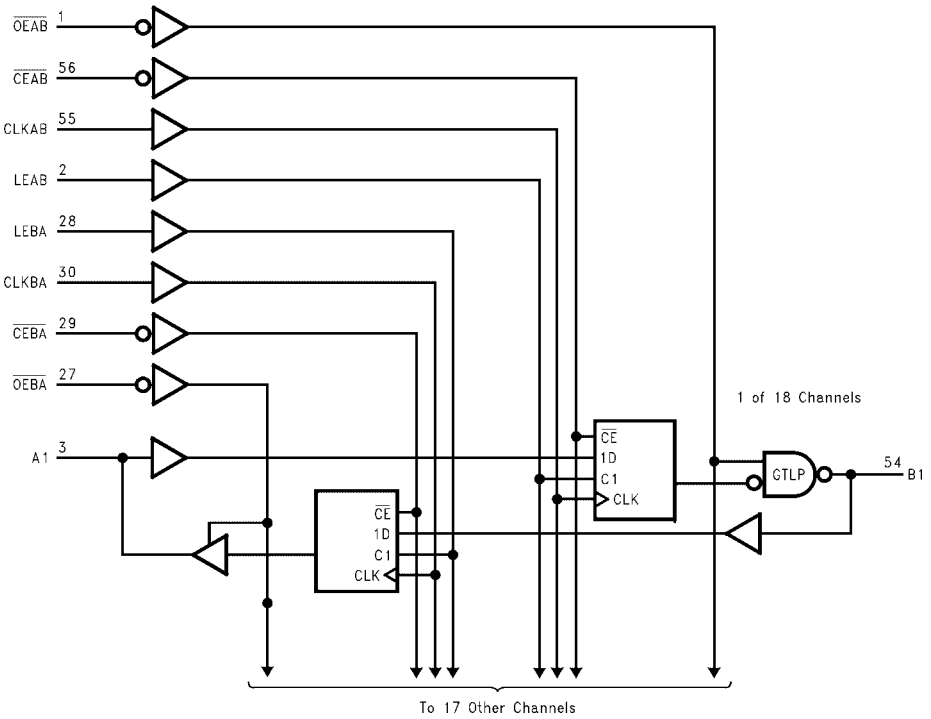
Inputs					Output	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A	B	
X	H	X	X	X	Z	Latched
L	L	L	H	X	B_0 (Note 4)	Storage
L	L	L	L	X	B_0 (Note 5)	of A Data
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked
L	L	L	↑	H	H	Storage
						of A Data
H	L	L	X	X	B_0 (Note 5)	Clock Inhibit

Note 3: A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

Note 4: Output level before the indicated steady state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Note 5: Output level before the indicated steady-state input conditions were established.

Logic Diagram



Absolute Maximum Ratings (Note 6)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 7)	−0.5V to V_{CC} + 0.5V
DC Output Sink Current into	
A Port I_{OL}	48 mA
DC Output Source Current from	
A Port I_{OH}	−48 mA
DC Output Sink Current into	
B Port in the LOW State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
ESD Performance	>2000V
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 8)

Supply Voltage V_{CC}/V_{CCQ}	3.15V to 3.45V
Bus Termination Voltage (V_{TT})	
GTLP	1.47V to 1.53V
V_{REF}	0.98V to 1.02V
Input Voltage (V_I)	
on A Port and Control Pins	0.0V to 3.45V
on B Port	0.0V to 3.45V
HIGH Level Output Current (I_{OH})	
A Port	−24 mA
LOW Level Output Current (I_{OL})	
A Port	+24 mA
B Port	+50 mA
Operating Temperature (T_A)	−40°C to +85°C

Note 6: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions in not implied.

Note 7: I_O Absolute Maximum Rating must be observed.

Note 8: Unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 9)	Max	Units
V_{IH}	B Port			V_{REF} +0.05		V_{TT}	V
	Others			2.0			
V_{IL}	B Port			0.0		V_{REF} − 0.05	V
	Others					0.8	
V_{REF}	GTLP (Note 10)				1.0		V
	GTL				0.8		
V_{IK}		V_{CC} = 3.15V	I_I = −18 mA			−1.2	V
V_{OH}	A Port	V_{CC}, V_{CCQ} = Min to Max (Note 11)	I_{OH} = −100 µA	V_{CC} −0.2			V
		V_{CC} = 3.15V	I_{OH} = −8 mA	2.4			
			I_{OH} = -24mA	2.0			
V_{OL}	A Port	V_{CC}, V_{CCQ} = Min to Max (Note 11)	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15V	I_{OL} = 24mA			0.5	
	B Port	V_{CC} = 3.15V	I_{OL} = 40 mA			0.40	V
			I_{OL} = 50 mA			0.55	
I_I	Control Pins	V_{CC} = Min to Max (Note 11)	V_I = 3.45V or 0V			±5	µA
	A Port	V_{CC} = 3.45V	V_I = 0V			−10	µA
			V_I = 3.45			10	
	B Port	V_{CC} = 3.45V	V_I = V_{CC}			5	µA
			V_I = 0			−5	
I_{OFF}	A Port and Control Pins	V_{CC} = 0	V_I or V_O = 0 to 3.45V			30	µA
$I_{I(hold)}$	A Port	V_{CC} = 3.15V	V_I = 0.8V	75			µA
			V_I = 2.0V			−75	
I_{OZH}	A Port	V_{CC} = 3.45V	V_O = 3.45			10	µA
	B Port		V_O = 1.5V			5	
I_{OZL}	A Port	V_{CC} = 3.45V	V_O = 0V			−10	µA
	B Port		V_O = 0.55V			−5	
I_{CC} (V_{CC}/V_{CCQ})	A or B Ports	V_{CC} = 3.45V	Outputs HIGH		30	40	mA
		I_O = 0	Outputs LOW		30	40	
		V_I = V_{CC} or GND	Outputs Disabled		30	45	

DC Electrical Characteristics (Continued)

Symbol		Test Conditions		Min	Typ (Note 9)	Max	Units
ΔI_{CC} (Note 12)	A Port and Control Pins	V_{CC} = 3.45V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V		0	2	mA
C_i	Control Pins		$V_I = V_{CC}$ or 0		6		pF
	A Port		$V_I = V_{CC}$ or 0		7.5		
	B Port		$V_I = V_{CC}$ or 0		9.0		

Note 9: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 3.3V, and T_A = 25°C.

Note 10: GTLP V_{REF} and V_{TT} are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, V_{TT} and Rterm can be adjusted beyond the recommended operating conditions to accommodate backplane impedances other than 50Ω, but must remain within the boundaries of the DC Absolute Maximum ratings. Similarly V_{REF} can be adjusted to optimize noise margin.

Note 11: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Note 12: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).

Symbol		Test Conditions	Min	Max	Unit
f_{MAX}	Maximum Clock Frequency		175		MHz
t_{WIDTH}	Pulse Duration	LEAB or LEBA HIGH	3.0		ns
		CLKAB or CLKBA HIGH or LOW	3.0		
t_{SU}	Setup Time	A before CLKAB↑	1.1		ns
		B before CLKBA↑	3.0		
		A before LEAB	1.1		
		B before LEBA	2.7		
		$\overline{CEAB}$ before CLKAB↑	1.2		
		$\overline{CEBA}$ before CLKBA↑	1.4		
t_{HOLD}	Hold Time	A after CLKAB↑	0.0		ns
		B after CLKBA↑	0.0		
		A after LEAB	0.8		
		B after LEBA	0.0		
		$\overline{CEAB}$ after CLKAB↑	1.0		
		$\overline{CEBA}$ after CLKBA↑	1.9		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).
C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 13)	Max	Unit
t_{PLH}	A	B	2.1	4.1	6.3	ns
t_{PHL}			1.0	2.7	4.4	
t_{PLH}	LEAB	B	2.2	4.2	6.3	ns
t_{PHL}			1.0	2.4	4.2	
t_{PLH}	CLKAB	B	2.2	4.4	6.5	ns
t_{PHL}			1.0	2.5	4.4	
t_{PLH}	$\overline{OEAB}$	B	2.0	3.8	5.6	ns
t_{PHL}			1.0	2.6	4.3	
t_{RISE}	Transition Time, B Outputs (20% to 80%)			3.1		ns
t_{FALL}	Transition Time, B Outputs (20% to 80%)			2.1		
t_{PLH}	B	A	1.8	3.8	5.8	ns
t_{PHL}			1.8	3.8	5.8	
t_{PLH}	LEBA	A	0.3	2.2	4.6	ns
t_{PHL}			0.4	2.4	4.6	
t_{PLH}	CLKBA	A	0.5	2.4	4.6	ns
t_{PHL}			0.6	2.6	4.6	
t_{PZH}, t_{PZL}	$\overline{OEBA}$	A	0.3	2.7	5.2	ns
t_{PHZ}, t_{PLZ}			0.3	2.5	5.2	

Note 13: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

Extended Electrical Characteristics

Over recommended ranges of supply voltage and operating free-air temperature V_{REF} = 1.0V (unless otherwise noted).
C_L = 30 pF for B Port and C_L = 50 pF for A Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 13)	Max	Unit
t_{OSLH} (Note 14)	A	B		0.8	1.0	ns
t_{OSHL} (Note 14)				0.3	0.5	ns
$t_{PV(HL)}$ (Note 15)(Note 16)	A	B			0.8	ns
t_{OSLH} (Note 14)	CLKAB	B		0.9	1.0	ns
t_{OSHL} (Note 14)				0.3	0.5	ns
$t_{PV(HL)}$ (Note 15)(Note 16)	CLKAB	B			0.8	ns
t_{OSLH} (Note 14)	B	A		0.7	1.0	ns
t_{OSHL} (Note 14)				0.6	1.0	ns
t_{OST} (Note 14)	B	A		0.7	1.1	ns
t_{PV} (Note 15)	B	A			1.5	ns
t_{OSLH} (Note 14)	CLKAB	A		0.5	1.0	ns
t_{OSHL} (Note 14)				0.6	1.0	ns
t_{OST} (Note 14)	CLKAB	A		1.1	1.2	ns
t_{PV} (Note 15)	CLKAB	A			1.5	ns

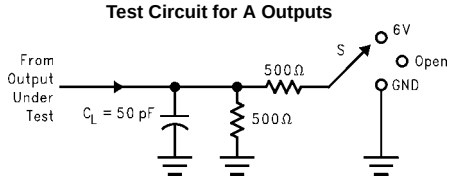
Note 14: t_{OSHL}/t_{OSLH} and t_{OST} - Output to output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs within the same packaged device. The specifications are given for specific worst case V_{CC} and temperature and apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 15: t_{PV} - Part to part skew is defined as the absolute value of the difference between the actual propagation delay for all outputs from device to device. The parameter is specified for a specific worst case V_{CC} and temperature. This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 16: Due to the open drain structure on GTLP outputs t_{OST} and $t_{PV(LH)}$ in the A-to-B direction are not specified. Skew on these paths is dependent on the V_{TT} and R_T values on the backplane.

Test Circuits and Timing Waveforms

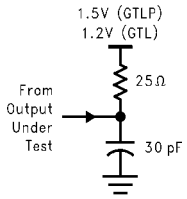
Test Circuit for A Outputs



Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

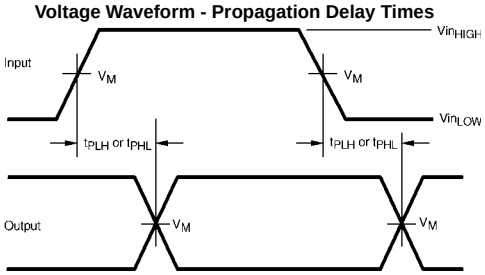
Note A: C_L includes probes and Jig capacitance.

Test Circuit for B Outputs

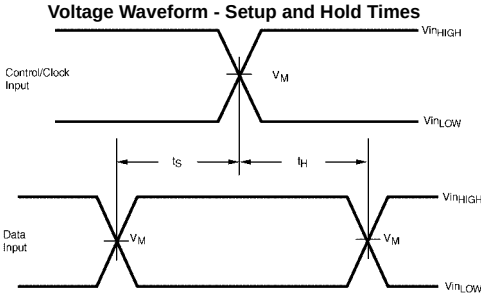


Note B: For B Port, C_L = 30 pF is used for worst case.

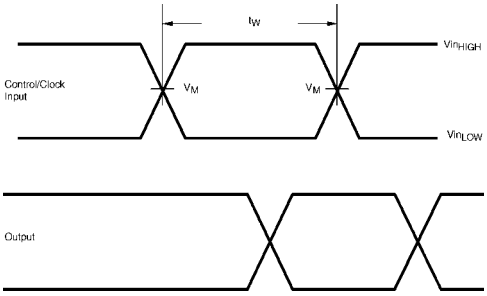
Voltage Waveform - Propagation Delay Times



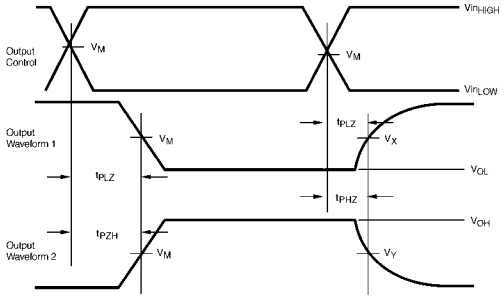
Voltage Waveform - Setup and Hold Times



Voltage Waveform - Pulse Width



Voltage Waveform - Enable and Disable times



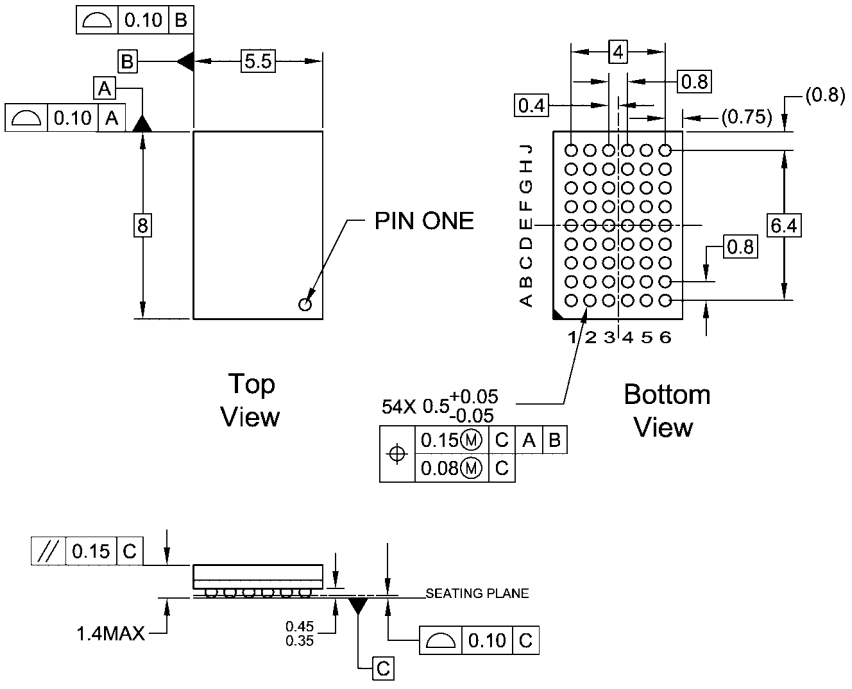
Output Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the control output.
Output Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the control output.

Input and Measure Conditions

	A or LVTTL Pins	B or GTLP Pins
V_{inHIGH}	3.0	1.5
V_{inLOW}	0.0	0.0
V_M	1.5	1.0
V_X	V_{OL} + 0.3V	N/A
V_Y	V_{OH} − 0.3V	N/A

All input pulses have the following characteristics: Frequency = 10MHz, $t_{RISE} = t_{FALL}$ = 2 ns (10% to 90%), Z_O = 50Ω.
The outputs are measured one at a time with one transition per measurement.

Physical Dimensions inches (millimeters) unless otherwise noted



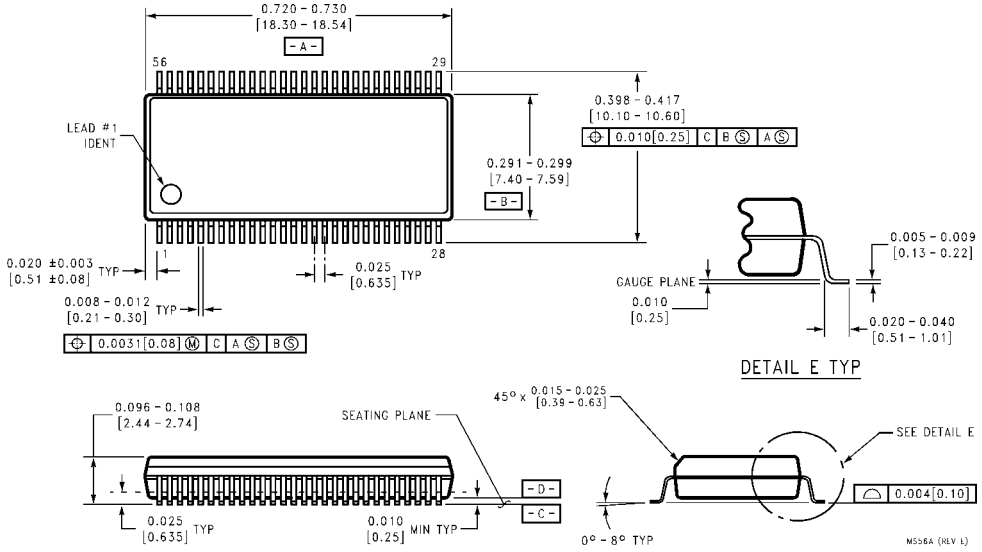
NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

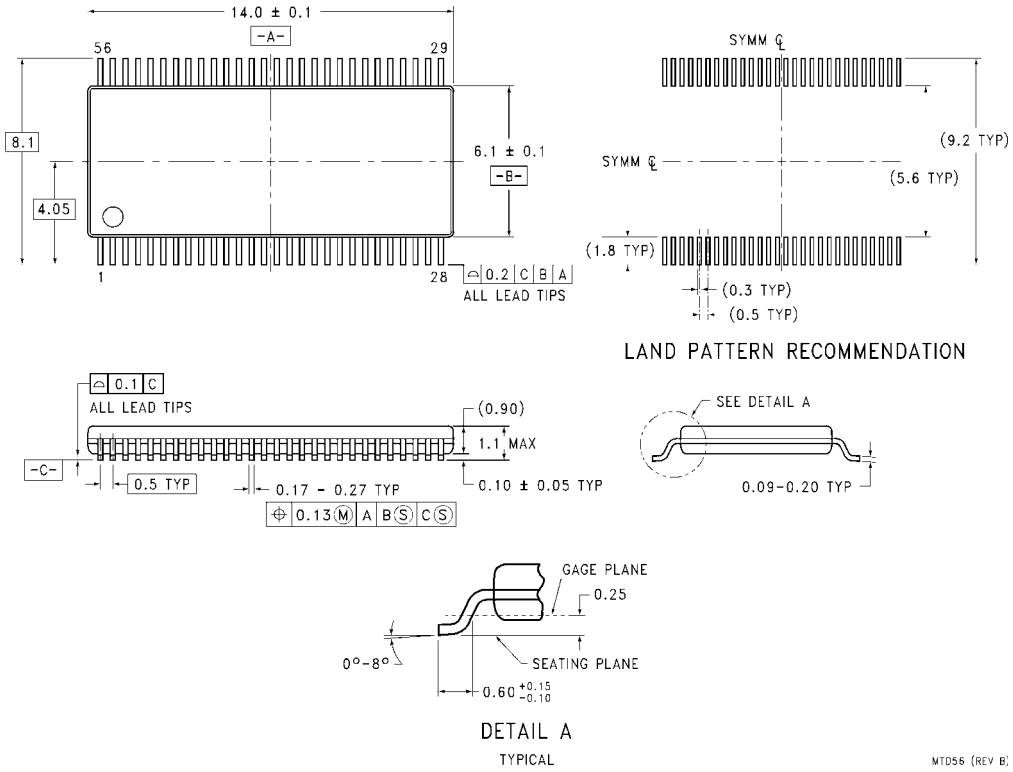
54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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