

74ALVC16601

Low Voltage 18-Bit Universal Bus Transceivers with 3.6V Tolerant Inputs and Outputs

General Description

The ALVC16601 is an 18-bit universal bus transceiver which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (CLKENAB and CLKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH-to-LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. When \overline{OEAB} is LOW, the outputs are active. When \overline{OEAB} is HIGH, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses \overline{OEBA} , LEBA, CLKBA and CLKENBA.

The ALVC16601 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The ALVC16601 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD} (A to B, B to A)
 - 3.4 ns max for 3.0V to 3.6V V_{CC}
 - 4.0 ns max for 2.3V to 2.7V V_{CC}
 - 7.0 ns max for 1.65V 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
 - Human body model > 2000V
 - Machine model >200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

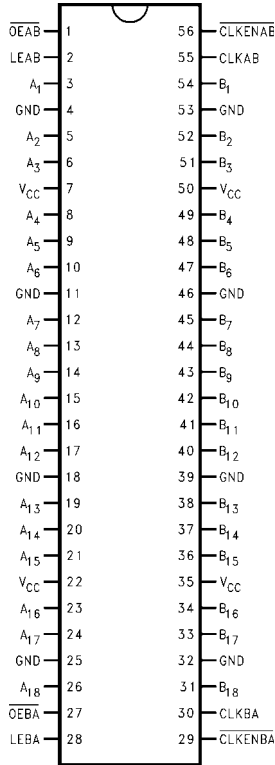
Order Number	Package Number	Package Description
74ALVC16601GX (Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74ALVC16601MTD (Note 3)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: BGA package available in Tape and Reel only.

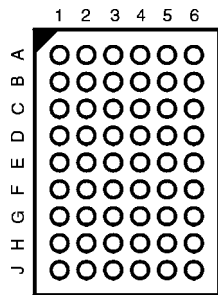
Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignment for TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OEAB} , \overline{OEBA}	Output Enable Inputs (Active LOW)
LEAB, LEBA	Latch Enable Inputs
CLKAB, CLKBA	Clock Inputs
$\overline{CLKENAB}$, $\overline{CLKENBA}$	Clock Enable Inputs
A ₁ -A ₁₈	Side A Inputs or 3-STATE Outputs
B ₁ -B ₁₈	Side B Inputs or 3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	A ₂	A ₁	\overline{OEAB}	$\overline{CLKENAB}$	B ₁	B ₂
B	A ₄	A ₃	LEAB	CLKAB	B ₃	B ₄
C	A ₆	A ₅	V _{CC}	V _{CC}	B ₅	B ₆
D	A ₈	A ₇	GND	GND	B ₇	B ₈
E	A ₁₀	A ₉	GND	GND	B ₉	B ₁₀
F	A ₁₂	A ₁₁	GND	GND	B ₁₁	B ₁₂
G	A ₁₄	A ₁₃	V _{CC}	V _{CC}	B ₁₃	B ₁₄
H	A ₁₆	A ₁₅	\overline{OEBA}	CLKBA	B ₁₅	B ₁₆
J	A ₁₇	A ₁₈	LEBA	$\overline{CLKENBA}$	B ₁₈	B ₁₇

Truth Table

(Note 4)

Inputs					Outputs
$\overline{CLKENAB}$	\overline{OEAB}	LEAB	CLKAB	A _n	B _n
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ (Note 5)
H	L	L	X	X	B ₀ (Note 5)
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ (Note 5)
L	L	L	H	X	B ₀ (Note 6)

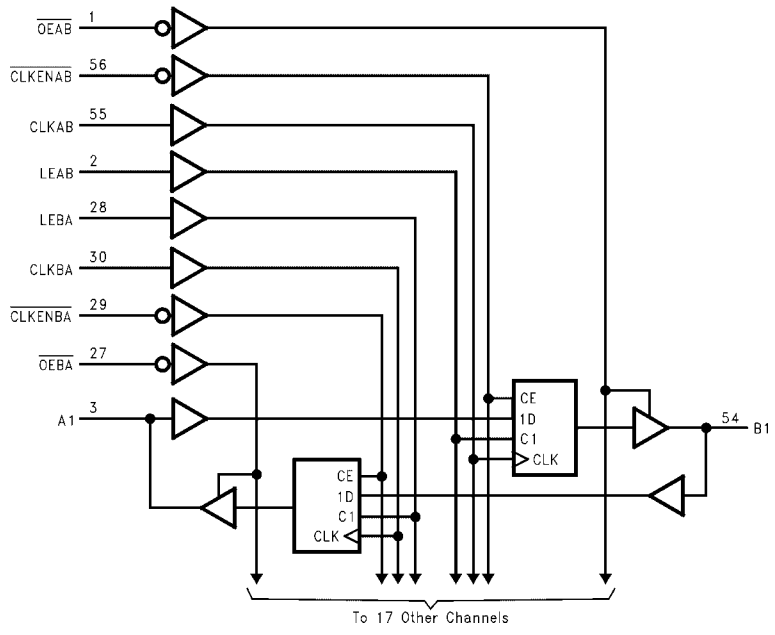
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance

Note 4: A-to-B data flow is shown; B-to-A flow is similar but uses \overline{OEBA} , LEBA, CLKBA, and $\overline{CLKENBA}$.

Note 5: Output level before the indicated steady-state input conditions were established.

Note 6: Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

Logic Diagram



Absolute Maximum Ratings (Note 7)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to 4.6V
Output Voltage (V_O) (Note 8)	-0.5V to V_{CC} + 0.5V
DC Input Diode Current (I_{IK})	
$V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 9)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 7: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 8: I_O Absolute Maximum Rating must be observed.

Note 9: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V
V_{IL}	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -6 \text{ mA}$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	1.65 - 3.6 1.65 2.3 2.7 3.0 3.0	$V_{CC} - 0.2$ 1.2 2 1.7 2.2 2.4		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 6 \text{ mA}$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	1.65 - 3.6 1.65 2.3 2.3 2.7 3		0.2 0.45 0.4 0.7 0.4 0.55	V
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		± 10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	μA

AC Electrical Characteristics										
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω								Units
		C _L = 50 pF				C _L = 30 pF				
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	250		200		200		100		ns
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus	1.3	3.4	1.5	4.0	1.0	3.5	1.5	7.0	ns
t _{PHL} , t _{PLH}	Propagation Delay CLK to Bus	1.3	4.0	1.5	4.9	1.0	4.4	1.5	8.8	ns
t _{PHL} , t _{PLH}	Propagation Delay LE to Bus	1.3	4.0	1.5	4.9	1.0	4.4	1.5	8.8	ns
t _{PZL} , t _{PZH}	Output Enable Time	1.3	4.3	1.5	5.4	1.0	4.9	1.5	9.8	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	1.3	4.2	1.5	4.7	1.0	4.2	1.5	7.6	ns
t _W	Pulse Width	1.5		1.5		1.5		4.0		ns
t _S	Setup Time	1.5		1.5		1.5		2.5		ns
t _H	Hold Time	1.0		1.0		1.0		1.0		ns
Capacitance										
Symbol	Parameter		Conditions		T _A = +25°C		Units			
					V _{CC}	Typical				
C _{IN}	Input Capacitance		V _I = 0V or V _{CC}		3.3	6	pF			
C _{OUT}	Output Capacitance		V _I = 0V or V _{CC}		3.3	7	pF			
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C _L = 50 pF		3.3	20	pF			
					2.5	20				

AC Loading and Waveforms

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_L
t_{PZH} , t_{PHZ}	GND

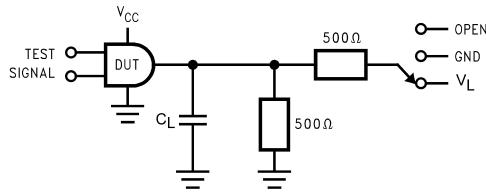


FIGURE 1. AC Test Circuit

TABLE 2. Variable Matrix
(Input Characteristics: $f = 1\text{MHz}$; $t_r = t_f = 2\text{ns}$; $Z_0 = 50\Omega$)

Symbol	V_{CC}			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
V_Y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
V_L	6V	6V	$V_{CC} \times 2$	$V_{CC} \times 2$

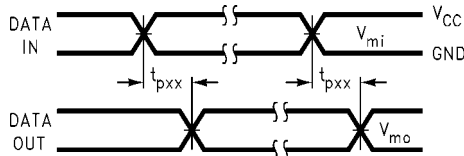


FIGURE 2. Waveform for Inverting and Non-inverting Functions

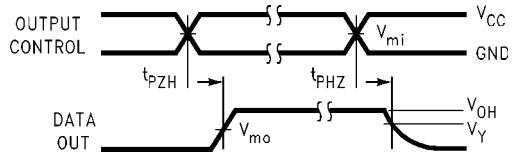


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

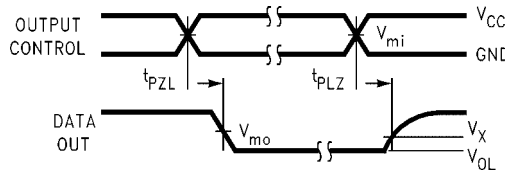


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

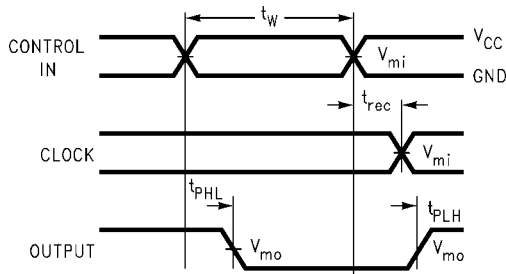


FIGURE 5. Propagation Delay, Pulse Width and t_{rec} Waveforms

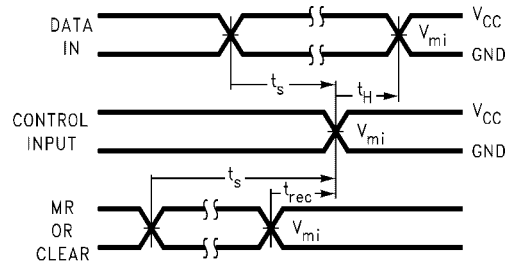
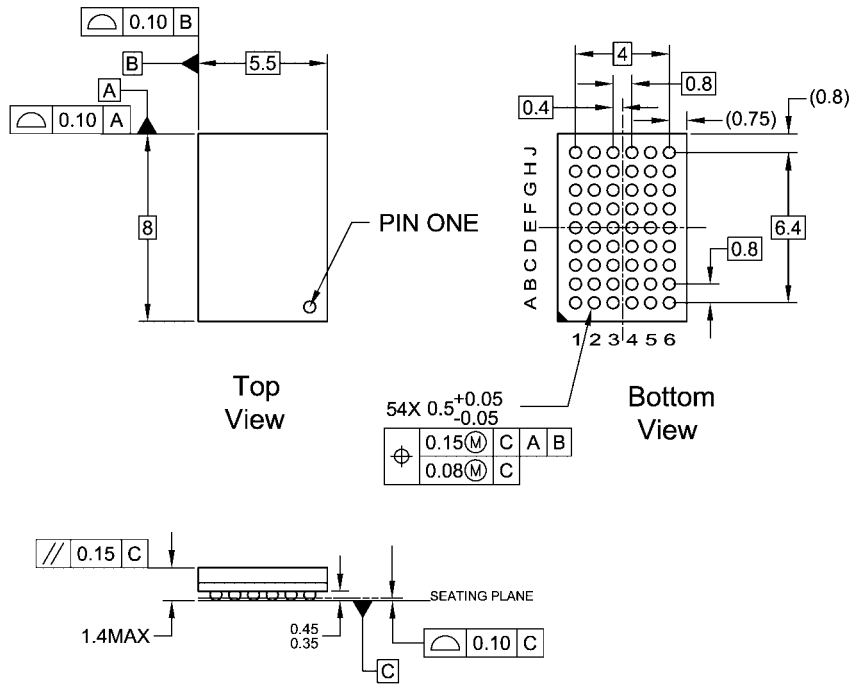


FIGURE 6. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Physical Dimensions inches (millimeters) unless otherwise noted

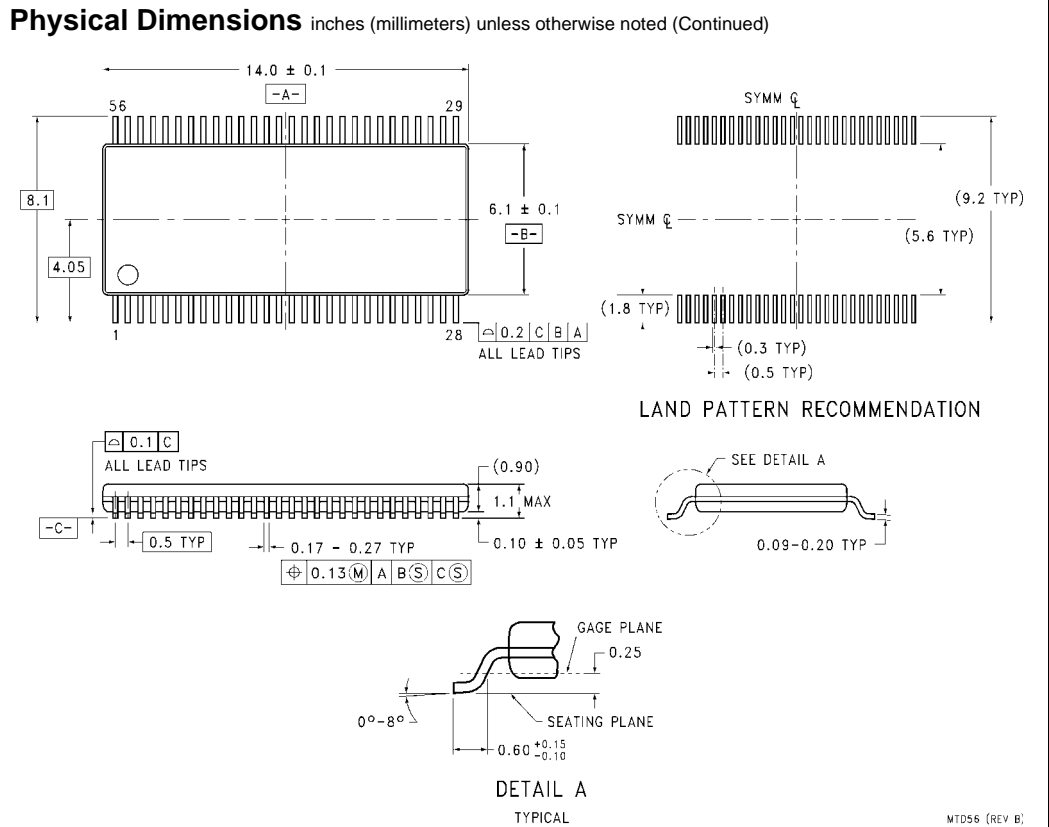


NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
Package Number BGA54A
(Preliminary)**



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

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