HD-6406

CMOS Programmable Asynchronous Communication Interface

REFERENCE PAGE 5-54 FOR APPLICATION NOTE 108

Features

- Single Chip UART/BRG
- DC to 16MHz Operation
- Crystal or External Clock Input
- On Chip Baud Rate Generator
  - ▸ 72 Selectable Baud Rates
- DMA or Vectored Interrupt Mode
- Maskable Interrupts
- Microprocessor Bus Oriented Interface
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Power — 1mA/MHz Typical
- Complete Modem Interface
- Line Break Generation and Detection
- Loopback and Echo Modes

Description

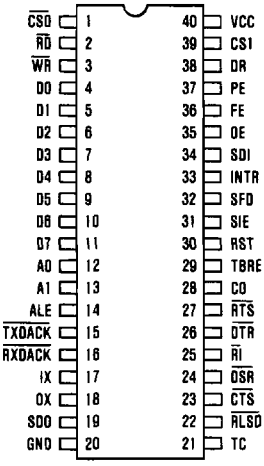
The HD-6406 (PACI) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing Harris Semiconductor's advanced Scaled SAJI IV CMOS process, the PACI will support data rates from DC to 1Mbaud (0-16MHz clock). In addition to all standard UART functions, the PACI includes a complete Data Communications Equipment (DCE) interface.

Provision is made for DMA control of the PACI so that operation at the higher data rates is not hindered by slow microprocessor response times. An ALE control input permits direct interfacing to multiplexed data/address buses common to many microprocessors.

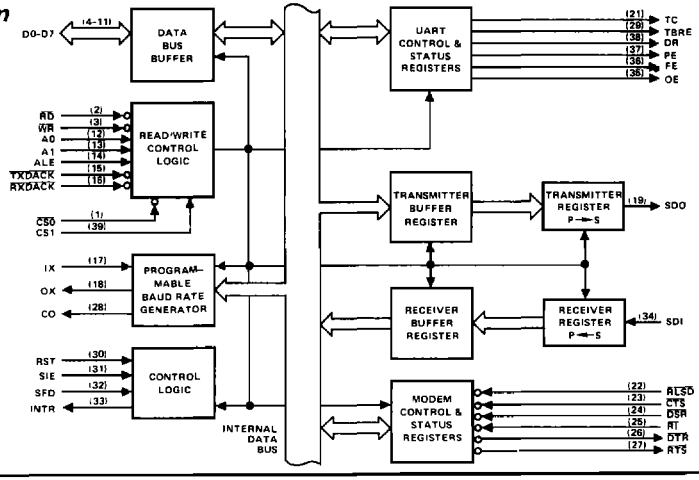
The interrupt structure of the PACI is user-programmable and can be configured to provide a single interrupt for any status change. A subsequent read of an internal status register will identify the source of the interrupt. If desired, the PACI can also provide separate hardware interrupt outputs for the receiver, transmitter and modem status changes. Separate error condition outputs can be used to pinpoint the exact cause of any detected error condition.

Pinout

TOP VIEW



Block Diagram



CAUTION. Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

PIN NUMBER	TYPE	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1, 39	I	$\overline{CS0}$, CS1	Low, High	CHIP SELECTS. The chip select inputs act as enable signals for the $\overline{RD}$ and $\overline{WR}$ input signals during all non-DMA bus operations.
2	I	$\overline{RD}$	Low	READ. The $\overline{RD}$ input causes data to be output to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0, A1) during non-DMA operations. During DMA read operations ($\overline{RXDACK}$ true) the address inputs are ignored and the contents of the Receiver Buffer Register is output providing the DR bit in the Modem Status Register (MSR) is true.
3	I	$\overline{WR}$	Low	WRITE: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the PACI. Addressing and chip select action is the same as for read operations with the exception that $\overline{TXDACK}$ provides the select qualifier for DMA write operations providing the TBRE bit in the MSR is true
4-11	I/O	D0-D7	High	DATA BITS 0-7. The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the PACI and the CPU. For character formats of less than 8 bits, the corresponding D7, D6 and D5 are considered 'don't cares' for data writes and are 0 for data reads. These lines are normally at their high impedance state except during read operations. D0 is the LSB and is the first serial data bit received or transmitted.
12, 13	I	A0, A1	High	ADDRESS 0, 1: The address lines select the various internal registers during CPU bus operations. Qualified DMA operations ignore the address inputs and access the appropriate receive or transmit buffer register.
14	I	ALE	High	ADDRESS LATCH ENABLE: ALE true enables the internal transparent address latches for the A0, A1 inputs. The address is latched when ALE goes false (low).
15	I	$\overline{TXDACK}$	Low	TRANSMIT DMA ACKNOWLEDGE: A true $\overline{TXDACK}$ notifies the PACI that a transmit DMA cycle has been granted. It acts as a chip select which enables the $\overline{WR}$ input to access the Transmitter Buffer Register when the TBRE bit is in the USR is true
16	I	$\overline{RXDACK}$	Low	RECEIVE DMA ACKNOWLEDGE: A true $\overline{RXDACK}$ notifies the PACI that a receive DMA cycle has been granted. It acts as a chip select which enables the $\overline{RD}$ input to access the Receive Buffer Register when the DR bit in the USR is true
17, 18	I, O	IX, OX		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open
19	O	SDO	High	SERIAL DATA OUTPUT. Serial data output from the PACI transmitter circuitry. A Mark (1) is high and a Space (0) is low. SD0 is held in the Mark condition when the transmitter is disabled with $\overline{CTS}$ false, RST true, when the Transmitter Register is empty, or when in the Loop Mode
20		GND	Low	GROUND. Power supply ground connection.
21	O	TC	High	TRANSMISSION COMPLETE: TC goes true when a complete character, including stop bits, has been transmitted and TBRE is true. TC is reset with a data write to TBR. RST will set TC true.
22	I	$\overline{RLSD}$	Low	RECEIVE LINE SIGNAL DETECT: The logical state of this input is reflected in the $\overline{RLSD}$ bit of the Modem Status Register. Any change of state will cause an interrupt on INTR if INTEN and MIEN are true.
23	I	$\overline{CTS}$	Low	CLEAR TO SEND: The logical state of the $\overline{CTS}$ line is reflected in the CTS bit of the Modem Status Register. Any change of state of $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SD0 in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect the Loop mode of operation.
24	I	$\overline{DSR}$	Low	DATA SET READY. The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of DSR will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the PACI.

Pin Description

PIN NUMBER	TYPE	SYMBOL	ACTIVE LEVEL	DESCRIPTION
25	I	$\overline{RI}$	Low	RING INDICATOR. The logical state of the $\overline{RI}$ line is reflected inn the Modem Status Register. Any change of state of $\overline{RI}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the PACI.
26	O	$\overline{DTR}$	Low	DATA TERMINAL READY. The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 to the same bit in the MCR or whenever a RST (high) is applied to the PACI.
27	O	$\overline{RTS}$	Low	REQUEST TO SEND: The $\overline{RTS}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the same bit in the MCR or whenever a RST (high) is applied to the PACI.
28	O	CO		CLOCK OUT. This output is user programmable to provide either buffered IX output or a buffered Baud Rate Generator (16X) clock output. The buffered IX (Crystal or external clock source) output is provided when the BRSR bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate.
29	O	TBRE	High	TRAMSMITTER BUFFER REGISTER EMPTY. The TBRE output is set (high) whenever the Tranmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a RST to the PACI will also set the TBRE output. TBRE is cleared (low) whenever data is written to the TBR.
30	I	RST	High	RESET: The RST input forces the PACI into an "Idle" mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits which are set. The PACI remains in an "Idle' state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.
31	I	SIE	High	SINGLE INTERRUPT ENABLE. A true (high) level on the SIE input enables interrupts caused by the DR and TBRE status bits. This enables the user to utilize a single hardware interrupt signal (INTR) for any status change within the PACI.
32	I	SFD	High	STATUS FLAGS DISABLE: Holding the SFD input true (high) prevents the true state of the USR bits PE, OE, FE and TC from causing an interrupt. This control input, like the SIE input, enables the user to define what status changes will effect the INTR output.
33	O	INTR	High	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit and the SIE and SFD control inputs selectively enable various status changes to provide an input to the INTR logic. Figure 9 shows an overall view of the relationship of these interrupt control signals.
34	I	SDI	High	SERIAL DATA INPUT: Serial data input to the PACI receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode when RST is true or when the Receiver Enable (REN) bit in the MCR register is false.
35	O	OE	High	OVERRUN ERROR. A true level on the OE output indicates that the Receiver Buffer Register (RBR) was full when a character was received. Transfer to the RBR will not occur. OE is updated each time a character is transferred to the RBR. RST high will set OE low.
36	O	FE	High	FRAMING ERROR: A true level on the FE output indicates that there were invalid stop bits in the last received character. The FE output is updated each time a character is transferred to the RBR. RST high will reset FE.
37	O	PE	High	PARITY ERROR: PE is set true whenever the parity of a received character does not match the programmed parity. The PE output is updated each time a character is transferred to the RBR. PE is reset whenever RST is true or when no parity check is programmed.
38	O	DR	High	DATA READY: A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data read of the RBR or when RST is true.
40		VCC	High	VCC: +5 Volt positive power supply pin. A 0.1μF decoupling capacitor from VCC (pin 40) to GND (pin 20) is recommended.

Functional Description

RESET

During and after power-up, the PACI should be given a **RST high for at least two IX clock cycles** in order to initialize and drive the PACI's circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal BRG circuits, clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected.
- Clears the UART Status Register (USR) except for TC and TBRE which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST low), the PACI remains in the idle mode until programmed to its desired system configuration.

PROGRAMMING THE HD-6406 PACI

The complete functional definition of the PACI is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the PACI to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate etc. Once programmed, the PACI is ready to perform its communication functions.

The control registers can be written to in any order, however the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the PACI is programmed and operational these registers can be updated any time that the PACI is not immediately transmitting or receiving data.

Table 1 shows the required control signals to access the PACI's internal registers.

ALE	$\overline{CS0}$	CS1	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
1 or ↓	0	1	0	0	↓	1	Data bus → TBR
1 or ↓	0	1	0	0	1	↓	RBR → Data bus
1 or ↓	0	1	0	1	↓	1	Data bus → UCR
1 or ↓	0	1	0	1	1	↓	USR → Data bus
1 or ↓	0	1	1	0	↓	1	Data bus → MCR
1 or ↓	0	1	1	0	1	↓	MCR → Data bus
1 or ↓	0	1	1	1	↓	1	Data bus → BRSR
1 or ↓	0	1	1	1	1	↓	MSR → Data bus

TABLE 1.

The Address Latch Enable (ALE) input acts as an address latch control signal during these operations. If ALE is left high, the address inputs A0, A1 must be held true during the entire bus operation (demultiplexed bus operation). For multiplexed bus applications the address inputs A0, A1 are latched when ALE goes low. In this case A0 and A1 are not required to be held true for the entire bus cycle.

DMA control of the PACI is discussed in a later section of this data sheet and involves reading and writing of the Receiver and Transmitter Buffer Registers (RBR and TBR).

The following descriptions discuss the control registers in detail.

UART CONTROL REGISTER (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a zero in order to insure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

UCR

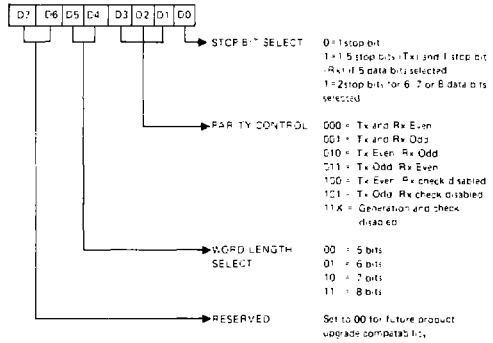


FIGURE 1.

BAUD RATE SELECT REGISTER (BRSR)

The PACI is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select which divide ratio (one of 72) the internal Baud Rate Generator circuitry will use. The internal circuitry is seperated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4, or ÷5. This Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432MHz, 2.4576MHz or 3.072MHz and a Prescaler of ÷3, ÷4 or ÷5 respectively, the Prescaler output will provide a constant 614.400Hz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 to 38.4Kbaud can be selected (see Table 2). Non-standard baud rates up to 1Mbaud can be selected by using different input frequencies (up to 16MHz) and/or different Prescaler and Divisor Select ratios. The baud rate generator provides a clock which is 16 times the desired

baud rate. For example, in order to operate at a 1Mbaud data rate a 16MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of "external" would be used to provide a 16MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver Circuits.

The C0 select bit in the BRSR selects whether a buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16X baud rate clock) will be output on the C0 output (pin 28). The Baud Rate Generator output will always be a 50% nominal duty cycle except when "external" is selected and the Prescaler is set to ÷3 or ÷5.

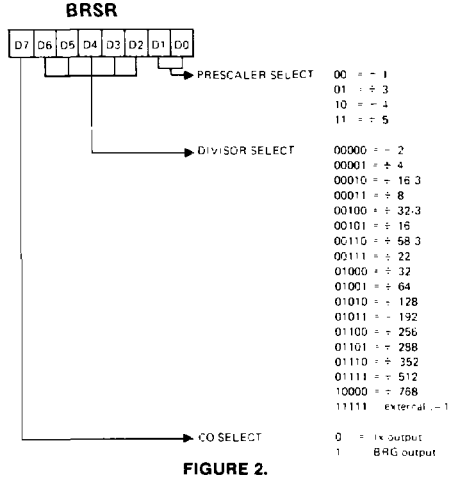


FIGURE 2.

BAUD RATE	DIVISOR
38.4K	External
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000*	58/3
1800*	21
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

TABLE 2.

Note These baud rates are based upon the following input frequency-/prescale divisor combinations.
1.8432MHz and Prescale = ÷3
2.4576MHz and Prescale = ÷4
3.072MHz and Prescale = ÷5
* All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%
1800	1828.57	1.56%

MODEM CONTROL REGISTER

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low). The Operating Mode bits configure the PACI into one of four possible modes. "Normal" configures the PACI for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a re-synchronized output (see Figure 4). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state. Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{RI}$, $\overline{RLSD}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D7 must always be written to with a logic zero to insure correct PACI operation.

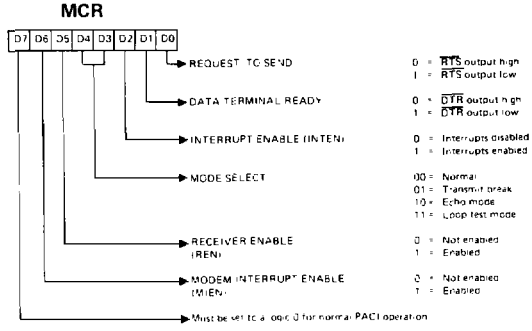


FIGURE 3.

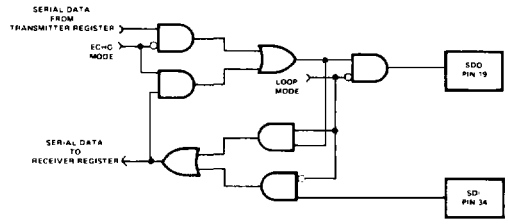


FIGURE 4. LOOP AND ECHO MODE FUNCTIONALITY

UART STATUS REGISTER (USR)

The USR provides a single register that the controlling system can examine to ascertain if errors have occurred or if other status changes in the PACI require the system's attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the PACI. **Reading the USR clears all of the status bits in the USR but does not affect associated output pins.** Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that last character received contained improper stop bits. This could be caused by the total absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed parity of the receiver and the calculated parity of the received characters data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the Modem input lines ($\overline{RI}$, $\overline{RLSD}$, $\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these four signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the PACI has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the SFD (pin 32) input is low and the INTEN bit in the MCR register is true.

USR

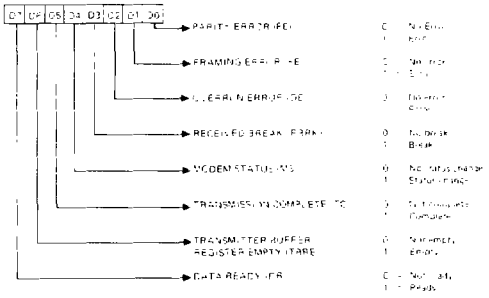


FIGURE 5

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character. Assertion of this bit will cause an interrupt if the SIE (pin 31) input is high and the INTEN bit in the MCR is enabled.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character and that the CPU may access this data. An interrupt will be generated (INTR) if SIE input is high and the INTEN bit is enabled.

MODEM STATUS REGISTER (MSR)

The MSR provides a means whereby the CPU can read the modem signal inputs by accessing the data bus interface of the PACI. **Like all of the register images of external pins in the PACI, true logic levels are represented by a high (1) signal level.** By following this consistent definition the system software need not be concerned with whether external signals are high or low true. In particular the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state of any of the modem input signals will set the Modem Status (MS) bit in the USR register. When this happens an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Ring Indicator ($\overline{RI}$) input indicates to the PACI that the modem is receiving a ringing signal.

The Receive Line Signal Detect ($\overline{RLSD}$) input is used to notify the PACI that the signal quality received by the modem is within acceptable limits.

The Data Set Ready ($\overline{DSR}$) input is a status indicator from the modem to the PACI which indicates that the modem is ready to provide received data to the PACI receiver circuitry.

Clear to Send ($\overline{CTS}$) is both a status and control signal from the modem that tells the PACI that the modem is ready to receive transmit data from the PACI transmitter output (SDO). A high (false) level on this input will inhibit the PACI from beginning transmission and if asserted in the middle of a transmission will only permit the PACI to finish transmission of the current character.

MSR

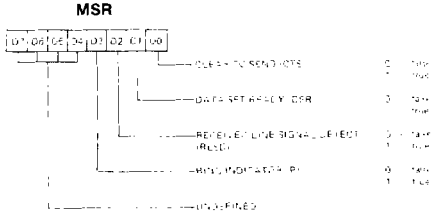
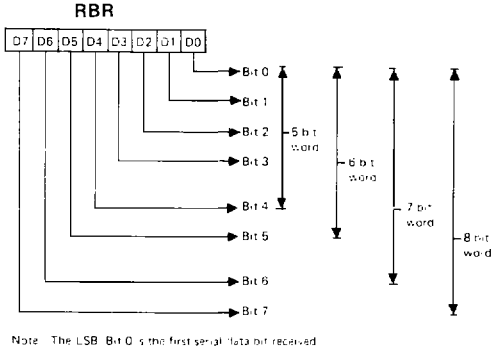


FIGURE 6

RECEIVER BUFFER REGISTER (RBR)

The receiver circuitry in the PACI is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the LSB (D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to 0 by the PACI. Received data at the SDI input pin is shifted into the Receiver Register by an internal 1X clock

which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data. While the Receiver Register is shifting a new character into the PACI, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.

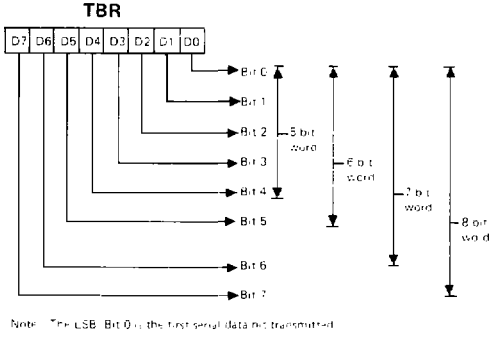


Note: The LSB, Bit 0, is the first serial data bit received.

FIGURE 7.

TRANSMITTER BUFFER REGISTER (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the microprocessor data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter. Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC output pin and flag (USR register) indicates when both the TBR and TR are empty.



Note: The LSB, Bit 0, is the first serial data bit transmitted.

FIGURE 8.

PACI INTERRUPT STRUCTURE

The PACI has provision for both software and hardware masking of interrupts generated for the INTR output pin. The two input pins, SIE and SFD, provide the mask control for the receiver and transmitter status interrupts. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall PACI interrupts respectively. Figure 9 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{RLSD}$, $\overline{RI}$, $\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. **Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits.** The output pins associated with these status bits are not affected by reading the USR register.

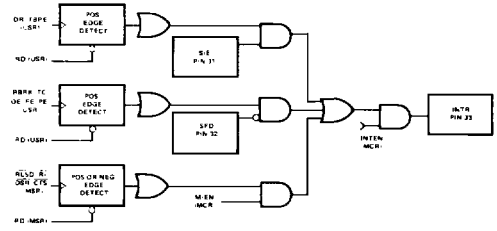


FIGURE 9.

DMA CONTROL OF THE PACI

Because of the high data rates possible with the PACI, provision for DMA control of the transmitter and receiver buffer registers has been included in the design. The $\overline{RXDACK}$ and $\overline{TXDACK}$ inputs in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs are driven by the system DMA controller to access the RBR and TBR registers respectively.

Reading of the RBR via the $\overline{RXDACK}$ control signal requires that the DR bit in the USR is set (high) and that the $\overline{RD}$ input be driven low. When these conditions are

met the address logic overrides the address inputs (A0, A1) and forces a read of the RBR. Similarly, a DMA write to the TBR requires that the TBRE bit in the USR register is set (high) and that $\overline{TXDACK}$ and $\overline{WR}$ are asserted by the DMA controller. Once again the address logic overrides the address inputs and forces a write to the TBR register.

The $\overline{CS0}$ and CS1 inputs would normally be in their inactive state during DMA accesses. The A0, A1, and ALE inputs are overridden during DMA operations and as such their logical state is a don't care.

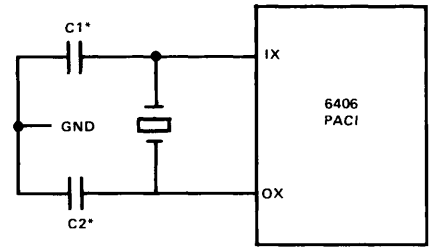
CRYSTAL OPERATIONS

The PACI crystal oscillator circuitry is designed to operate with a fundamental, parallel resonent crystal. This circuit is the same as used in the Harris 82C84A clock generator/driver and as such the general applications information contained in Tech Brief TB-47 that applies to the oscillator operation will be pertinent to the PACI. To summarize Table 3 and Figure 10 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source the Ix input is driven and the Ox output is left open. Power consumption when using an external clock is typically 2 times lower than when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	1.0 to 16MHz
Type of Operation	Parallel resonent, Fund. mode
Load Capacitance (CL)	20 or 32 pf. (typ.)
R_{series}(Max.)	100 ohms (f=16 MHz, CL = 32pf.) 200 ohms (f=16 MHz, CL = 20pf.)

TABLE 3.



* C1 = C2 ≈ 20pf for CL = 20pf.
C1 = C2 ≈ 47pf for CL = 32pf.

FIGURE 10.

REGISTER BIT ASSIGNMENT SUMMARY

REGISTER NAME	MNEMONIC	BIT ASSIGNMENT							
		LSB 0	1	2	3	4	5	6	MSB 7
Receiver Buffer	RBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Transmitter Buffer	TBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
UART Status	USR	Parity Error (PE)	Framing Error (FE)	Overrun Error (OE)	Received Break (RBRK)	Modem Status (MS)	Transmission Complete (TC)	Transmitter Buffer Reg. empty (TBRE)	Data Ready (DR)
UART Control	UCR	Stop Bit Select	Parity Control 0	Parity Control 1	Parity Control 2	Word Length 0	Word Length 1	Reserved*	Reserved *
Modem Control	MCR	Request To Send (RTS)	Data Terminal Ready (DTR)	Interrupt Enable (INTEN)	Mode Select 0	Mode Select 1	Receiver Enable (REN)	Modem Interrupt enable (MIEN)	0
Modem Status	MSR	Clear to Send (CTS)	Data Set Ready (DSR)	Received Line Signal Detect (RLSD)	Ring Indicator (RI)	Not Used	Not Used	Not Used	Not Used
Bit Rate Select	BRSR	Prescaler Select 0	Prescaler Select 1	Divisor Select 0	Divisor Select 1	Divisor Select 2	Divisor Select 3	Divisor Select 4	Co Select

* *Reserved for future use. Always set to zero (0) to maintain future software compatibility.*

Absolute Maximum Ratings

Supply Voltage ..... +8.0 Volts
Input, Output or I/O Voltage Applied ..... GND -0.5V to VCC +0.5V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 16°C/W (CERDIP Package)
21°C/W (LCC Package)
θ_{ja} ..... 43°C/W (CERDIP Package)
48°C/W (LCC Package)
Gate Count ..... 1500 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range
HD-6406-5 ..... 0°C to +70°C
HD-6406-9 ..... -40°C to +85°C
HD-6406-2/-8 ..... -55°C to +125°C

D. C. Specifications

VCC = 5.0V ±10%; T_A = 0°C to +70°C (6406-5);
T_A = -40°C to +85°C (6406-9);
T_A = -55°C to +125°C (6406-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V	HD-6406-5/-9 HD-6406-2/-8
VIL	Logical Zero Input Voltage		0.8	V	
VTH	Schmidt Trigger Logical One Input Voltage	VCC -0.5		V	Reset Input
VTL	Schmidt Trigger Logical Zero Input Voltage		GND +0.5	V	Reset Input
VIH (CLK)	Logical One Clock Voltage	VCC -0.5		V	
VIL (CLK)	Logical Zero Clock Voltage		GND +0.5	V	External Clock
VOH	Output High Voltage	3.0 VCC -0.4		V	IOH = +2.5mA IOH = -400μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	LA	VIN = GND or VCC, DIP Pins 1, 2, 3, 12-16, 22-25, 30, 31, 32, 34-39
IO	Input/Output Leakage Current	-10.0	+10.0	LA	VO = GND or VCC, DIP Pins 4-11
ICCOP*	Operating Power Supply Current		3	mA	External Clock F = 2.4576 MHz, VCC = 5.5V, VIN = VCC or GND, Outputs Open

*Guaranteed and sampled, but not 100% tested. ICCOP is typically ≤ 1mA/MHz

Capacitance $T_A = 25^oC$

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN*	Input Capacitance	10	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT*	Output Capacitance	15	pF	
CI/O*	I/O Capacitance	20	pF	

*Guaranteed and sampled, but not 100% tested.

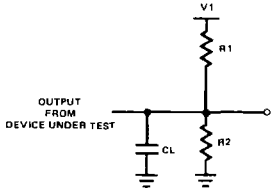
A.C. Specifications

VCC = +5V ±10%, GND = 0V: $T_A = 0^oC$ to $+70^oC$ (HD-6406-5)
$T_A = -40^oC$ to $+85^oC$ (HD-6406-9)
$T_A = -55^oC$ to $+125^oC$ (HD-6406-2/-8)

TIMING REQUIREMENTS & RESPONSES

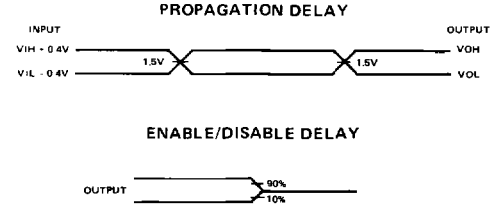
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TLHLL	ALE Pulse Width	50		ns	
(2) TAVLL	Address Setup	20		ns	
(3) TLLAX	Address Hold	20		ns	
(4) TSVCTL	Select Setup to Control Leading Edge	30		ns	
(5) TCTHSX	Select Hold from Control Trailing Edge	50		ns	
(6) TCTLCTH	Control Pulse Width	150		ns	Control Consists of RD or WR
(7) TCTHCTL	Control Disable to Control Enable	190		ns	
(8) TRLDV	Read Low to Data Valid		120	ns	1
(9) TRHDZ	Read Disable	0	60	ns	2
(10) TCTHLH	Control Inactive to ALE High	20		ns	
(11) TDVWH	Data Setup Time	50		ns	
(12) TWHDX	Data Hold Time	20		ns	
(13) FC	Clock Frequency	0	16	MHz	TCHCL + TCLCH Must Be ≥ 62.5ns
(14) TCHCL	Clock High Time	25		ns	
(15) TCLCH	Clock Low Time	25		ns	
(16) TR/TF	IX Input Rise/Fall Time (10%-90%) (External Clock)		tx	ns	tx ≤ 1/(6FC) or 50ns Whichever is Smaller
(17) TFCO	Clock Output Fall Time		15	ns	CL = 50pF
(18) TRCO	Clock Output Rise Time		15	ns	CL =50pF

A.C. Test Circuit



TEST CONDITION	V1	R1	R2	CL
1 Propagation Delay	1.7V	520	∞	100pF
2 Disable Delay	VCC	5K	5K	50pF

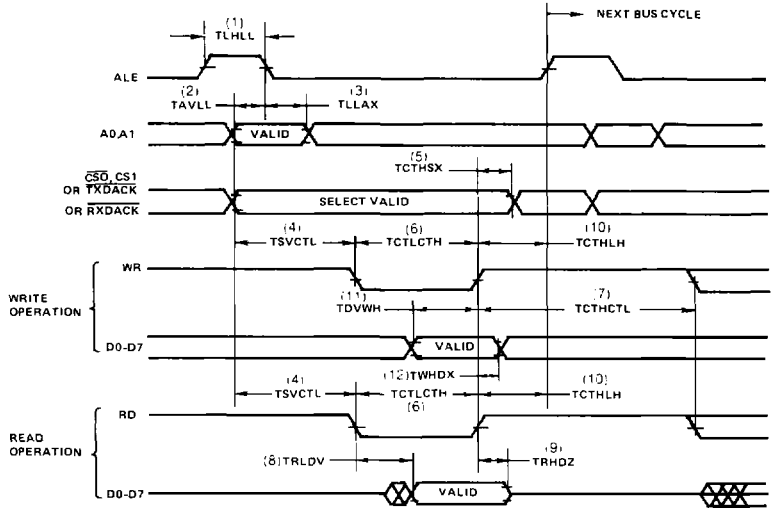
A.C. Testing Input, Output Waveform



A.C. Testing: All inputs signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1nsec per volt.

Timing Diagrams

MULTIPLEXED BUS OPERATION



DEMULTIPLEXED BUS OPERATION (ALE HIGH)