

100395 Low Power 9-Bit ECL-to-TTL Translator with Registers

General Description

The 100395 is a 9-bit translator for converting F100K logic levels to FAST® TTL logic levels. A high on the output enable (\overline{OE}) holds the TTL outputs in a high impedance state. Two separate clock inputs are available for multiplexing and system level testing.

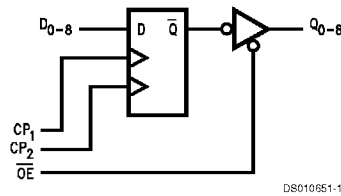
The 100395 is designed with FAST TTL 64 mA outputs for bus driving capability. All inputs have 50 k Ω pull down resistors. When the inputs are either unconnected or at the same potential, the outputs will go LOW.

Features

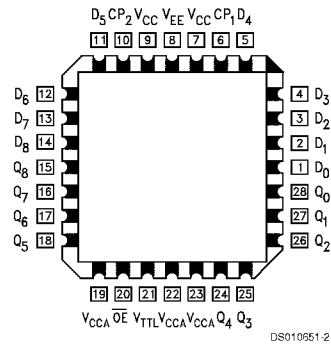
- 64 mA I_{OL} drive capability
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Registered outputs
- FAST TTL outputs

Ordering Code:

Logic Symbol

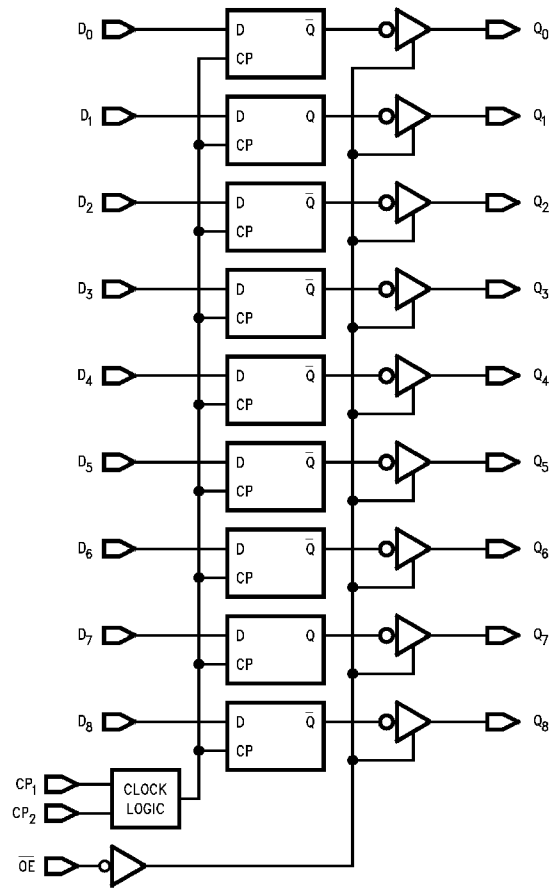


Connection Diagram



Pin Names	Description
D ₀ -D ₈	Data Inputs (ECL)
Q ₀ -Q ₈	Data Outputs (TTL)
\overline{OE}	Output Enable
CP ₁ , CP ₂	Clock Inputs

Logic Diagram



DS010551-3

Truth Table

Inputs				Outputs
CP ₁	CP ₂	\overline{OE}	D _N	Q _N
↗	L	L	L	L
L	↗	L	L	L
↗	L	L	H	H
L	↗	L	H	H
H	X	X	X	NC
X	H	X	X	NC
L	L	X	X	NC
X	X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance
 NC = No Change

Absolute Maximum Ratings (Note 1)

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	-0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
TTL Input Voltage	-0.5V to +7.0V
Output Current (DC Output HIGH)	+130 mA

ESD (Note 2)

≥ 2000V

Recommended Operating Conditions

Case Temperature (T_C)	0°C to +85°C
Supply Voltage	
V_{EE}	-5.7V to -4.2V
V_{TTL}	+4.5V to +5.5V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
						$I_{OH} = -15\text{ mA}$	$V_{IN} = V_{IH} (\text{Max})$ or $V_{IL} (\text{Min})$
V_{OH}	Output HIGH Voltage	2.4			V		
V_{OL}	Output LOW Voltage			0.55	V	$I_{OL} = 64\text{ mA}$	
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5			μA	$V_{IN} = V_{IL} (\text{Min})$	
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH} (\text{Max})$	
I_{OZL}	3-STATE Current Output High			-50	μA	$V_{OUT} = +0.4V$	
I_{OZH}	3-STATE Current Output Low			+50	μA	$V_{OUT} = +2.7V$	
I_{CEX}	Output High Leakage Current			250	μA	$V_{OUT} = V_{CC}$	
I_{OS}	Output Short-Circuit Current	-100		-225	mA		
I_{EE}	V_{EE} Power Supply Current	-67		-29	mA	Inputs Open	
I_{CCH}	V_{TTL} Power Supply Current High			29	mA		
I_{CCL}	V_{TTL} Power Supply Current Low			65	mA		
I_{CCZ}	V_{TTL} Power Supply Current 3-STATE			49	mA		

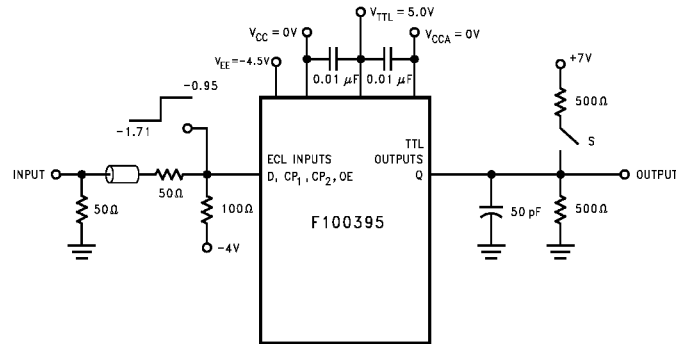
Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC, AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.30	5.00	2.30	5.00	2.30	5.00	ns	Figures 1, 2
t_{PHL}	Clock to Output	3.00	5.60	3.00	5.60	3.40	6.40		
t_{PZL}	Output Enable Time	3.20	7.60	3.20	7.60	3.20	7.60	ns	Figures 1, 3
t_{PZH}	$\overline{OE} \downarrow$ to Q_N	2.40	5.60	2.40	5.60	2.40	5.60		
t_{PLZ}	Output Disable Time	3.20	7.60	3.20	7.60	3.20	7.60	ns	Figures 1, 3
t_{PHZ}	$\overline{OE} \uparrow$ to Q_N	2.40	5.60	2.40	5.60	2.40	5.60		
t_H	Data to CP \overline{EN}	1.5		1.5		1.5		ns	Figures 1, 2
	Hold Time	1.5		1.5		1.5			
t_S	Data to CP \overline{EN}	0.5		0.5		0.5		ns	Figures 1, 2
	Setup Time	0.5		0.5		0.5			
$t_{pw(H)}$	Clock Pulse Width	2.0		2.0		2.0		ns	Figures 1, 2

Test Circuit



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Notes:

$V_{CC} = 0V$, $V_{CCA} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5V$.

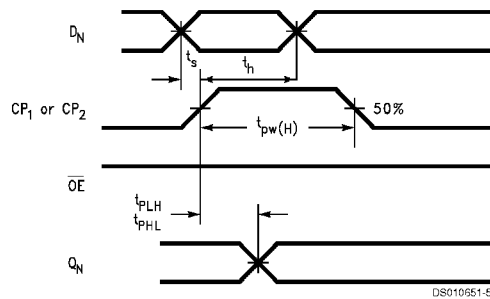
All unused outputs are loaded with 500Ω to GND. Decoupling capacitors are necessary in the test and end application environment. When V_{CC} and V_{CCA} are common to a single power plane, typically $0.0V$, decouple V_{TTL} to that plane with one $0.01 \mu F$ capacitor.

FIGURE 1. AC Test Circuit

Switch Positions for Parameter Testing

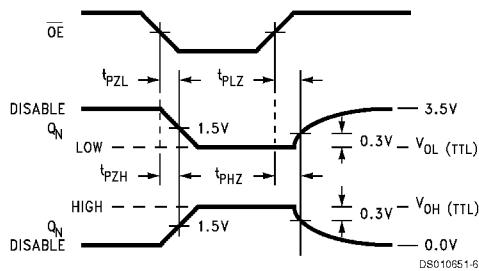
Parameter	S-Position
t_{PLH} , t_{PHL}	Open
t_{PHZ} , t_{PZH}	Open
t_{PLZ} , t_{PZL}	Closed

Switching Waveforms



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FIGURE 2. Propagation Delay and Transition Times

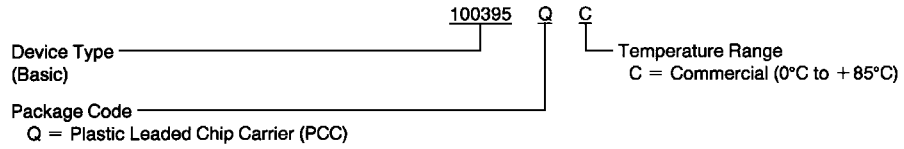


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FIGURE 3. Enable and Disable Waveforms, \overline{OE} to Q_N

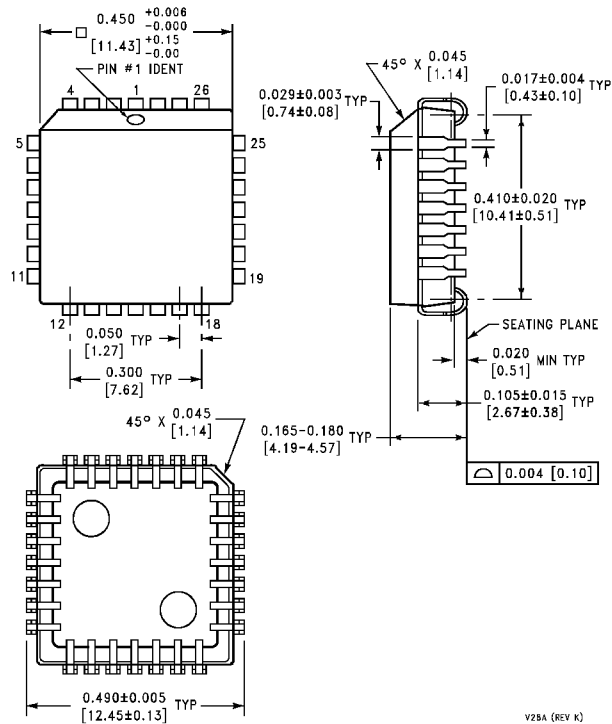
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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Physical Dimensions inches (millimeters) unless otherwise noted



V28A (REV K)

28-Lead Plastic Chip Carrier (Q)
Package Number V28A

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Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

www.fairchildsemi.com

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europa.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179