4104B

QUAD LOW VOLTAGE TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

DESCRIPTION – The 4104B Quad Low Voltage to High Voltage Translator with 3-State Outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage CMOS and TTL to high voltage CMOS. It has four Data Inputs (I_0-I_3), an active HIGH Output Enable input (EO), four Data Outputs (Z_0-Z_3) and their Complements ($\overline{Z}_0$-$\overline{Z}_3$). With the Output Enable input HIGH, the Outputs (Z_0-Z_3, $\overline{Z}_0$-$\overline{Z}_3$) are in the low impedance "ON" state, either HIGH or LOW as determined by the Data Inputs; with the Output Enable input LOW, the Outputs are in the high impedance "OFF" state. The voltage level on the Output Enable input may swing between V_{DDI} and V_{SS}.

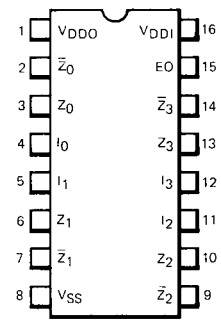
The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. For the allowable operating range of V_{DDI} and V_{DDO} see Figure 1. Each input protection circuit is terminated between V_{DDO} and V_{SS}. This allows the input signals to be driven from any potential between V_{DDO} and V_{SS}, without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10 mA.

When used in a bus organized system, all 4104B devices on the same bus line should be connected to the same V_{DDO} and V_{SS} supplies. Otherwise, parasitic diodes from the output to V_{DDO} and V_{SS} can become forward biased, even while the device is in the OFF state, causing catastrophic failure if the current is not limited to 10 mA.

- **3-STATE FULLY BUFFERED OUTPUTS**
- **OUTPUT ENABLE INPUT (ACTIVE HIGH)**
- **DUAL POWER SUPPLY**

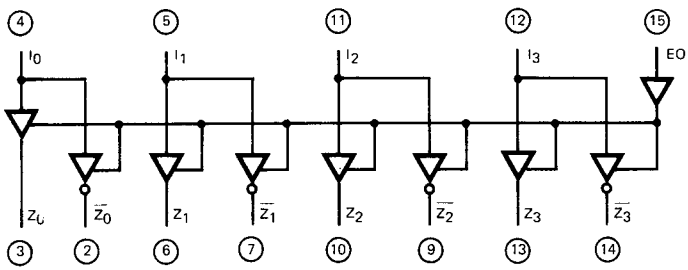
PIN NAMES	FUNCTION
I_0–I_3	Data Inputs
EO	Output Enable Input
Z_0–Z_3	Data Outputs
$\overline{Z}_0$–$\overline{Z}_3$	Complimentary Data Outputs

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC SYMBOL



V_{DDO} = Pin 1
V_{DDI} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: $V_{DDO} = V_{DDI}$ as shown, $V_{SS} = 0$ V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DDO/I}$ = 5 V			$V_{DDO/I}$ = 10 V			$V_{DDO/I}$ = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		3.5		Note 1	7		Note 1	11		Note 1	V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage		Note 2		1.5	Note 2		3	Note 2		4	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		4.95			9.95			14.95			V	MIN, 25°C	I_{OH} <1 μA Note 3
			4.95			9.95			14.95				MAX	
			4.5			9.0			13.5				All	I_{OL} <1 μA Note 4
V_{OL}	Output LOW Voltage				0.05			0.05			0.05	V	MIN, 25°C	I_{OL} <1 μA Note 3
					0.05			0.05			0.05		MAX	
					0.5			1.0			1.5		All	I_{OH} <1 μA Note 4
I_{IN}	Input Current	XC									0.3	μA	MIN, 25°C	Lead Under Test at 0 V or V_{DDO}. All Other Inputs Simultaneously at 0 V or V_{DDO}
											1.0		MAX	
		XM									0.1	μA	MIN, 25°C	
											1.0		MAX	
I_{OH}	Output HIGH Current		-1.5									mA	MIN, 25°C	V_{OUT} = 2.5 V for V_{DDO} = 5 V Note 3
			-1.0										MAX	
			-0.7			-1.4			-2.2				MIN, 25°C	$V_{OUT} = V_{DDO}$ -0.5 V Note 3
			-0.4			-0.8			-1.4				MAX	
I_{OL}	Output LOW Current		1.0			2.6			3.6			mA	MIN, 25°C MAX	V_{OUT} = 0.4 V for V_{DDO} = 5 V V_{OUT} = 0.5 V for V_{DDO} = 10 V V_{OUT} = 0.5 V for V_{DDO} = 15 V Note 3
			0.8			2.0			3.6					
			0.4			1.2			2.0					
I_{OZH}	Output OFF Current HIGH	XC									1.6	μA	MIN, 25°C	Output Returned to V_{DDO}, EO = V_{SS}
											12		MAX	
		XM									0.4	μA	MIN, 25°C	
											12		MAX	
I_{OZL}	Output OFF Current LOW	XC									-1.6	μA	MIN, 25°C	Output Returned to V_{SS}, EO = V_{SS}
											-12		MAX	
		XM									-0.4	μA	MIN, 25°C	
											-12		MAX	
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All Inputs at 0 V or $V_{DDI} = V_{DDO}$
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

NOTES:
1. V_{IH} must be less than or equal to V_{DDO}. If V_{IH} is greater than V_{DDO}, current at each input must be limited to 10 mA.
2. V_{IL} must be greater than or equal to V_{SS}, if V_{IL} is less than V_{SS}, current at each input must be limited to 10 mA.
3. Inputs at 0 V or V_{DDO} per function.
4. Inputs at minimum V_{IH} or maximum V_{IL} per function.
5. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

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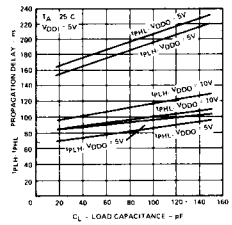
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DDI} = 5 V, V_{DDO} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 5)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DDO} = 5 V			V_{DDO} = 10 V			V_{DDO} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		160	375		85	180		75	144	ns	C_L = 50 pF,
t_{PHL}	I_n to Z_n or $\overline{Z}_n$		160	375		85	180		75	144		R_L = 200 kΩ
t_{PZH}	Output Enable Time		200	450		80	110		70	88	ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			200	450		100	170		80	136		(R_L = 1 kΩ to V_{DDO})
t_{PHZ}	Output Disable Time		75	165		90	170		75	136	ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			50	115		80	110		70	88		(R_L = 1 kΩ to V_{DDO})
t_{TLH}	Output Transition Time		60	135		30	70		25	45	ns	Input Transition
t_{THL}			60	135		30	70		25	45		Times ⩽ 20 ns

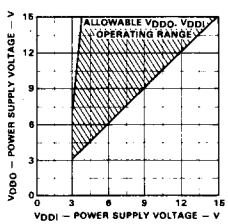
Notes on previous page.

Fig. 1 TYPICAL ELECTRICAL CHARACTERISTICS

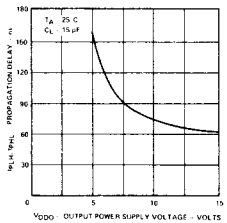
PROPAGATION DELAY VERSUS C_L



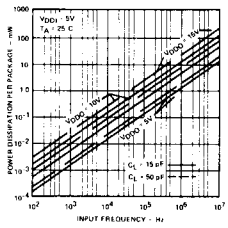
V_{DDO} VERSUS V_{DDI}



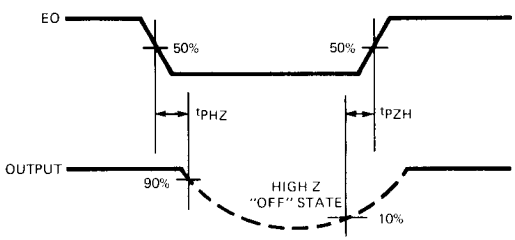
PROPAGATION DELAY VERSUS V_{DDO}



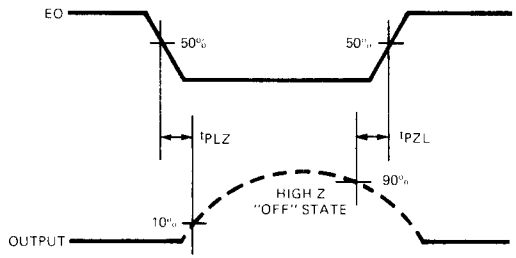
POWER DISSAPATION VERSUS FREQUENCY



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})