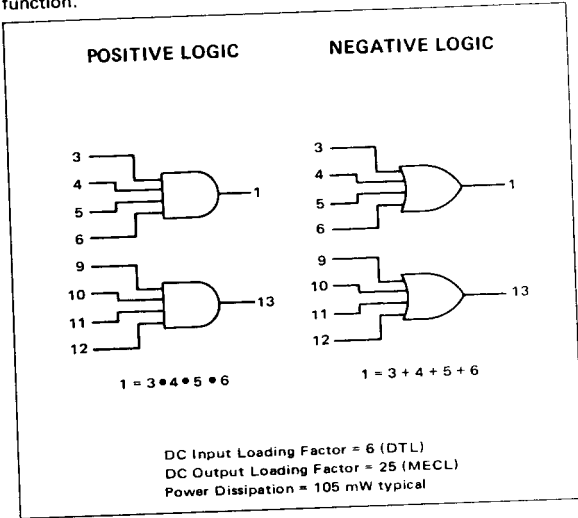


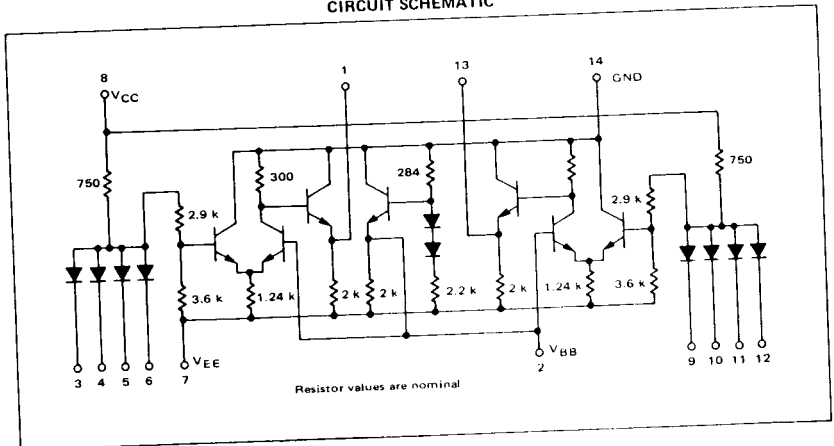
SATURATED LOGIC-TO-MECL
DUAL TRANSLATORS

MC1017
MC1217

A dual level translator for converting saturated logic levels to MECL signal levels. The translator provides the positive logic AND function.



CIRCUIT SCHEMATIC

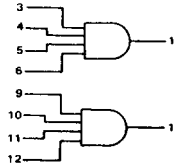


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MC1017, MC1217 (continued)

ELECTRICAL CHARACTERISTICS

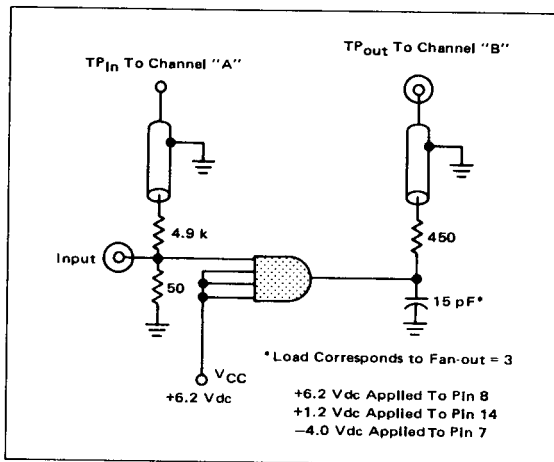
Test procedures are shown for only one translator.
The other translator is tested in the same manner.



Characteristic	Symbol	Pin Under Test	MC1217 Test Limits						Unit	MC1017 Test Limits						
			-55°C		+25°C		+125°C			0°C		+25°C		+75°C		Unit
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max	
Positive Supply Drain Current	I_C	8	-	-	-	4.0	-	-	mA dc	-	-	-	4.0	-	-	mA dc
Negative Supply Drain Current	I_E	7	-	-	-	24	-	-	mA dc	-	-	-	24	-	-	mA dc
Input Diode Reverse Current	I_R	3 4 5 6	-	-	-	0.2	-	2.0	μ A dc	-	-	-	0.2	-	2.0	μ A dc
Input Diode Forward Current	I_F	3 4 5 6	-	-	-	2.0	-	-	mA dc	-	-	-	2.0	-	-	mA dc
'OR' Logical '1' Output Voltage	V_{OH}^1	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	V dc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	V dc
'OR' Logical '0' Output Voltage	V_{OL}	1 1 1 1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	V dc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	V dc
Bias Driver Output Voltage [†]	$V_{BB}^†$	2	-1.35	-1.20	-1.26	-1.10	-1.11	-0.98	V dc	-1.28	-1.14	-1.26	-1.10	-1.19	-1.04	V dc
Switching Times			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Propagation Delay	t_{3-1}	1	17	22	15	20	13	18	ns	16	21	15	20	14	19	ns
Rise Time	t_{1-1}	↓	13	18	15	20	19	25		14	19	15	20	17	22	
Fall Time	t_{1-}	↓	7.0	10	7.0	10	8.0	12		7.0	10	7.0	10	7.0	11	
	t_{-}	↓	7.0	10	7.0	10	8.0	12		7.0	10	7.0	10	7.0	11	

¹ V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).
[†] V_{BB} limits apply from no load (0 mA) to full load (-1.0 mA).

SWITCHING TIME TEST CIRCUIT @ 25°C



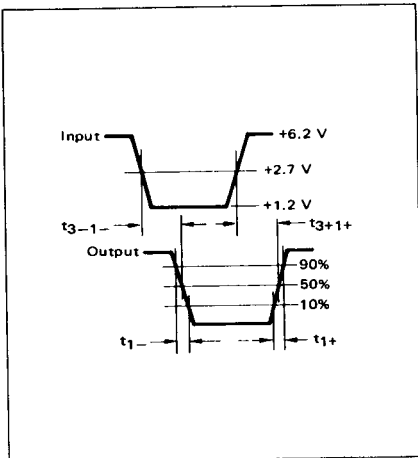
@Test
Temperature

MC1217 {
-55°C
+25°C
+125°C

MC1017 {
0°C
+25°C
+75°C

TEST VOLTAGE/CURRENT VALUES						
Vdc ± 1.0%						
V _{OH}	V _{IL}	V _{max}	V _{CC}	V _{EE}	I _L	mAdc
2.1	0.5	-	5.0	-2	2.5	-
2.0	1.0	8.0	5.0	-2	2.5	-
2.0	0.7	8.0	5.0	-2	2.5	-
2.0	0.85	-	5.0	-2	2.5	-
1.9	1.00	8.0	5.0	-2	2.5	-
1.8	0.85	8.0	5.0	-2	2.5	-

			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW						
Characteristic	Symbol	Pin Under Test	V _{OH}	V _{IL}	V _{max}	V _{CC}	V _{EE}	I _L	V _{CC} (Gnd)
Positive Supply Drain Current	I _C	8	-	-	-	8	7	-	14
Negative Supply Drain Current	I _E	7	-	-	-	8	7	-	14
Input Diode Reverse Current	I _R	3	-	-	3	-	-	-	4, 5, 6, 14
		4	-	-	4	-	-	-	3, 4, 6, 14
		5	-	-	5	-	-	-	3, 4, 6, 14
Input Diode Forward Current	I _F	3	-	-	-	8	7	-	3, 14
		4	-	-	-	8	7	-	3, 14
		5	-	-	-	8	7	-	3, 14
OR" Logical "1" Output Voltage	V _{OH} †	1	3, 4, 5, 6	-	-	8	7	1	14
		1	-	3	-	5	7	-	14
		1	-	4	-	5	7	-	14
OR" Logical "0" Output Voltage	V _{OL}	1	-	5	-	8	7	-	14
		1	-	5	-	8	7	-	14
		1	-	6	-	8	7	2†	14
Bias Driver Output Voltage	V _{BB} †	2	-	-	-	8	7	-	14
Switching Times			Pulse In	Pulse Out		(+6.2 V)	(-4.0 V)		(+1.2 V)
Propagation Delay	t ₃₋₁₊	1	1	3	-	8	7	-	14
Rise Time	t ₁₊	†	†	†	-	†	†	-	†
Fall Time	t ₁₋	†	†	†	-	†	†	-	†



SWITCHING TIME WAVEFORMS