Remote Thermal Diode Monitor with Linear Fan Control

ADM1028

FEATURES

On-Chip Temperature Sensor
External Temperature Measurement with Remote Diode
Interrupt and Over-Temperature Outputs
Fault-Tolerant Fan Control with Auto Hardware Trip Point
Remote Reset and Power-Down Functions
LDCM Support
System Management Bus (SMBus) Communications
Standby Mode to Minimize Power Consumption
Limit Comparison of all Monitored Values
DAC Output for Linear Fan Speed Control
Ramp Rate Register for Control of Rate of Change of Fan Speed, Reduction of Fan Acoustics

APPLICATIONS

Network Servers and Personal Computers
Microprocessor-Based Office Equipment
Test Equipment and Measuring Instruments

GENERAL DESCRIPTION

The ADM1028 is a low-cost temperature monitor and fan controller for microprocessor-based systems. The temperature of a remote sensor diode may be measured, allowing monitoring of processor temperature in single processor systems. An on-chip temperature sensor monitors ambient system temperature.

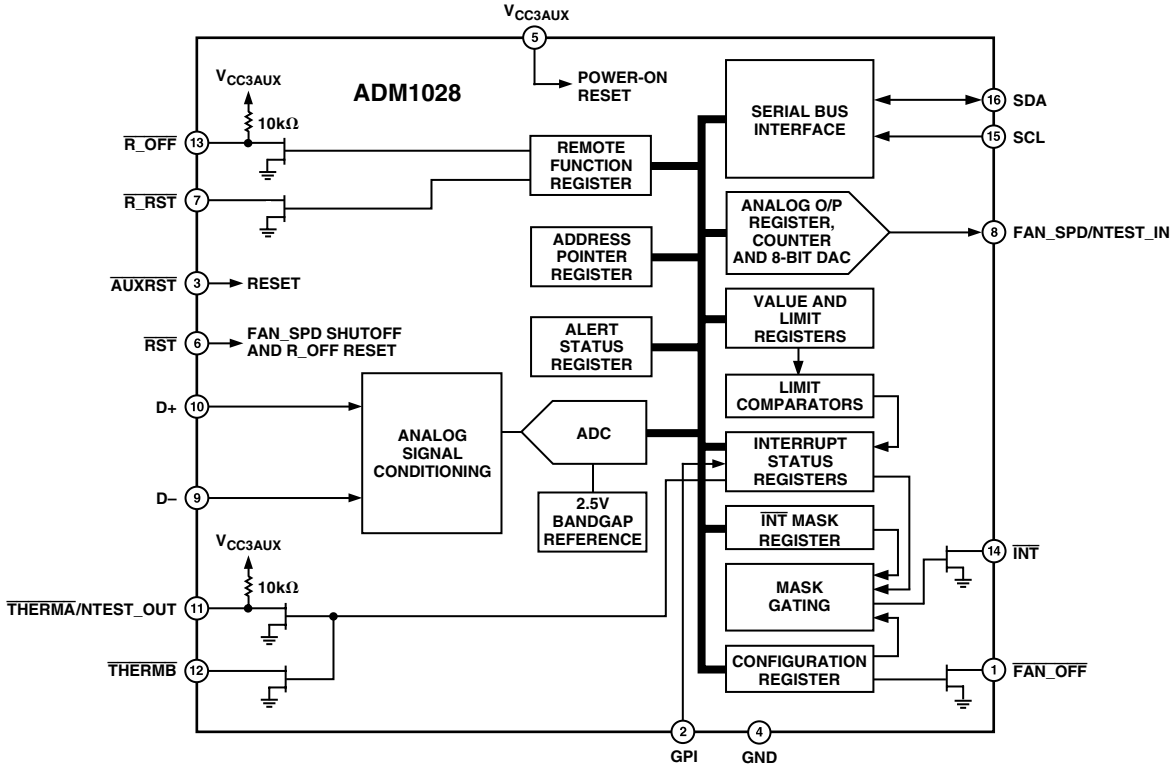
Measured values can be read out via the System Management Bus, and values for limit comparisons can be programmed in over the same serial bus.

The ADM1028 also contains a DAC for fan speed control. An automatic hardware temperature trip point is provided and the fan will be driven to full speed if it is exceeded. A Ramp Rate Register is provided to control the rate with which fan speed is increased or decreased. This is to eliminate sudden changes in fan speed, thereby reducing fan acoustics and prolonging the fan's life.

Finally, the chip has remote reset and power-down functionality, allowing it to be remotely shut down via the SMBus.

The ADM1028's 3.0 V to 5.5 V supply voltage range, low supply current, and SMBus make it ideal for a wide range of applications. These include hardware monitoring applications in PCs, electronic test equipment, and office electronics.

FUNCTIONAL BLOCK DIAGRAM



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ADM1028–SPECIFICATIONS[1, 2] ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit	Test Conditions
POWER SUPPLY					
Supply Voltage, V_{CC}	3.0	3.30	5.5	V	
Supply Current, I_{CC}		2	3.2	mA	Interface Inactive, ADC Active
TEMPERATURE-TO-DIGITAL CONVERTER					
Internal Sensor Accuracy			±3	°C	
			±2	°C	$60°C \le T_A \le 100°C$
Resolution		1		°C	
External Diode Sensor Accuracy			±5	°C	
			±3	°C	$60°C \le T_A \le 100°C$
Resolution		1		°C	
Remote Sensor Source Current		120		µA	High Level (D+ = D– + 0.65 V)
		7		µA	Low Level (D+ = D– + 0.65 V)
ANALOG OUTPUT					
Output Voltage Range	0		2.5	V	
Total Unadjusted Error, TUE			±3	%	I_L = 2 mA
Full-Scale Error		±1	±3	%	
Zero Error		±2		LSB	No Load
Differential Nonlinearity, DNL			±1	LSB	Monotonic by Design
Integral Nonlinearity		±1		LSB	
Output Source Current		2		mA	
Output Sink Current		1		mA	
$\overline{\text{THERMA}}$ OUTPUT					
$\overline{\text{THERMA}}$ Pull-Up Resistance	9	12	14	kΩ	
DIGITAL OUTPUT $\overline{\text{THERMA}}$/NTEST_OUT, R_OFF					
Output High Voltage, V_{OH}	2.4			V	I_{OUT} = 3.0 mA
Output Low Voltage, V_{OL}			0.4	V	
OPEN-DRAIN DIGITAL OUTPUTS ($\overline{\text{INT}}$, $\overline{\text{THERMB}}$, $\overline{\text{FAN\_OFF}}$, $\overline{\text{R\_RST}}$)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA
High Level Output Leakage Current, I_{OH}		0.1	1	µA	$V_{OUT} = V_{CC}$[3]
FAN SPEED RAMP RATES					
Counter Frequency	1 ± 50%		16 ± 50%	Hz	
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = –3.0 mA
High Level Output Leakage Current, I_{OH}		0.1	1	µA	$V_{OUT} = V_{CC}$
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current			±5	µA	
Hysteresis		500		mV	Note 4
DIGITAL INPUT LOGIC LEVELS (FAN_SPD/TEST_IN, GPI)					
Input High Voltage, V_{IH}	2.2			V	
Input Low Voltage, V_{IL}			0.8	V	
DIGITAL INPUT LEAKAGE CURRENT (ALL DIGITAL INPUTS)					
Input High Current, I_{IH}	–1	–0.005		µA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}		+0.005	+1	µA	V_{IN} = 0
Input Capacitance, C_{IN}	3	6	9	pF	Note 4

Parameter	Min	Typ	Max	Unit	Test Conditions
SERIAL BUS TIMING[4]					
Clock Frequency, f_{SCLK}			100	kHz	See Figure 1
Bus Free Time, t_{BUF}	4.7			µs	See Figure 1
Start Setup Time, $t_{SU;STA}$	4.7			µs	See Figure 1
Start Hold Time, $t_{HD;STA}$	4.0			µs	See Figure 1
Stop Condition Setup Time, $t_{SU;STO}$	4.0			µs	See Figure 1
SCL Low Time, t_{LOW}	4.7			µs	See Figure 1
SCL High Time, t_{HIGH}	4.0			µs	See Figure 1
SCL, SDA Rise Time, t_r			1000	ns	See Figure 1
SCL, SDA Fall Time, t_f			300	ns	See Figure 1
Data Setup Time, $t_{SU;DAT}$	250			ns	See Figure 1
Data Hold Time, $t_{HD;DAT}$	300			ns	See Figure 1

NOTES
[1]Typicals are at T_A = 25°C and represent most likely parametric norm. Standby current typ is measured with V_{CC} = 3.3 V.
[2]Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.2 V for a rising edge.
[3]I_{OH} for $\overline{FAN\_OFF}$ guaranteed by design, not production tested.
[4]Guaranteed by design, not production tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{CC}) . . . . . 6.5 V
Voltage on Digital Inputs Except Therm and D– . . . . . –0.3 V to +6.5 V
Voltage on Therm Pin . . . . . –0.3 V to V_{CC} + 0.3 V
Voltage on D– Pin . . . . . –0.3 V to + 0.6 V
Voltage on Any Other Input or Output Pin . . . . . –0.3 V to V_{CC} + 0.3 V
Input Current at Any Pin . . . . . ±5 mA
Package Input Current . . . . . ±20 mA
Maximum Junction Temperature (T_J max) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperatures
Soldering (10 sec) . . . . . 300°C
IR Reflow Peak Temperature . . . . . 220°C
ESD Rating (Human Body Model) . . . . . 4000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional. Operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

16-Lead QSOP Package:
θ_{JA} = 105°C/W, θ_{JC} = 39°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1028ARQ	0°C to 100°C	Shrink Small Outline Package (QSOP)	RQ-16

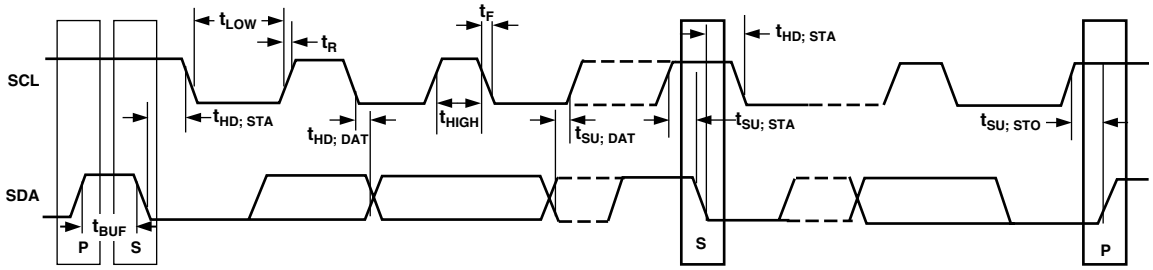
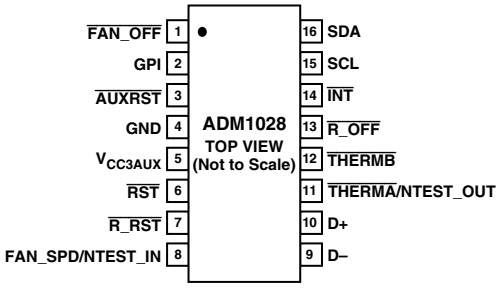


Figure 1. Serial Bus Timing Diagram

CAUTION

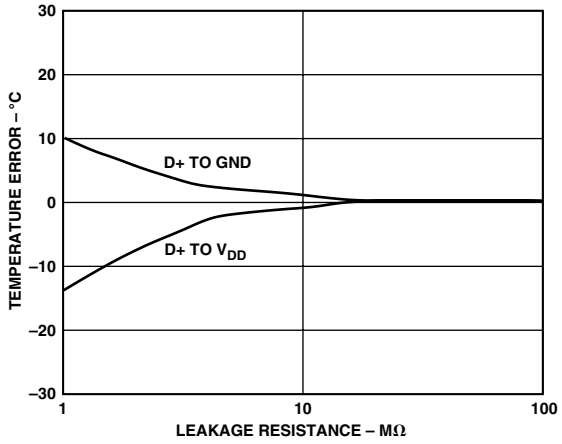
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1028 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

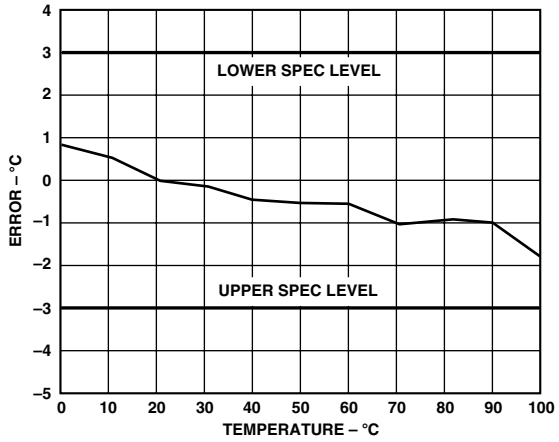


PIN FUNCTION DESCRIPTIONS

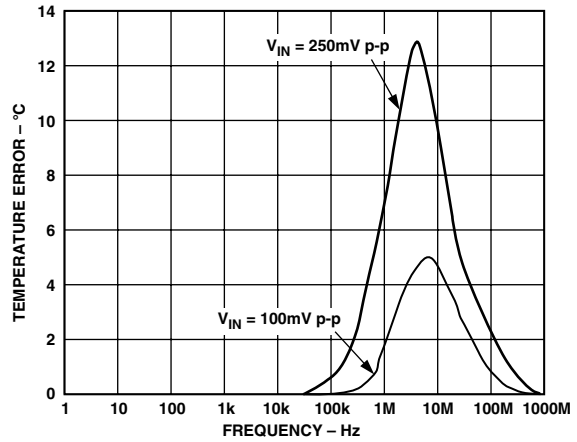
Pin No.	Mnemonic	Description
1	$\overline{\text{FAN\_OFF}}$	Digital Output (Open Drain) Fan Off Request. When asserted low, this indicates a request to shut off the fan independent of the FAN_SPD output. When negated (output FET off) it indicates that the fan may be turned on.
2	GPI	Digital Input (12 V tolerant). This pin is a general-purpose logic input with 12 V tolerance. It can be programmed as an active high or active low input that sets Bit 4 of the Interrupt Status Register. A voltage >2.2 V on this pin, represents a Logic "1," while a floating condition is interpreted as Logic "0."
3	$\overline{\text{AUXRST}}$	Digital Input. This pin can be driven low as an input to reset the ADM1028.
4	GND	Ground. Power and signal ground.
5	V_{CC3AUX}	Power 3.3 V Aux. Power source and voltage monitor input for power-on reset.
6	$\overline{\text{RST}}$	Digital Input. This pin can be pulled low externally to indicate to the ADM1028 that the main system power has been removed. The ADM1028 will shut off the FAN_SPD output and reset its $\overline{\text{R\_OFF}}$ output.
7	$\overline{\text{R\_RST}}$	Digital Output (Open Drain). This pin is a remote reset output that pulses low on receipt of a specific SMBus message.
8	FAN_SPD/NTEST_IN	Analog Output/Test Input. An active-high input that enables NAND board-level connectivity testing. Refer to section on NAND testing. Used as an analog output for fan speed control when NAND test is not selected.
9	D–	Remote Thermal Diode Negative Input. This is the negative input (current sink) from the remote thermal diode. This also serves as the negative input into the A/D.
10	D+	Remote Thermal Diode Positive Input. This is the positive input (current source) from the remote thermal diode. This serves as the positive input into the A/D.
11	$\overline{\text{THERMA}}$/NTEST_OUT	Digital Output (Open Drain with Integrated V_{CC3AUX} Pull-Up). An active low thermal overload output that indicates a violation of a temperature setpoint (over temperature). The fan is on full-speed whenever this pin is asserted low. Acts as the output of the NAND Tree when the ADM1028 is in NAND Tree Test Mode.
12	$\overline{\text{THERMB}}$	Digital Output (Open Drain). This pin is a second $\overline{\text{THERM}}$ signal. It can be used to drive external circuitry with a different external pull-up supply rail.
13	$\overline{\text{R\_OFF}}$	Digital Output or Open Drain with Integrated V_{CC3AUX} Pull-Up. Remote off (power-down) output. This pin is driven high on receipt of a specific SMBus message. The pin (and its associated register bit) remain high until the $\overline{\text{RST}}$ input is asserted low.
14	$\overline{\text{INT}}$	Digital Output (Open Drain), System Interrupt Output. This signal indicates a violation of a set trip point. The output is enabled when Bit 1 of the Configuration Register is set to 1. The default state is disabled.
15	SCL	Digital Input. SMBus Clock.
16	SDA	Digital I/O (Open Drain). SMBus Bidirectional Data.



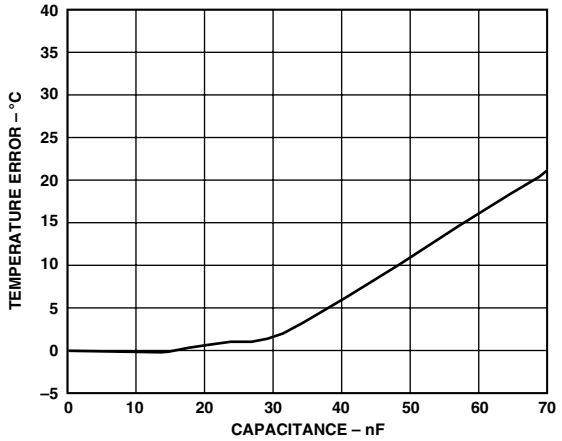
TPC 1. Temperature Error vs. PC Board Track Resistance (D+ to V_{DD})



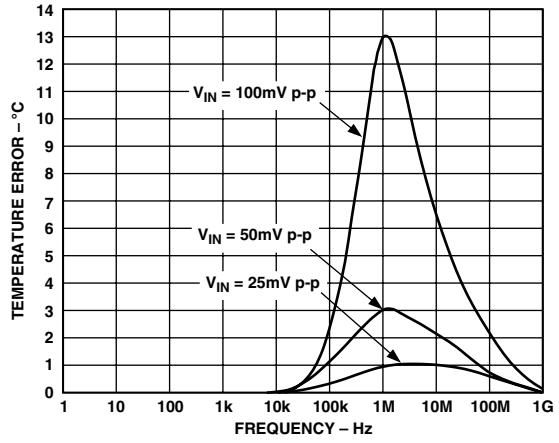
TPC 4. Temperature Error of ADM1028 vs. Pentium® III Temperature



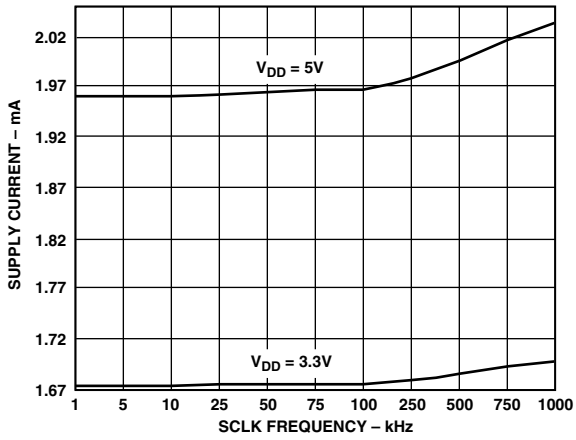
TPC 2. Temperature Error vs. Power Supply Noise Frequency



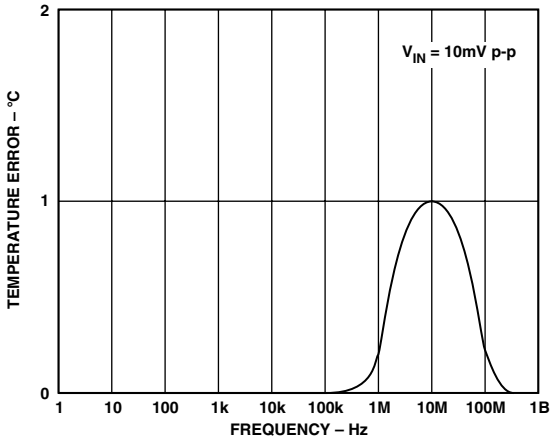
TPC 5. Temperature Error vs. Capacitance Between D+ and D–



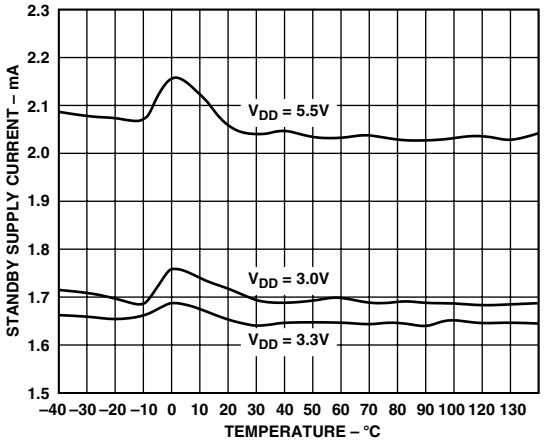
TPC 3. Temperature Error vs. Common-Mode Noise Frequency



TPC 6. Standby Current vs. Clock Frequency



TPC 7. Temperature Error vs. Differential-Mode Noise Frequency



TPC 8. Standby Supply Current vs. Temperature

FUNCTIONAL DESCRIPTION

The ADM1028 is a low-cost temperature monitor and fan controller for microprocessor-based systems. The temperature of a remote sensor diode may be measured, allowing monitoring of processor temperature in a single-processor system. An on-chip temperature sensor allows monitoring of system ambient temperature.

Measured values can be read out via the serial System Management Bus, and values for limit comparisons can be programmed in over the same serial bus.

The ADM1028 also contains a DAC for fan speed control. An automatic hardware temperature trip point is provided for fault tolerant fan control and the fan will be driven to full speed if this is exceeded. Two interrupt outputs are provided, which will be asserted if the software or hardware limits are exceeded.

Finally, the chip has remote reset and shutdown capabilities.

INTERNAL REGISTERS OF THE ADM1028

A brief description of the ADM1028's principal internal registers is given below. More detailed information on the function of each register is given in Tables III to IX.

Configuration Register: Provides control and configuration.

Address Pointer Register: This register contains the address that selects one of the other internal registers. When writing to the ADM1028, the first byte of data is always a register address, which is written to the Address Pointer Register.

Interrupt ($\overline{\text{INT}}$) Status Register: This register provides status of each Interrupt event.

Interrupt ($\overline{\text{INT}}$) Mask Register: Allows masking of individual interrupt sources.

Value and Limit Registers: The results of temperature measurements are stored in these registers, along with their limit values.

Analog Output Register: The code controlling the analog output DAC is stored in this register.

Alert Status Register: Indicates the status of the $\overline{\text{THERM}}$ signal and GPI pin.

Remote Function Register: This register allows control of the $\overline{\text{R\_RST}}$ and $\overline{\text{R\_OFF}}$ outputs.

Fan Speed Ramp Register: This register allows enabling/disabling of DAC ramp, as well as providing control of fan speed ramp rate.

SERIAL BUS INTERFACE

Control of the ADM1028 is carried out via the serial bus. The ADM1028 is connected to this bus as a slave device, under the control of a master device, e.g. the 810 chipset.

The ADM1028 has a 7-bit serial bus address. When the device powers up, it will do so with a default serial bus address. The SMBus address for the ADM1028 is 0101110 binary.

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high-to-low transition on the serial data line SDA, while the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, i.e., whether data will be written to or read from the slave device.

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{\text{W}}$ bit is a 0, the master will write to the slave device. If the R/$\overline{\text{W}}$ bit is a 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, eight bits of data followed by an Acknowledge Bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low-to-high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the tenth clock pulse to assert a STOP

condition. In READ mode, the master device will override the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADM1028, write operations contain either one or two bytes, and read operations contain one byte, and perform the following functions:

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in Figure 2a. The device address is sent over the bus followed by R/$\overline{W}$ set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there is only one possibility:

1. The serial bus address is written to the device along with the address pointer register value. The ADM1028 should then acknowledge the write by pulling SDA low during the ninth clock pulse. The master does not generate a STOP condition but issues a new START condition. The serial bus address is again sent but with the R/$\overline{W}$ bit high, indicating a READ operation. The ADM1028 will then return the data from the selected register, and a No Acknowledge is generated to signify the end of the read operation. The master will then initiate a STOP condition to end the transaction and release the SMBus.

   In Figures 2a and 2b, the serial bus address is shown as the default value 0101110.

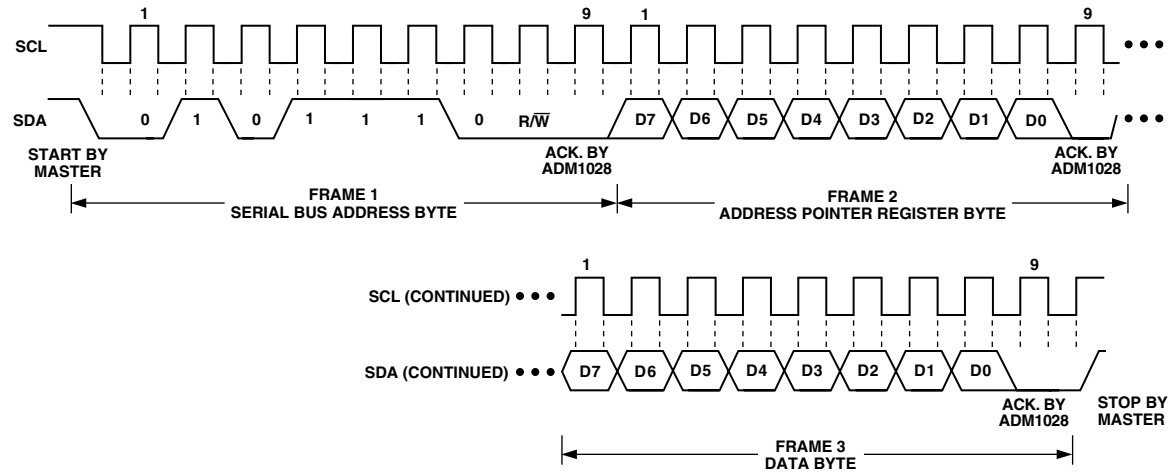


Figure 2a. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

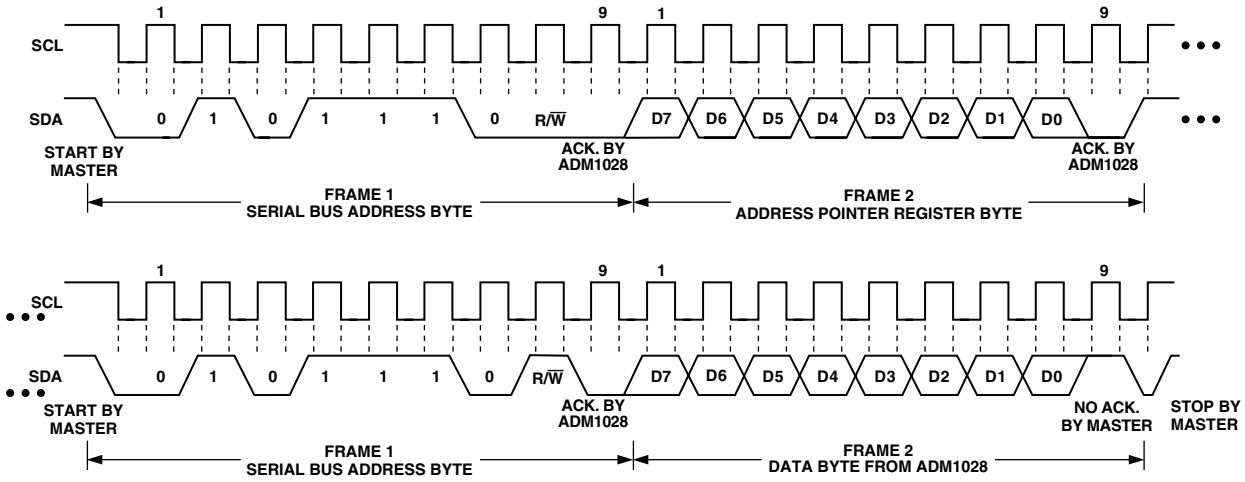


Figure 2b. Reading Data from the ADM1028

TEMPERATURE MEASUREMENT SYSTEM

Internal Temperature Measurement

The ADM1028 contains an on-chip bandgap temperature sensor. The on-chip ADC performs conversions on the output of this sensor and outputs the temperature data in 8-bit two's complement format. The format of the temperature data is shown in Table I.

Table I. Temperature Data Format

Temperature	Digital Output
–128°C	1000 0000
–125°C	1000 0011
–100°C	1001 1100
–75°C	1011 0101
–50°C	1100 1110
–25°C	1110 0111
–1°C	1111 1111
0°C	0000 0000
+1°C	0000 0001
+10°C	0000 1010
+25°C	0001 1001
+50°C	0011 0010
+75°C	0100 1011
+100°C	0110 0100
+125°C	0111 1101
+127°C	0111 1111

External Temperature Measurement

The ADM1028 can measure the temperature of an external diode sensor or diode-connected transistor, connected to Pins 9 and 10.

Pins 9 and 10 are a dedicated temperature input channel. The default functions of Pins 11 and 12 are as $\overline{\text{THERM}}$ outputs to indicate over-temperature conditions.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about –2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from device to device, and individual calibration is required to null this out, making the technique unsuitable for mass production.

The technique used in the ADM1028 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by:

$$\Delta V_{BE} = KT/q \times \ln(N)$$

where:

K is Boltzmann's constant.
q is charge on the carrier.
T is absolute temperature in Kelvins.
N is ratio of the two currents.

Figure 3 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used, the base is connected to the D– input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D– input and the base to the D+ input.

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D– input.

If the sensor is used in a very noisy environment, a capacitor of value up to 1000 pF may be placed between the D+ and D– inputs to filter the noise.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low-pass filter to remove noise, thence to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 8-bit two's complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. An external temperature measurement nominally takes 9.6 ms.

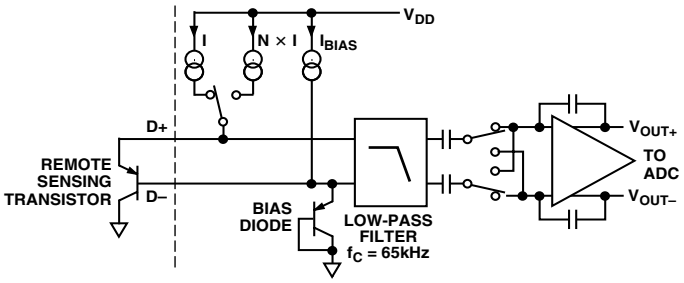


Figure 3. Signal Conditioning

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1028 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D– tracks close together, in parallel with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. Ten mil track minimum width and spacing is recommended.
4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and at the same temperature.

   Thermocouple effects should not be a major problem as 1°C corresponds to about 200 µV, and thermocouple voltages are about 3 µV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 µV.
5. Place 0.1 µF bypass and 2200 pF input filter capacitors close to the ADM1028.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted-pair cable is recommended. This will work up to about 6 to 12 feet.

7. For really long distances (up to 100 feet) use shielded twisted-pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D– and the shield to GND close to the ADM1028. Leave the remote end of the shield unconnected to avoid ground loops.

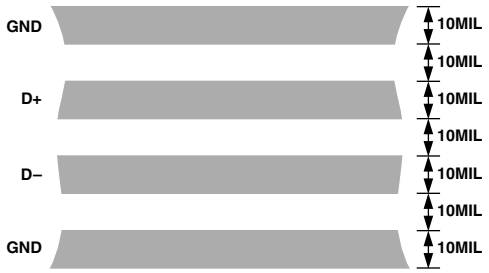


Figure 4. Arrangement of Signal Tracks

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor C1 may be reduced or removed. In any case, the total shunt capacitance should not exceed 1000 pF.

Cable resistance can also introduce errors. 1 Ω series resistance introduces about 0.5°C error.

ANALOG OUTPUT

The ADM1028 has a single analog output (FAN_SPD) from an unsigned 8-bit DAC which produces 0 V–2.5 V. The analog output register defaults to 00 during power-on reset, which produces minimum fan speed. The analog output may be amplified and buffered with external circuitry such as an op amp and transistor to provide fan speed control.

Suitable fan drive circuits are given in Figures 5a to 5e. When using any of these circuits, the following points should be noted:

1. All of these circuits will provide an output range from zero to almost $+V_{FAN}$.
2. To amplify the 2.5 V range of the analog output up to $+V_{FAN}$, the gain of these circuits needs to be set as shown.
3. Care must be taken when choosing the op amp to ensure that its input common-mode range and output voltage swing are suitable.
4. The op amp may be powered from the +V rail alone. If it is powered from +V then the input common-mode range should include ground to accommodate the minimum output voltage of the DAC, and the output voltage should swing below 0.6 V to ensure that the transistor can be turned fully off.
5. In all these circuits, the output transistor must have an I_{CMAX} greater than the maximum fan current, and be capable of dissipating power due to the voltage dropped across it when the fan is not operating at full-speed.
6. If the fan motor produces a large back e.m.f. when switched off, it may be necessary to add clamp diodes to protect the output transistors in the event that the output very quickly goes from full-scale to zero.

Figure 5c shows how the $\overline{\text{FAN\_OFF}}$ signal may be used (with any of the control circuits) to gate the fan on and off independent of the value on the FAN_SPD/NTEST_IN pin.

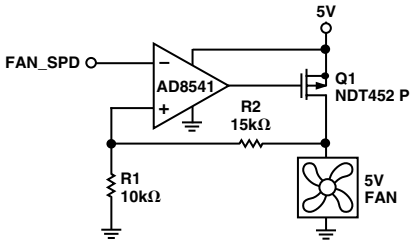


Figure 5a. 5 V Fan Circuit with Op Amp

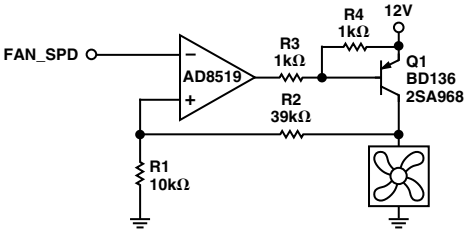


Figure 5b. 12 V Fan Circuit with Op Amp and PNP Transistor

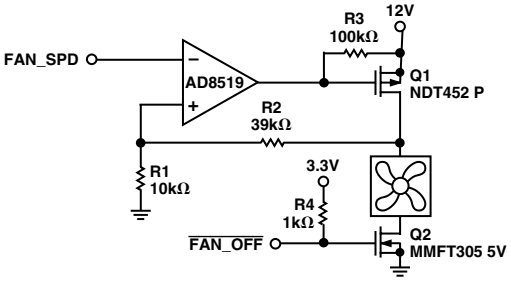


Figure 5c. 12 V Fan Circuit with Op Amp and P-Channel MOSFET

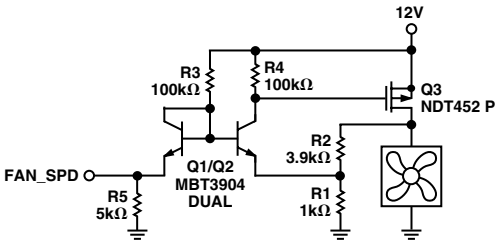


Figure 5d. Discrete 12 V Fan Drive Circuit with P-Channel MOSFET, Single Supply

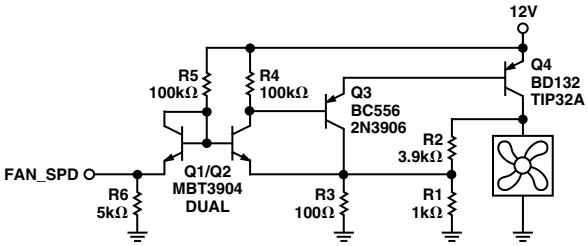


Figure 5e. Discrete 12 V Fan Drive Circuit with Bipolar Output Single Supply

FAULT TOLERANT FAN CONTROL

The ADM1028 incorporates a fault tolerant fan control capability that is tied to operation of the $\overline{\text{THERMA}}$, $\overline{\text{THERMB}}$ outputs. It can override the setting of the analog output and force it to maximum to give full fan speed in the event of a critical over-temperature problem, even if, for some reason, this has not been handled by the system software.

There are two temperature set point registers that will activate the fault tolerant fan control. One of these limits is programmable by the user and one is a hardware (read-only) register that will operate if the user does not program any limit. The fault tolerant fan control is activated if a limit is exceeded for three or more consecutive readings. These limits are separate from the normal high and low temperature limits for the $\overline{\text{INT}}$ output, which do not affect the fault tolerant fan control or $\overline{\text{THERM}}$ outputs.

A hardware limit of 100°C is programmed into the register at address 18h, for the remote diode Default $\overline{\text{THERM}}$ limit. This is the default limit and the analog output will be forced to full-scale if the remote sensor reads more than 100°C. This makes the fault tolerant fan control fail-safe in that it will operate at this temperature even if the user has programmed no other limit, or in the event of a software malfunction. Similarly, the Default Internal Temp $\overline{\text{THERM}}$ limit held in register 17h, forces the analog output full-scale if the ambient temperature measured is more than 70°C.

The user may override the default limits by programming a new limit into register 14h for the remote sensor and a new limit into register 13h for the internal sensor. The default value in register 14h is the same as for the read-only register (100°C), but it may be programmed with higher or lower values.

Once registers 13h and 14h have been programmed, or if the defaults are acceptable, Bit 3 of the configuration register must be set to "1." This bit is a write-once bit that can only be written to "1," and it has two effects:

1. It makes the values in registers 13h and 14h the active limits, and disables read-only registers 17h and 18h.
2. It locks the data into registers 13h and 14h, so that it cannot be changed until the lock bit is reset, either when $\overline{\text{AUXRST}}$ or $\overline{\text{RST}}$ is asserted, or a Power-On Reset occurs.

Once the hardware override of the analog output is triggered, it will only return to normal operation after three consecutive measurements that are 5 degrees lower than the set limit.

Whenever FAN_SPD output is forced to full-scale, the $\overline{\text{FAN\_OFF}}$ output is negated.

FAN SPEED RAMPING

The ADM1028 device contains a Fan Speed Ramping mechanism that is accomplished using an 8-bit counter and a control register. On power-up, or an assertion of $\overline{\text{RST}}$ or $\overline{\text{AUXRST}}$, the Fan Speed Register, counter, and Fan Speed Ramp Register are initialized to 0x00. The fan speed ramping mechanism is disabled by default and any value written to the Fan Speed Register is immediately reflected on the FAN_SPD output. Setting Bit 0 of the Fan Speed Ramp Rate Register enables the ramping mechanism. The counter is then preloaded with the current value contained in the Fan Speed Register, which prevents the fan speed from changing until a new value is written to the Fan Speed Register.

When a new target Fan Speed Value is written to the Fan Speed Register, the counter begins counting up or down (depending on whether the current value is greater or less than the target value). The counter will then count at the rate specified by the ramp rate bits of the Fan Speed Ramp Register. Once the counter reaches the target value the counter will stop counting. The FAN_SPD value is derived from the output of the counter. If a new value is written to the Fan Speed Register while a ramp function is occurring, the counter may change count direction to reach the new target value. The operation of $\overline{\text{THERM}}$ is independent of the fan speed ramping mechanism. Thus, $\overline{\text{THERM}}$ will assert immediately for over-temperature conditions.

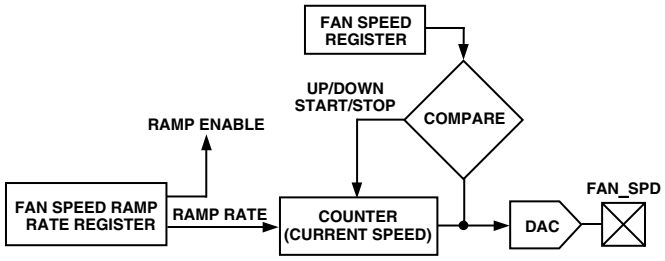


Figure 6.

THE ADM1028 INTERRUPT SYSTEM

The ADM1028 has three interrupt outputs, $\overline{\text{INT}}$, $\overline{\text{THERMA}}$ and $\overline{\text{THERMB}}$. These have different functions. $\overline{\text{INT}}$ responds to violations of software programmed temperature limits and its interrupt sources are maskable, as described in more detail later. Interrupts and status bits are only set if a limit is exceeded for at least three consecutive conversions.

Operation of the $\overline{\text{INT}}$ output is illustrated in Figure 7. Assuming that the temperature starts off within the programmed limits and that temperature interrupt sources are not masked, $\overline{\text{INT}}$ will go low if the temperature measured by the external sensor goes outside the programmed high or low temperature limit for the sensor. $\overline{\text{INT}}$ also goes low whenever $\overline{\text{THERM}}$ is low.

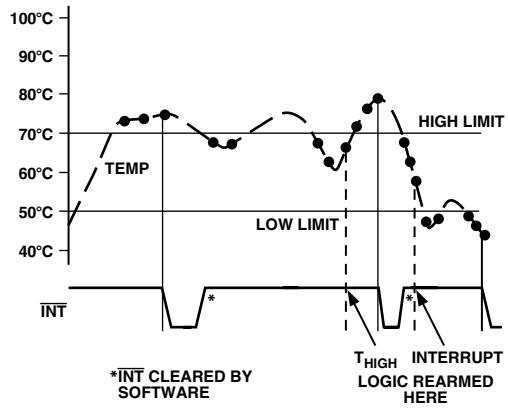


Figure 7. Operation of $\overline{\text{INT}}$ Output

Once the interrupt has been cleared, it will not be reasserted even if the temperature remains outside the limit previously exceeded. However, $\overline{\text{INT}}$ will be rearmed if the temperature falls back within the set limits for three consecutive conversions. Once the $\overline{\text{INT}}$ function has been rearmed, it will then be reasserted once a limit is exceeded for three consecutive conversions.

INTERRUPT MASKING

Any of the bits in the Interrupt Status Register can be masked out by setting the corresponding mask bit in the Interrupt Mask Register. That interrupt source will then no longer generate an interrupt. However, the bits in the status register will be set as normal.

INTERRUPT CLEARING

The Interrupt Status Register reflects out-of-limit conditions. The Status bits may be individually cleared by writing a "1" to the appropriate status bits. Writing a "1" to Bits 1 and 2 causes software interrupts to be generated. Bit 4 (GPI) of the Interrupt Status Register reflects the current status of the GPI pin, and so cannot be cleared by writing to this bit.

The $\overline{\text{INT}}$ output is cleared with the $\overline{\text{INT}}$_Enable bit, which is Bit 1 of the Configuration Register, without affecting the contents of the Interrupt ($\overline{\text{INT}}$) Status Registers.

$\overline{\text{THERM}}$ OUTPUTS

The $\overline{\text{THERMA}}$, $\overline{\text{THERMB}}$ signals are functionally identical. These system over-temperature outputs will assert together when an over-temperature is detected. $\overline{\text{THERMA}}$ (Pin 11) is an open drain digital output which has an integrated pull-up resistor to V_{CC3AUX}. $\overline{\text{THERMB}}$ is an open drain digital output, intended to drive external circuitry operating at a different supply voltage level.

$\overline{\text{THERM}}$ OPERATING MODE

$\overline{\text{THERM}}$ only responds to the "hardware" temperature limits at addresses 14h and 18h, not to the software programmed limits. The function of these registers was described earlier with regard to fault tolerant fan speed control.

$\overline{\text{THERM}}$ will go low if the hardware temperature limit is exceeded for three consecutive measurements. It will remain low until the temperature falls five degrees below the limit for three consecutive measurements. While $\overline{\text{THERM}}$ is low, the analog output will go to FFh to boost a controlled fan to full speed and $\overline{\text{FAN\_OFF}}$ will be negated.

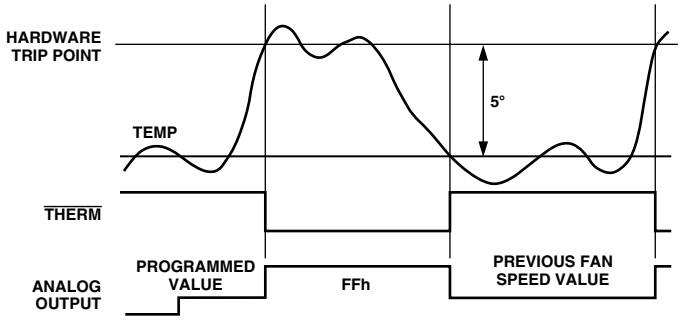


Figure 8. Operation of $\overline{\text{THERM}}$ Outputs

When the Fault Tolerant Fan Control state is exited, the analog FAN_SPD output returns to its previously programmed value, which may have been changed during the time that the FAN_SPD output was forced to FFh.

INTERRUPT STRUCTURE

The Interrupt Structure of the ADM1028 is shown in more detail in Figure 9. As each measurement value is obtained and stored in the appropriate value register, the value and the limits from the corresponding limit registers are fed to the high and low limit comparators. The result of each comparison (1 = out of limit, 0 = in limit) is routed to the corresponding bit input of the Interrupt Status Register via a data demultiplexer, and used to set that bit high or low as appropriate.

The Interrupt Mask Register has bits corresponding to each of the Interrupt Status Register Bits. Setting an Interrupt Mask Bit high forces the corresponding Status Bit output low, while setting an Interrupt Mask Bit low allows the corresponding Status Bit to be asserted. After masking, the status bits are all OR'd together to produce the $\overline{\text{INT}}$ output, which will pull low if any unmasked status bit goes high, i.e. when any measured value goes out of limit.

The $\overline{\text{INT}}$ output is enabled when Bit 1 of the Configuration Register ($\overline{\text{INT}}$_Enable) is high.

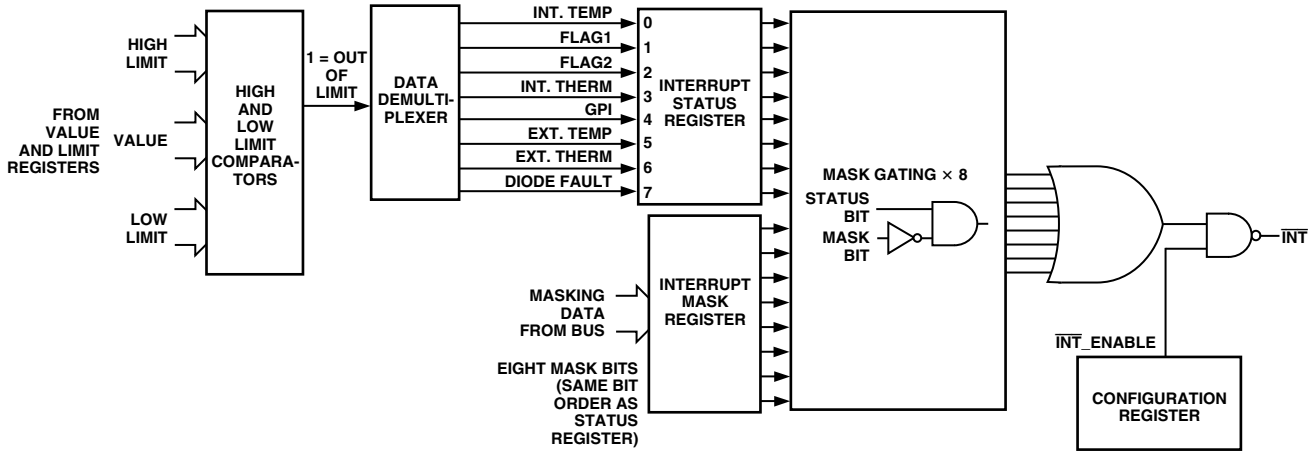


Figure 9. Interrupt Register Structure

GENERAL-PURPOSE LOGIC INPUT (GPI)

Pin 2 is used as a general-purpose logic input with 12 V tolerance. The GPI input may be programmed to be active high or active low by clearing or setting Bit 6 of the Configuration Register. The default value is active high. Bit 4 of the Interrupt Status register follows the state (or inverted state) of GPI and will generate an interrupt when it is set to 1, like any other input to the Interrupt Status Register. However, the GPI bit is not latched in the Status Register and always reflects the current state (or inverted state) of the GPI input. If it is 1, it will not be cleared by reading the Status Register.

POWER-ON RESET

When the ADM1028 is powered up, it will initiate a power-on reset sequence when the supply voltage V_{CC3AUX} rises above the power-on reset threshold, with registers being reset to their power-on values. Normal operation will begin when the supply voltage rises above the reset threshold. Registers whose power-on values are not shown have power-on conditions that are indeterminate (this includes the Value and Limit Registers). In most applications, usually the first action after power-on would be to write limits into the Limit Registers.

Power-on reset clears or initializes the following registers (the initialized values are shown in Table III):

- Configuration Register
- Interrupt Status Register
- Interrupt Mask Register
- Analog Output Register
- Programmable Trip Point Registers

The ADM1028 can also be reset by taking $\overline{\text{AUXRST}}$ low as an input. All registers will be reset to their default values and the ADC will remain inactive as long as $\overline{\text{AUXRST}}$ is below the reset threshold. Taking the $\overline{\text{RST}}$ pin low will cause the following registers to be reset.

- Bit 3 of the Configuration Register (Programmable $\overline{\text{THERM}}$ Limit Lock Bit)
- DAC Output, Fan Speed

INITIALIZATION (SOFT RESET)

Soft reset performs a similar, but not identical, function to power-on reset. It restores the power-on default values to the Configuration Register, the Interrupt Status Register and the Interrupt Mask Register. The Limit Registers remain unchanged. It rearms the $\overline{\text{INT}}$ structure but not the $\overline{\text{THERM}}$ structure.

Soft reset is accomplished by setting Bit 4 of the Configuration Register high. This bit automatically clears after being set.

Unlike clearing $\overline{\text{INT}}$, where the temperature must fall back within the set limits for three conversions before the $\overline{\text{INT}}$ function is rearmed, the soft reset allows $\overline{\text{INT}}$ to be pulled low immediately after the soft reset.

NAND TREE TEST

A NAND tree is provided in the ADM1028 for Automated Test Equipment (ATE) board level connectivity testing. The device is placed into NAND tree test mode by powering up with pin FAN_SPD/NTEST_IN (Pin 8) held high. This pin is sampled and its state at power-up is latched. If it is connected high, then the NAND tree test mode is invoked. NAND tree test mode will only be exited once the ADM1028 is powered down.

In NAND tree test mode, all digital inputs may be tested as illustrated in Table II. $\overline{\text{THERMA}}$/NTEST_OUT will become the NAND tree output pin.

The structure of the NAND Tree is shown in Figure 10. To perform a NAND Tree test, all pins are initially driven low. The test vectors set all inputs low then, one-by-one, toggles them high (keeping them high). Exercising the test circuit with this "walking one" pattern, starting with the input closest to the output of the tree, cycling toward the farthest, causes the output of the tree to toggle with each input change. Allow for a typical propagation delay of 500 ns.

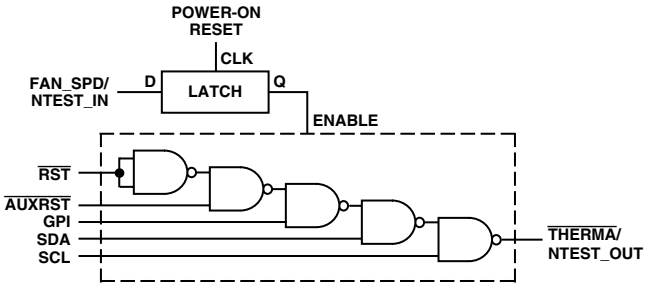


Figure 10. NAND Tree

CONFIGURING THE INTERRUPT

On power-up, the Interrupt functionality of the device is disabled. The Configuration Register (0x40) must be written to, in order to enable the interrupt output. The $\overline{\text{INT}}$_Enable bit (Bit 1) of the Register should be set to 1.

Table II. Test Vectors

$\overline{\text{RST}}$	$\overline{\text{AUXRST}}$	GPI	SDA	SCL	$\overline{\text{THERMA}}$
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	1	1
0	0	1	1	1	0
0	1	1	1	1	1
1	1	1	1	1	0

Table III. ADM1028 Registers

Register Name	Address A7–A0 in Hex	Comments
Value Registers	0x14–0x38	See Table IV
Company ID	0x3E	This location will contain the company identification number. This register is read only.
Revision	0x3F	This location will contain the revision number of the part in the lower four bits of the register [3:0]. The upper four bits reflect the ADM1028 Version Number [7:4]. The first version is 1101. The next version of ADM1028 would be 1110, etc. For instance, if the stepping were A0 and this part is an ADM1028, this register would read 1101 0000. This register is read only.
Configuration Register	0x40	See Table V. Power-on value = 0010 0001.
Interrupt Status Register	0x41	See Table VI. Power-on value = 0000 0000.
Interrupt Mask Register	0x43	See Table VII. Power-on value = 0000 0000.
Manufacturer Test	0x44–0x4A	Test Registers for manufacturer's use only. Do not write to these registers.
Remote Function	0x4B	See Table VIII. Power-on value = 0000 0000.
Alert Status	0x4C	See Table IX. Power-on value = 0000 0000.
Fan Speed Ramp Register	0xCO	See Table X. Power-on value = 0000 0000.

Table IV. Registers 0x13–0x3A Value Registers

Address	Read/Write	Description
0x13	Read/Write	Programmable Internal Therm Automatic Trip Point—Default 127°C. This register can only be written to if the write once bit in the Configuration Register (0x40, Bit 3) has not been set.
0x14	Read/Write	Programmable Remote Thermal Diode Automatic Trip Point—Default 100°C. This register can only be written to if the write once bit in the Configuration Register (0x40, Bit 3) has not been set.
0x15	Read/Write	Test register for manufacturer's use only. Do not write to this register.
0x17	Read Only	Default Internal Therm Automatic Trip Point—Default 70°C. Cannot be changed. Disabled when Bit 3 of Configuration Register is set.
0x18	Read Only	Default Remote Thermal Diode Automatic Trip Point—Default 100°C. Cannot be changed. Disabled when Bit 3 of Configuration Register is set.
0x19	Read/Write	Analog Output, FAN_SPD (Defaults to 0x00h).
0x26	Read Only	External/Remote Temperature Value.
0x27	Read Only	Internal Temperature Value.
0x37	Read/Write	External/Remote Temperature High Limit—Default +127°C.
0x38	Read/Write	External/Remote Temperature Low Limit—Default –128°C.
0x39	Read/Write	Internal Temperature High Limit—Default +127°C.
0x3A	Read/Write	Internal Temperature Low Limit—Default –128°C.

Table V. Register 0x40 Configuration Register Power-On Default <7:0> = 21h

Bit	Name	R/$\overline{W}$	Description
0	START	Read/Write	Setting this bit to a "1" enables startup of ADM1028; clearing this bit to "0" places ADM1028 in standby mode. At startup, temperature monitoring and limit checking functions begin. Note, all limit values should be programmed into ADM1028 prior to using the standard thermal interrupt mechanism based upon high and low limits. (Power-Up Default = 1.)
1	$\overline{INT}$ Enable	Read/Write	Setting this bit to a "1" enables the $\overline{INT}$ output. 1 = Enabled 0 = Disabled (Power-Up Default = 0.)
2	Reserved	Read Only	Reserved (Default = 0).
3	Programmable Therm Limit Lock Bit	Read/Write Once	Setting this bit to a "1" will lock in the value set into the Programmable Remote Therm Limit Register (Value Register 0x14). Furthermore, if this bit is set, the values in the Default Remote Therm Limit Register Bit (Value Register 0x18) will no longer have an effect on the $\overline{THERM}$, FAN_SPD, or $\overline{FAN\_OFF}$ outputs. This bit cannot be written again until after RST has been asserted. (Power-Up Default = 0.)
4	Soft Reset	Read/Write	Setting this bit to a "1" will restore power-up default values to the Configuration Register, Interrupt Status Register and Interrupt Mask Register. This also rearms $\overline{INT}$ structure but not the THERM structure. This bit automatically clears itself since the power-on default is zero.
5	$\overline{FAN\_OFF}$	Read/Write	Setting this bit to a "1" will cause the $\overline{FAN\_OFF}$ pin to be floated. Clearing this bit to "0" will cause the $\overline{FAN\_OFF}$ pin to be driven low which requests that the fan be turned off. This bit will be unconditionally set if the $\overline{THERM}$ pin is ever asserted; once $\overline{THERM}$ is negated this bit must be returned to its prior state (prior to $\overline{THERM}$ assertion). Reading this bit reflects the state of the $\overline{FAN\_OFF}$ output buffer. Due to the open-drain nature of this pin the value read does not represent the actual state of the external circuit connected to it. (Power-Up Default = 1.)
6	GPI Invert	Read/Write	Setting this bit to a "1" will invert the GPI input for the purpose of level detection and interrupt generation. Clearing this bit to "0" leaves the GPI input unmodified. (Power-Up Default = 0.)
7	Reserved	Read Only	Reserved. (Power-Up Default = 0).

Table VI. Register 0x41. Interrupt Status Register. Power-On Default <7:0> = 00h

Bit	Name	Read/Write	Description
0	Int. Temp Error	Read/Write "1" to clear	A one indicates that one of the limits for the internal temperature sensor has been exceeded.
1	Flag 1	Read/Write	This bit can be used as a general purpose flag with the capability of generating an interrupt. Writing a "1" to this bit causes it to be set to "1." Writing a "0" clears this bit.
2	Flag 2	Read/Write	This bit can be used as a general purpose flag with the capability of generating an interrupt. Writing a "1" to this bit causes it to be set to "1." Writing a "0" clears this bit.
3	Int. $\overline{THERM}$	Read/Write "1" to clear	A one indicates that the internal thermal overload ($\overline{THERM}$) limit has been exceeded.
4	GPI Input	Read Only	A "1" indicates that the GPI pin is asserted. The polarity of the GPI pin is determined by GPI Invert (Bit 6) in the Configuration Register. For example, if GPI Invert is cleared then this bit will be "1" when the GPI pin is high ("1"); this bit will be "0" when the GPI pin is low ("0".) If GPI Invert is set then this bit will be "1" when the GPI pin is low ("0"); this bit will be "0" when the GPI pin is high ("1"). Note that the state of GPI is not latched; this bit simply reflects the state or inverted state of the GPI pin. Note: if this bit is "1" reading this register will NOT clear it to "0."
5	Ext. Temp Error	Read/Write "1" to clear	A one indicates that one of the limits for the external temperature sensor has been exceeded.
6	Ext. $\overline{THERM}$	Read/Write "1" to clear	A one indicates that the external thermal overload ($\overline{THERM}$) limit has been exceeded.
7	Ext Diode Fault	Read/Write "1" to clear	A one indicates either a short- or open-circuit fault on the remote sensor diode.

Table VII. Register 0x43 Interrupt Mask Register. Power-On Default <7:0> = 00h

Bit	Name	Read/Write	Description
0	Int Temp Error	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.
1	Flag 1 Mask	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.
2	Flag 2 Mask	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.
3	Int $\overline{\text{THERM}}$	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.
4	GPI Mask	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.
5	Ext Temp Error	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.
6	Ext $\overline{\text{THERM}}$	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.
7	Ext Diode Fault	Read/Write	A one disables the corresponding interrupt status bit for the $\overline{\text{INT}}$ output.

Table VIII. Register 0x4B Remote Function Register. Power-On Default <7:0> = 00h

Bit	Name	Read/Write	Description
0	$\overline{\text{R\_RST}}$	Read/Write	Writing a "1" to this bit causes the $\overline{\text{R\_RST}}$ output to be pulsed low for a minimum of 125 µs. This bit will self-clear to 0 when the $\overline{\text{R\_RST}}$ pulse is complete. Writing a "0" to this bit has no effect. Reading this bit reflects the state of this register bit and not the state of the pin. The power-on default value is "0."
1	$\overline{\text{R\_OFF}}$	Read/Write	Writing a "1" to this bit causes the $\overline{\text{R\_OFF}}$ output to be driven high. This bit will be cleared, and the output driven low, when $\overline{\text{RST}}$ is asserted. Writing a "0" to this bit has no effect. The power-on default value is "0."
2	Reserved	Read/Write	Reserved (Default = 0).
3	Reserved	Read/Write	Reserved (Default = 0).
4	Reserved	Read/Write	Reserved (Default = 0).
5	Reserved	Read/Write	Reserved (Default = 0).
6	Reserved	Read/Write	Reserved (Default = 0).
7	Reserved	Read/Write	Reserved (Default = 0).

Table IX. Register 0x4C Alert Status Register. Power-On Default <7:0> = 00h

Bit	Name	Read/Write	Description
0	Ext $\overline{\text{THERM}}$ Alert	Read Only	A one indicates that the external thermal overload limit is currently exceeded.
1	GPI Alert	Read Only	This bit represents the logic level of the GPI pin if Bit 6 of the Configuration Register is "0," or the inverse logic level of the GPI pin if Bit 6 of the Configuration Register is "1."
2	Int $\overline{\text{THERM}}$ Alert	Read Only	A one indicates that the internal thermal overload limit is currently exceeded.
3	Reserved	Read Only	Undefined.
4	Reserved	Read Only	Undefined.
5	Reserved	Read Only	Undefined.
6	Reserved	Read Only	Undefined.
7	Reserved	Read Only	Undefined.

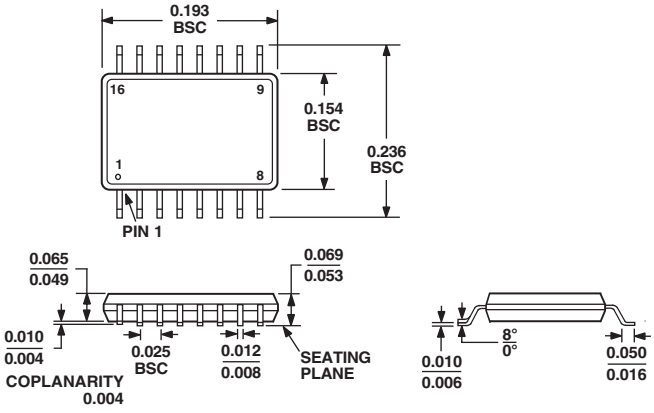
Table X. Register 0xCO Fan Speed Ramp Register. Power-On Default <7:0> = 00h

Bit	Name	Read/Write	Description
0	Fan Speed Ramp Enable	Read/Write	Setting this bit to a "1" will enable the fan speed ramping mechanism. When this bit is a 1, writing to the Fan Speed Register will set the new target fan speed; the input to the DAC will then count, up or down as appropriate, to the new fan speed value at the rate specified in bits [1:2] of this register. Clearing this bit to "0" will disable the fan speed ramping mechanism and will cause data written to the Fan Speed Register to be immediately reflected to the DAC. The DAC input may or may not continue ramping if this bit is changed from a "1" to a "0" while the fan speed is currently ramping.
<2:1>	Ramp Rate	Read/Write	Fan Speed Ramp Rate. The speed at which the fan speed ramp counter increments/decrements is selected as follows: Bits <2:1> — Count Rate — Counter Frequency 00 — 1.0s — 1 Hz 01 — 0.25s — 4 Hz 10 — 0.125s — 8 Hz 11 — 0.0625s — 16 Hz
<7:3>	Reserved	Read/Write	Reserved (Default = 0)

C02365–0–4/03(B)

OUTLINE DIMENSIONS

16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches



COMPLIANT TO JEDEC STANDARDS MO-137AB

Revision History

Location **Page**

4/03—Data Sheet changed from REV. A to REV. B.

Added ESD Caution 3
Updated OUTLINE DIMENSIONS 16

2/02—Data Sheet changed from REV. 0 to REV. A.

Edits to FUNCTIONAL BLOCK DIAGRAM 1
Edits to SPECIFICATIONS 2
Added Fan Speed Ramp Register 6
Edits to Table III 13
Added Table X 16