Click here to ask about the production status of specific part numbers.

MAX32680

Ultra-Low-Power Arm Cortex-M4F with Precision Analog Front-End and Bluetooth LE 5.2

General Description

The MAX32680 microcontroller (MCU) is an advanced system-on-chip (SoC), featuring an Arm® Cortex®-M4F CPU for efficient computation of complex functions and algorithms that is qualified to operate at a temperature range of -40°C to +85°C. The SoC integrates power regulation and management with a single-inductor multiple-output (SIMO) buck regulator system. Onboard is the latest generation Bluetooth® 5.2 Low Energy (LE) radio, supporting LE Audio, angle of arrival (AoA), and angle of departure (AoD) for direction finding, long-range (coded) modes, and high-throughput modes.

The device offers large onboard memory with 512KB flash and 128KB SRAM, with optional error correction coding (ECC) on one 32KB SRAM bank. This 32KB bank can be optionally retained in BACKUP mode. An 8KB user one-time programmable (OTP) area is available, and 8 bytes are retained, even during power-down.

An analog front-end (AFE) provides two 12-channel delta-sigma (Δ-Σ) analog-to-digital converters (ADC) with features and specifications optimized for precision sensor measurement. Each Δ-Σ ADC can digitize external analog signals as well as system temperature. An optional programmable gain amplifier (PGA) with gains of 1x to 128x precedes each ADC. ADC outputs can be optionally converted on the fly from integer to single-precision floating-point format. A 12-bit digital-to-analog converter (DAC) is also included. The device also provides robust security features such as an advanced encryption standard (AES) engine, true random number generator (TRNG), and secure boot.

The device is available in an 88L LGA (10mm x 10mm, 0.4mm pitch) package.

Applications

- Industrial Pressure, Temperature, Level, and Flow Sensors/Transmitters
- Medical Pressure and Temperature Sensors

Benefits and Features

- Ultra-Low-Power Wireless Microcontroller
  - Internal 100MHz Oscillator
  - 512KB Flash and 128KB SRAM
    - Optional ECC on One 32KB SRAM Bank
- Bluetooth 5.2 LE Radio
  - Dedicated, Ultra-Low-Power, 32-Bit RISC-V Coprocessor to Offload Timing-Critical Bluetooth Processing
  - Fully Open-Source Bluetooth 5.2 Stack Available
  - Supports AoA, AoD, LE Audio, and Mesh
  - High-Throughput (2Mbps) Mode
  - Long-Range (125kbps and 500kbps) Modes
  - Rx Sensitivity: -97.5dBm; Tx Power: +4.5dBm
  - Single-Ended Antenna Connection (50Ω)
- Smart Integration Reduces BOM, Cost, and PCB Size
  - Two 16-Bit to 24-Bit Δ-Σ ADCs
    - 12 Channels, Assignable to Either ADC
    - Flexible Resolution and Sample Rates
      - 24-Bits at 0.4ksps, 16-Bits at 4ksps
  - Four External Input, 10-Bit Δ-Σ ADC 7.8ksps
  - 12-Bit DAC
  - On-Die Temperature Sensor
  - Digital Peripherals: Two SPI, Two I^2C, up to Four UART, and up to 36 GPIOs
  - Timers: Six 32-Bit Timers, Two Watchdog Timers, Two Pulse Trains, 1-Wire® Master
- Power Management Maximizes Battery Life
  - 2.0V to 3.6V Supply Voltage Range
  - Integrated SIMO Power Regulator
  - Dynamic Voltage Scaling (DVS)
  - 23.8µA/MHz ACTIVE Mode Current at 3.0V Coremark®
  - 4.4µA at 3.0V Retention Current for 32KB SRAM
  - Selectable SRAM Retention in Low-Power Modes
- Robust Security and Reliability
  - TRNG
  - Secure Nonvolatile Key Storage and AES-128/192/256
  - Secure Boot to Protect IP/Firmware
  - Wide, -40°C to +85°C Operating Temperature

***Ordering Information* appears at end of data sheet.**

19-101233; Rev 0; 8/21

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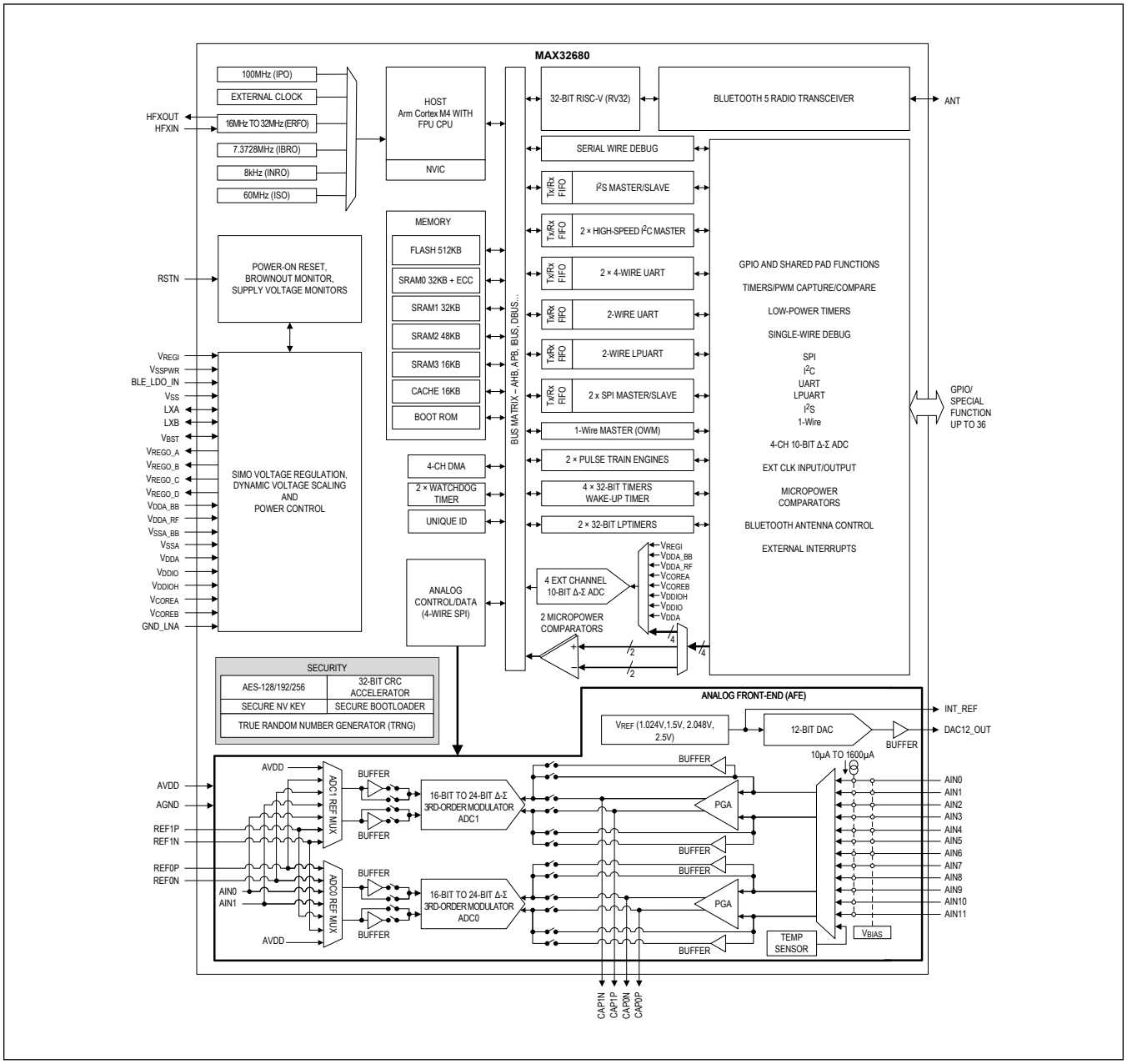
Simplified Block Diagram



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Absolute Maximum Ratings

V_{COREA}, V_{COREB} ..... -0.3V to +1.21V
V_{DDIO}, V_{DDA} ..... -0.3V to +1.98V
V_{DDIOH}, AVDD ..... -0.3V to +3.63V
AIN[0-11] ..... V_{SSA} - 0.03V to AVDD + 0.03V
V_{REGI} ..... -0.3V to +3.63V
V_{DDA_RF}, V_{DDA_BB} ..... -0.3V to +1.21V
BLE_LDO_IN ..... -0.3V to +1.5V
RSTN, GPIO (V_{DDIOH}) ..... -0.3V to V_{DDIOH} + 0.5V
GPIO (V_{DDIO}) ..... -0.3V to V_{DDIO} + 0.5V
HFXIN, HFXOUT, RSTN, GPIO ..... -0.3V to V_{DDIO} + 0.3V
REF1P, REF1N, REF0P, REF0N, VREG1, CAP1N, CAP1P, CAP0N, CAP0P, DAC12_OUT ..... -0.3V to AVDD + 0.3V
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA
V_{DDIO} Combined Pins (sink) 100mA
V_{DDIOH} Combined Pins (sink) 100mA
V_{SSA}, V_{SSA_BB} 100mA
V_{SS}, AGND, GND_LNA 100mA
V_{SSPWR} 100mA
Continuous Package Power Dissipation CTBGA (multilayer board) T_A = +70°C (derate 18.99mW/°C above +70°C) 1518.99mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	L8800M+1
Outline Number	21-100567
Land Pattern Number	90-100205
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	N/A
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	52.67°C/W
Junction to Case (θ_{JC})	27.00°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Core Input Supply Voltage A	V_{COREA}		0.9	1.1	1.21	V
Core Input Supply Voltage B	V_{COREB}		0.9	1.1	1.21	V
Input Supply Voltage, Battery	V_{REGI}		2.7	3.3	3.63	V
Input Supply Voltage, Analog	AVDD	A_{VDD} must be connected to V_{DDIOH}	2.7	3.3	3.63	V
	V_{DDA}		1.71	1.8	1.98	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage, GPIO	V_{DDIO}		1.71	1.8	1.98	V
Input Supply Voltage, GPIO (High)	V_{DDIOH}	V_{DDIOH} must be connected to AVDD	1.71	3.0	3.63	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{COREA}		0.76		V
		Monitors V_{COREB}	0.72	0.77		
		Monitors V_{DDA}	1.58	1.64	1.69	
		Monitors V_{DDIO}	1.58	1.64	1.69	
		Monitors V_{DDIOH}	1.58	1.64	1.69	
		Monitors V_{REGI}	1.91	1.98	2.08	
		Monitors V_{DDA_BB}		0.773		
		Monitors V_{DDA_RF}		0.773		
Power-On Reset Voltage	V_{POR}	Monitors V_{COREA}		0.57		V
		Monitors V_{DDA}		1.25		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REGI} Current, ACTIVE Mode	I_{REGI_DACT}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode executing Coremark, RV32 in SLEEP mode, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		23.8		µA/MHz
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 and RV32 in ACTIVE mode executing While(1), ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA. This specification is a function of the IPO frequency.		29.3		
		Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode executing While(1), RV32 in SLEEP mode, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		22.2		
		Dynamic, total current into V_{REGI} pin, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in ACTIVE mode running from ISO, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		18.7		
	I_{REGI_FACT}	Fixed, IPO enabled, ISO enabled, total current into V_{REGI}, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in ACTIVE mode 0MHz, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		740		µA
V_{REGI} Current, SLEEP Mode	I_{REGI_DSLP}	Dynamic, IPO enabled, $f_{SYS\_CLK(MAX)}$ = 100MHz, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode, ECC disabled, standard DMA with two channels active; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		6.4		µA/MHz
	I_{REGI_FSLP}	Fixed, IPO enabled, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 in SLEEP mode, RV32 in SLEEP mode, ECC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		1.33		mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REGI} Current, LOW POWER Mode	I_{REGI_DLP}	Dynamic, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 powered off, RV32 in ACTIVE mode, $f_{SYS\_CLK(MAX)}$ = 60MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			18.7		µA/MHz
	I_{REGI_FLP}	Fixed, ISO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, CM4 powered off, RV32 in ACTIVE mode 0MHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			630		µA
V_{REGI} Current, MICRO POWER Mode	I_{REGI_DMP}	Dynamic, ERTCO enabled, IBRO enabled, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, LPUART active, f_{LPUART} = 32.768kHz; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			230		µA
V_{REGI} Current, STANDBY Mode	I_{REGI_STBY}	Fixed, total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA			7.1		µA
V_{REGI} Current, BACKUP Mode	I_{REGI_BK}	Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	All SRAM retained		6.3		µA
		Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA	No SRAM retention		3		
		Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V, RTC disabled; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	SRAM0 retained		4.4		
			SRAM0 and SRAM1 retained		5.2		
			SRAM0, SRAM1, and SRAM2 retained		5.6		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REGI} Current, POWER DOWN Mode	I_{REGI_PDM}	Total current into V_{REGI} pins, V_{REGI} = 3.0V, V_{COREA} = V_{COREB} = 1.1V; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		0.16		µA
V_{REGO_X} Output Current	$V_{REGO\_X\_IOUT}$	Output current for each of the V_{REGO_X} outputs		5	50	mA
V_{REGO_X} Output Current Combined	$V_{REGO\_X\_IOUT\_TOT}$	All four V_{REGO_X} outputs combined		15	100	mA
V_{REGO_X} Output Voltage Range	$V_{REGO\_X\_RANGE}$	$V_{REGI} \geq V_{REGO\_X}$ + 200mV; output voltage range must be configured to meet the input voltage range of the load device pin (V_{RST} to V_{MAX})	V_{RST}	1.0	V_{MAX}	V
V_{REGO_X} Efficiency	$V_{REGO\_X\_EFF}$	V_{REGI} = 2.7V, V_{REGO_X} = 1.1V, load = 30mA		90		%
SLEEP Mode Resume Time	t_{SLP_ON}	Time from power mode exit to execution of first user instruction		0.847		µs
LOW POWER Mode Resume Time	t_{LP_ON}	Time from power mode exit to execution of first user instruction		6.08		µs
MICRO POWER Mode Resume Time	t_{MP_ON}	Time from power mode exit to execution of first user instruction		12.4		us
STANDBY Mode Resume Time	t_{STBY_ON}	Time from power mode exit to execution of first user instruction		14.7		µs
BACKUP Mode Resume Time	t_{BKU_ON}	Time from power mode exit to execution of first user instruction		1.15		ms
POWER DOWN Mode Resume Time	t_{PDM_ON}	Time from power mode exit to execution of first user instruction		5		ms
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		0.0625		100,000	kHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		ns
Internal Primary Oscillator (IPO)	f_{IPO}			100		MHz
Internal Secondary Oscillator (ISO)	f_{ISO}			60		MHz
Internal Baud Rate Oscillator (IBRO)	f_{IBRO}			7.3728		MHz
Internal Nanoring Oscillator (INRO)	f_{INRO}	8kHz selected		8		kHz
		16kHz selected		16		
		30kHz selected		32		
External RF Oscillator Frequency (ERFO)	f_{ERFO}	32MHz crystal, C_L = 12pF, ESR ≤ 50Ω, C_0 ≤ 7pF, temperature stability ±20ppm, initial tolerance ±20ppm		32		MHz
External System Clock Input Frequency	f_{EXT_CLK}	EXT_CLK selected			80	MHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Low-Power Timer 1 Clock Input Frequency	$f_{EXT\_LPTMR1\_CLK}$	LPTMR1_CLK selected			8	MHz
External Low-Power Timer 2 Clock Input Frequency	$f_{EXT\_LPTMR2\_CLK}$	LPTMR2_CLK selected			8	MHz
GENERAL-PURPOSE I/O						
Input Low Voltage	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	
Input Low Voltage for RSTN	V_{IL_RSTN}			0.5 x V_{DDIOH}		V
Input High Voltage	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply	0.7 × V_{DDIO}			V
	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply	0.7 × V_{DDIOH}			
Input High Voltage for RSTN	V_{IH_RSTN}			0.5 x V_{DDIOH}		V
Output Low Voltage	V_{OL_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = 1mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA	V_{DDIO} - 0.4			
	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 00, I_{OL} = -1mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 01, I_{OL} = -2mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 10, I_{OL} = -8mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] = 11, I_{OL} = -8mA	V_{DDIOH} - 0.4			
		V_{DDIOH} = 1.71V, GPIOn_DS_SEL[1:0] fixed at 00, I_{OL} = -1mA	V_{DDIOH} - 0.4			
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-100		+100	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-800		+800	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pullup Resistor RSTN	R_{PU_R}	Pullup to V_{DDIOH}		25		kΩ
Input Pullup/Pulldown Resistor for All GPIO	R_{PU1}	Normal resistance, P1M = 0		25		kΩ
	R_{PU2}	Highest resistance, P1M = 1		1		MΩ
BLUETOOTH RADIO / POWER						
Bluetooth LDO Input Voltage	$V_{BLE\_LDO\_IN}$		0.9	1.1	1.5	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BLUETOOTH RADIO / FREQUENCY						
Operating Frequency		1MHz channel spacing	2360		2500	MHz
PLL Programming Resolution	PLL_{RES}			1		MHz
Frequency Deviation at 1Mbps	Δf_{1MHz}			±170		kHz
Frequency Deviation at BLE 1Mbps	$\Delta f_{BLE1MHz}$			±250		kHz
Frequency Deviation at 2Mbps	Δf_{2MHz}			±320		kHz
Frequency Deviation at BLE 2Mbps	$\Delta f_{BLE2MHz}$			±500		kHz
BLUETOOTH RADIO / CURRENT CONSUMPTION (SIMO enabled, V_{REGI} = 3.3V. IPO enabled, f_{SYS_CLK} = 100MHz, Bluetooth LE stack running on CM4. Measured at the V_{REGI} device pin, V_{REGO_B} = 0.9V, V_{REGO_C} = 1.0V, RV32 in SLEEP mode.)						
Tx Run Current	$I_{TX\_+4.5DBM}$	P_{RF} = +4.5dBm		6.35		mA
	$I_{RFFE\_+4.5DBM}$			4.3		
	I_{TX_0DBM}	P_{RF} = 0dBm		4.17		
	I_{RFFE_0DBM}			2.12		
	I_{TX_-10DBM}	P_{RF} = -10dBm		3.65		
	I_{RFFE_-10DBM}			1.65		
Tx Startup Current	I_{START_TX}			2.05		mA
BLUETOOTH RADIO / CURRENT CONSUMPTION (SIMO enabled, V_{REGI} = 3.3V. IPO enabled, f_{SYS_CLK} = 100MHz, Bluetooth LE stack running on CM4. Measured at the V_{REGI} device pin, V_{REGO_B} = 0.9V, V_{REGO_C} = 1.0V, RV32 in SLEEP mode)						
Rx Run Current	I_{RX_1M}	f_{RX} = 1Mbps		4.0		mA
	I_{RX_2M}	f_{RX} = 2Mbps		4.12		
	I_{RFFE_1M}	f_{RX} = 1Mbps		1.95		
	I_{RFFE_2M}	f_{RX} = 2Mbps		2.07		
Rx Startup Current	I_{START_RX}			2.05		mA
BLUETOOTH RADIO / TRANSMITTER						
Maximum Output Power	P_{RF}			+4.5		dBm
RF Power Accuracy	P_{RF_ACC}			±1		dB
First Adjacent Channel Transmit Power ±2MHz	P_{RF1_1}	1Mbps Bluetooth LE		-30.5		dBc
First Adjacent Channel Transmit Power ±4MHz	P_{RF2_1}	1Mbps Bluetooth LE		-40		dBc
BLUETOOTH RADIO / RECEIVER						
Maximum Received Signal Strength at < 0.1% PER	P_{RX_MAX}			0		dBm

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Sensitivity, Ideal Transmitter	P_{SENS_IT}	Measured with 37 byte payload	1Mbps Bluetooth LE		-97.5		dBm
			2Mbps Bluetooth LE		-94		
Receiver Sensitivity, Dirty Transmitter	P_{SENS_DT}	Measured with 37 byte payload	1Mbps Bluetooth LE		-95.5		dBm
			2Mbps Bluetooth LE		-93		
Receiver Sensitivity, Long-Range Coded	P_{SENS_LR}	Measured with 37 byte payload	125kbps Bluetooth LE		-105.5		dBm
			500kbps Bluetooth LE		-101		
C/I Cochannel	C/I_{1MHz}	1Mbps Bluetooth LE			6.7		dB
	C/I_{2Mhz}	2Mbps Bluetooth LE			7		
Adjacent Interference	C/I_{+1_1}	+1MHz offset, 1Mbps Bluetooth LE			-2.5		dB
	C/I_{-1_1}	-1MHz offset, 1Mbps Bluetooth LE			-2.6		
	C/I_{+2_1}	+2MHz offset, 1Mbps Bluetooth LE			-22		
	C/I_{-2_1}	-2MHz offset, 1Mbps Bluetooth LE			-24		
	C/I_{+2_2}	+2MHz offset, 2Mbps Bluetooth LE			-2		
	C/I_{-2_2}	-2MHz offset, 2Mbps Bluetooth LE			-3		
	C/I_{+4_2}	+4MHz offset, 2Mbps Bluetooth LE			-32		
	C/I_{-4_2}	-4MHz offset, 2Mbps Bluetooth LE			-34		
Adjacent Interference, (3+n) MHz Offset [n = 0, 1, 2, . . .]	C/I_{3+MHZ}	1Mbps Bluetooth LE			-34.5		dB
Adjacent Interference, (6+2n) MHz Offset [n = 0, 1, 2, . . .]	C/I_{6+MHZ}	2Mbps Bluetooth LE			-34		dB
Intermodulation Performance, 1Mbps Bluetooth LE with 3MHz, 4MHz, 5MHz Offset	P_{IMD_1MBPS}	1Mbps Bluetooth LE			-38		dBm
Intermodulation Performance, 2Mbps Bluetooth LE with 6MHz, 8MHz, 10MHz Offset	P_{IMD_2MBPS}	2Mbps Bluetooth LE			-38		dBm
Received Signal Strength Indicator Accuracy	$RSSI_{ACC}$				±3		dB
Received Signal Strength Indicator Range	$RSSI_{RANGE}$				-98 to -50		dB
ADC (Δ-Σ)							
Resolution					10		bits

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Clock Rate	f_{ACLK}			0.1		8	MHz
ADC Clock Period	t_{ACLK}				$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[15:12], ADC_DIVSEL = [00], ADC_CH_SEL = [7:4]	REF_SEL = 0, INPUT_SCALE = 0	V_{SSA} + 0.05		V_{BG}	V
		AIN[15:12, ADC_DIVSEL = [01], ADC_CH_SEL = [7:4]	REF_SCALE = 0, INPUT_SCALE = 0	V_{SSA} + 0.05		2 x V_{BG}	
		AIN[15:12], ADC_DIVSEL = [10], ADC_CH_SEL = [7:4]	REF_SCALE = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	V_{SSA} + 0.05		V_{DDIOH}	
		AIN[15:12], ADC_DIVSEL = [11], ADC_CH_SEL = [7:4]	REF_SEL = 0, INPUT_SCALE = 0, V_{DDIOH} selected as the I/O supply	V_{SSA} + 0.05		V_{DDIOH}	
Input Impedance	R_{AIN}				30		kΩ
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}			1		pF
		Dynamically switched capacitance			250		fF
Integral Nonlinearity	INL	Measured at +25°C				±2	LSb
Differential Nonlinearity	DNL	Measured at +25°C				±1	LSb
Offset Error	V_{OS}				±1		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled			102		µA
ADC Setup Time	t_{ADC_SU}	Any power-up of ADC clock or ADC bias to CpuAdcStart				10	µs
ADC Output Latency	t_{ADC}				1067		t_{ACLK}
ADC Sample Rate	f_{ADC}					7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	ADC inactive or channel not selected			10		nA
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF			1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method			30		ppm
COMPARATORS							
Input Offset Voltage	V_{OFFSET}				±1		mV
Input Hysteresis	V_{HYST}	AINCOMPHYST[1:0] = 00			±23		mV
		AINCOMPHYST[1:0] = 01			±50		
		AINCOMPHYST[1:0] = 10			±2		
		AINCOMPHYST[1:0] = 11			±7		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN_CMP}	Common-mode range	0.6		1.35	V
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		20		ms
	t_{P_ERASE}	Page erase		20		
Flash Programming Time per Word	t_{PROG}			42		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +125°C	10			years

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA

(AVDD = +3.3V, REFP - REFN = AVDD, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Full-Scale Input Voltage				$\pm V_{REF}$/ Gain		
Absolute Input Voltage		Buffers disabled	V_{SSA} - 30mV		AVDD + 30mV	V
Input Voltage Range		Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}$		V_{REF}	
Common-Mode Voltage Range	V_{CM}	AIN buffers/PGA disabled	V_{SSA}		AVDD	V
		Buffers enabled	V_{SSA} + 0.1		AVDD - 0.1	
		PGA gain = 1 to 16	V_{SSA}+0.1 + (V_{IN})(Gain)/2		AVDD - 0.1 - (V_{IN})(Gain)/2	
		PGA gain = 32 to 128	V_{SSA} + 0.2 + (V_{IN})(Gain)/2		AVDD - 0.2 - (V_{IN})(Gain)/2	
Differential Input Current		Buffer disabled		±1		µA/V
		Buffer enabled		0 to 50		nA
		PGA enabled, GBD		±1		
Absolute Input Current		Buffer disabled		±1		µA/V
		Buffer enabled		20 to 80		nA
		PGA enabled, -40°C to +85°C, GBD		±2		
Input Capacitance		Bypass mode		10		pF
SYSTEM PERFORMANCE						
Resolution				24		bits

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(AVDD = +3.3V, REFP - REFN = AVDD, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate		50Hz/60Hz FIR filter, single-cycle conversions		1, 2, 4, 8, 16		sps
		50Hz FIR filter, single-cycle conversions		1.3, 2.5, 5, 10, 20, 35.6		
		60Hz FIR filter, single-cycle conversions		1.3, 2.5. 5, 10, 20, 36.5		
		SINC4 filter, single-cycle conversions		1, 2.5, 5, 10, 15, 30, 60, 120, 240, 480, 960, 1920		
		SINC4 filter, continuous conversions		4, 10, 20, 40, 60, 120, 240, 480, 960, 1920, 3840, 7680		
		SINC4 filter, duty cycle conversions		0.25, 0.63, 1.25, 2.5, 3.75, 7.7, 15, 30, 60, 120, 240, 480		
Data Rate Tolerance		Determined by internal clock accuracy	-6		6	%
Integral Nonlinearity (*Note 2*)	INL	Differential input, reference buffer enabled, PGA = 1, tested at 16sps, measured at +25°C, AVDD = 3.3V	-12	+2	+12	ppmFS
		Differential input, PGA = 2 to 16		6		
		Differential input, PGA = 32 to 64		11		
		Differential input, PGA = 128		15		
Offset Error		Referred to modulator input. After self and system calibration; V_{REFP} - V_{REFN} = 2.5V, tested at 16sps, measured at AVDD = 3.3V	-25	±0.5	+25	µV
Offset Error Drift				±50		nV/°C

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(AVDD = +3.3V, REFP - REFN = AVDD, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGA Gain Settings				1, 2, 4, 8, 16, 32, 64, 128		
Digital Gain Settings				2, 4		
PGA Gain Error (*Note 1*)		No calibration		±0.3		%
		Gain = 1, after calibration	-0.012		+0.012	
PGA Gain Drift (*Note 2*)				32		ppmFS/°C
Input Noise	V_n	FIR50Hz/60Hz, 16.8sps, PGA = 128		208		nV_{RMS}
Noise-Free Resolution	NFR	FIR50Hz/60Hz, 16.8sps, PGA = 1		17.3		bits
Normal Mode Rejection (Internal Clock)	NMR	50Hz/60Hz FIR filter, 50Hz ±1%, 16sps conversion, GBD		88		dB
		50Hz/60Hz FIR filter, 60Hz ±1%, 16sps single-cycle conversion, GBD		88		
		50Hz FIR filter, 50Hz ±1%, 35.6sps single-cycle conversion, GBD		49		
		60Hz FIR filter, 60Hz ±1%, 35.6sps single-cycle conversion, GBD		55.6		
		SINC4 filter, 50Hz ±1%, 10sps single-cycle conversion, GBD		88		
		SINC4 filter, 60Hz ±1%, 10sps single-cycle conversion, GBD		91		
Normal Mode Rejection (External Clock)	NMR	50Hz/60Hz FIR filter, 50Hz or 60Hz ±1%, 16sps single-cycle conversion		91		dB
		50Hz FIR filter, 50Hz ±1%, 35.6sps single-cycle conversion		49.4		
		60Hz FIR filter, 60Hz ±1%, 35.6sps single-cycle conversion		55.6		
		SINC4 filter, 50Hz ±1%, 10sps single-cycle conversion		92.4		
		SINC4 filter, 60Hz ±1%, 10sps single-cycle conversion		92.6		
Common-Mode Rejection	CMR	DC rejection, any PGA gain		100		dB
	CMR60	50Hz/60Hz rejection, PGA enabled		104		
Power Supply Rejection	PSRRA			94		dB
REFERENCE INPUTS						
Reference Voltage Range		Reference buffer(s) disabled	V_{SSA} - 30m		AVDD + 30m	V
		Reference buffer(s) enabled	V_{SSA} + 0.1		AVDD - 0.1	
Reference Voltage Input		V_{REF} = V_{REFP} - V_{REFN}	0.75	2.5	AVDD	V

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(AVDD = +3.3V, REFP - REFN = AVDD, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Input Current		Reference buffer disabled		2.1		µA/V
		Reference buffer enabled	-200	61	+200	nA
Reference Input Capacitance		Reference buffers disabled		15		pF
MATCHED CURRENT SOURCES						
Matched Current Source Outputs	IDAC			10, 50, 75, 100, 125, 150, 175, 200, 225, 250, 300, 400, 600, 800, 1200, 1600		µA
Current Source Output Voltage Compliance		IDAC ≤ 250µA	0		AVDD - 0.7	V
		IDAC = 1.6mA	0		AVDD - 1.2	
Initial Tolerance		T_A = +25°C, GBD	-5	±1	+5	%
Temperature Drift		Each IDAC		±50		ppm/°C
Current Matching		Between IDACs		±0.1		%
Temperature Drift Matching		Between IDACs		10		ppm/°C
Current Source Output Noise	I_N	Output current = 250µA. SINC4 filter, 60sps continuous. Noise is referred to input.		0.47		pA rms
V_{BIAS} OUTPUTS						
V_{BIAS} Voltage				AVDD/2		V
V_{BIAS} Voltage Output Impedance				125k (active), 20k (passive), 125k (passive)		Ω
SYSTEM TIMING						
Power-On Wake-Up Time		From AVDD > V_{POR}		240		µs
PGA Power-Up Time		C_{FILTER} = 0		0.25		ms
		C_{FILTER} = 20nF		2		
		C_{FILTER} = 100nF		10		

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(AVDD = +3.3V, REFP - REFN = AVDD, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGA Settling Time		After changing gain settings to Gain = 1, C_{FILTER} = 0		0.25		ms
		After changing gain settings to Gain = 1, C_{FILTER} = 100nF		10		
		After changing gain settings to Gain = 128, C_{FILTER} = 0		2		
Input Multiplexer Power-Up Time		Settled to 21 bits with 10pF load		2		µs
Input Multiplexer Channel-to-Channel Settling Time		Settled to 21 bits with 2kΩ external source resistor		2		µs
V_{BIAS} Power-Up Time		Active generator; settled within 1% of final value; C_{LOAD} = 1µF		10		ms
		125K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		575		
		20K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		90		
V_{BIAS} Settling Time		Active generator; settled within 1% of final value; C_{LOAD} = 1µF		10		ms
		125K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		605		
		20K passive generator; settled within 1% of final value; C_{LOAD} = 1µF		100		
Matched Current Source Startup Time				110		µs
Matched Current Source Settling Time				12.5		µs

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(AVDD = +3.3V, REFP - REFN = AVDD, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SPECIFICATIONS							
AVDD Current		ADC0 only	Standby mode		92		µA
			Bypass mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 60sps		167		
			Buffered mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 60sps		193.7		
			PGA enabled, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 60sps		292.4		
		ADC1. ADC0 must be enabled in Standby mode.	Bypass mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 60sps		167		
			Buffered mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 60sps		193.7		
			PGA enabled, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 60sps		292.4		

Electrical Characteristics—16-/24-Bit Δ-Σ ADC with PGA (continued)

(AVDD = +3.3V, REFP - REFN = AVDD, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AVDD Duty Cycle Power Mode		ADC0 only	Bypass mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 15sps		74		µA
			Buffered mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 15sps		89.1		
			PGA enabled, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 15sps		195.7		
		ADC1. ADC0 must be enabled in Standby mode.	Bypass mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 15sps		74		
			Buffered mode, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 15sps		89.1		
			PGA enabled, IDAC, V_{BIAS} sources off, AVDD = V_{REF} = V_{IN} = 3.3V, SINC4 filter, continuous conversions at 15sps		195.7		

Electrical Characteristics—12-Bit DAC

(AVDD = 3.3V, R_L = 10kΩ and C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A = +25°C for typical specifications, unless otherwise noted. VREF = 1.5V. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution	DAC_R			12			bits
Differential Nonlinearity	DNL	Power mode = 2 or 3, noise filter enabled GBD			±1		LSB
Integral Nonlinearity	INL	Power mode = 2 or 3, noise filter enabled GBD			±1		LSB
Offset Error	E_O	Measured at AVDD = 3.3V			±1		mV
Output Voltage Range	V_O	Min code to max code, GBD		V_{SSA} + E_O		AVDD - 0.5 + E_G	V
Output Impedance		Power mode = 3			6.1		kΩ
		Power mode = 2			8.9		
		Power mode = 1			16.3		
		Power mode = 0			97.7		
Voltage Output Settling Time	t_{SFS}	Noise filter enabled, code 400h to C00h, rising or falling, to ±0.5 LSB			4		ms
		Noise filter disabled, code 400h to C00h, rising or falling, to ±0.5 LSB			0.03		
Glitch Energy		Power mode = 0, 1, or 2			12		V x ns
		Power mode = 3, code 000h to A50h			12		
Active Current	I_{DAC12}	Static, V_{REF} = 2.5V	Power mode = 3		680		µA
			Power mode = 2		570		
			Power mode = 1		458		
			Power mode = 0		347		
		Static, V_{REF} = 2.0V	Power mode = 3		601		
			Power mode = 2		509		
			Power mode = 1		418		
			Power mode = 0		327		
		Static, V_{REF} = 1.5V	Power mode = 3		497		
			Power mode = 2		431		
			Power mode = 1		364		
			Power mode = 0		297		
		Static, V_{REF} = 1.0V	Power mode = 3		407		
			Power mode = 2		361		
			Power mode = 1		304		
			Power mode = 0		284		
Power-On Time		Excluding reference			10		µs

Electrical Characteristics—Internal Voltage Reference

(AVDD = 3.3V, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted. Internal Reference mode, 4.7µF at INT_REF; V_{REF} = 1.5V. T_A = +25°C for typical specifications, unless otherwise noted. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage at INT_REF	V_{INT_REF}	T_A = +25°C	INT_REF 1.024V		1.024		V
			INT_REF 1.50V		1.500		
			INT_REF 2.048V		2.048		
			INT_REF 2.50V		2.500		
Internal Reference Temperature Coefficient	T_{CREF}	T_A = -40°C to +85°C			±50		ppm/°C
Turn-On Time	t_{ON}	GBD			0.1 + (INT_VREF x 1.8)		ms
Leakage Current with INT_REF Output Disabled	I_{INT_REF}	GBD			15	50	nA
INT_REF Line Regulation					±50		µV/V
INT_REF Load Regulation	INT_Load	I_{SOURCE} = 0 to 500µA, T_A = +25°C			10		µV/V
Reference Supply Current		Measured at V_{REF} = 2.5V	Buffer enabled		218		µA

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	f_{SYS_CLK} = 100MHz, $f_{MCK(MAX)} = f_{SYS\_CLK}/2$			50	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Low Idle	t_{MLH}			$t_{MCK}/2$		ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				50	MHz

Electrical Characteristics—SPI (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

Electrical Characteristics—I^2C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics—I²S

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLKS}	96kHz LRCLK frequency			3.072	MHz
Bit Clock Period	t_{BCLKS}		$1/f_{BCLKS}$			ns
BCLK High Time	$t_{WBCLKHS}$			0.5		$1/f_{BCLKS}$
BCLK Low Time	$t_{WBCLKLS}$			0.5		$1/f_{BCLKS}$
LRCLK Setup Time	t_{LRCLK_BCLKS}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDOS}			12		ns
Setup Time for SD (Input)	t_{SU_SDIS}			6		ns
Hold Time SD (Input)	t_{HD_SDIS}			3		ns

Electrical Characteristics—1-Wire Master

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, Long Line mode		85		
		Overdrive		9		

Electrical Characteristics—1-Wire Master (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, Long Line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

Note 1: Gain error does not include zero-scale errors. It is calculated as (full-scale error - offset error).

Note 2: ppmFS is parts per million of full scale.

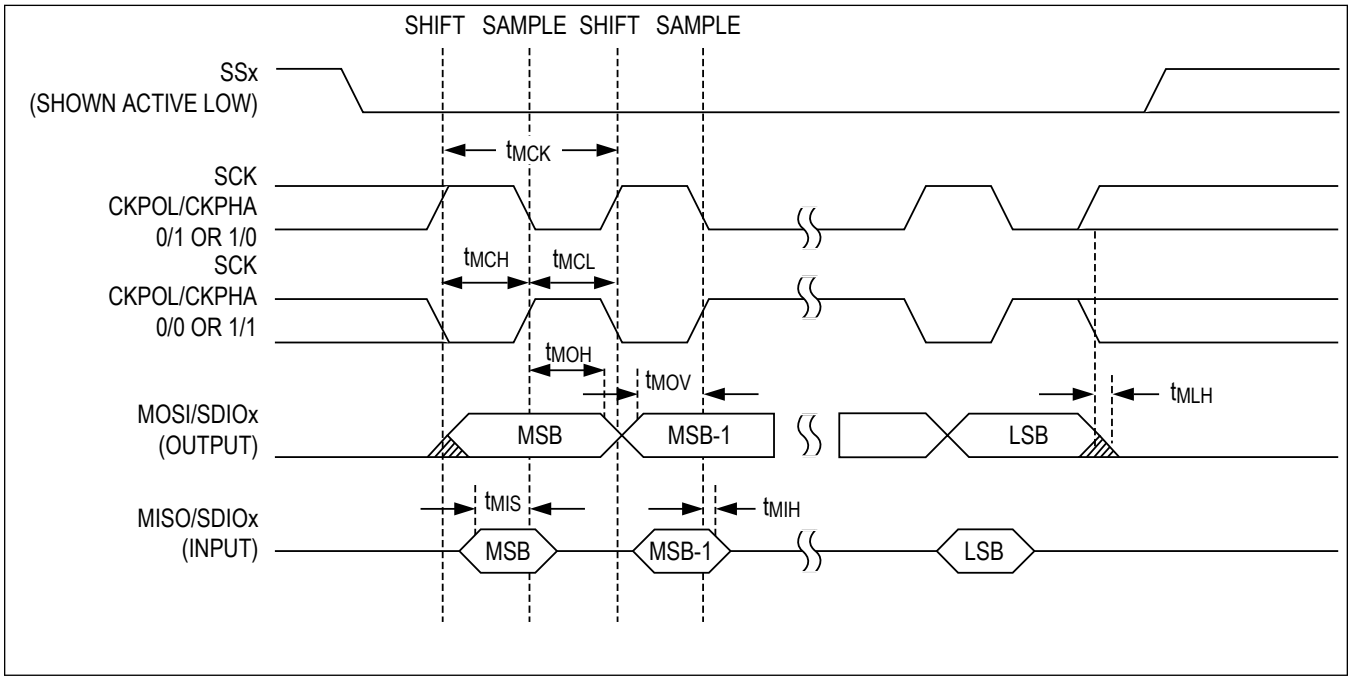


Figure 1. SPI Master Mode Timing Diagram

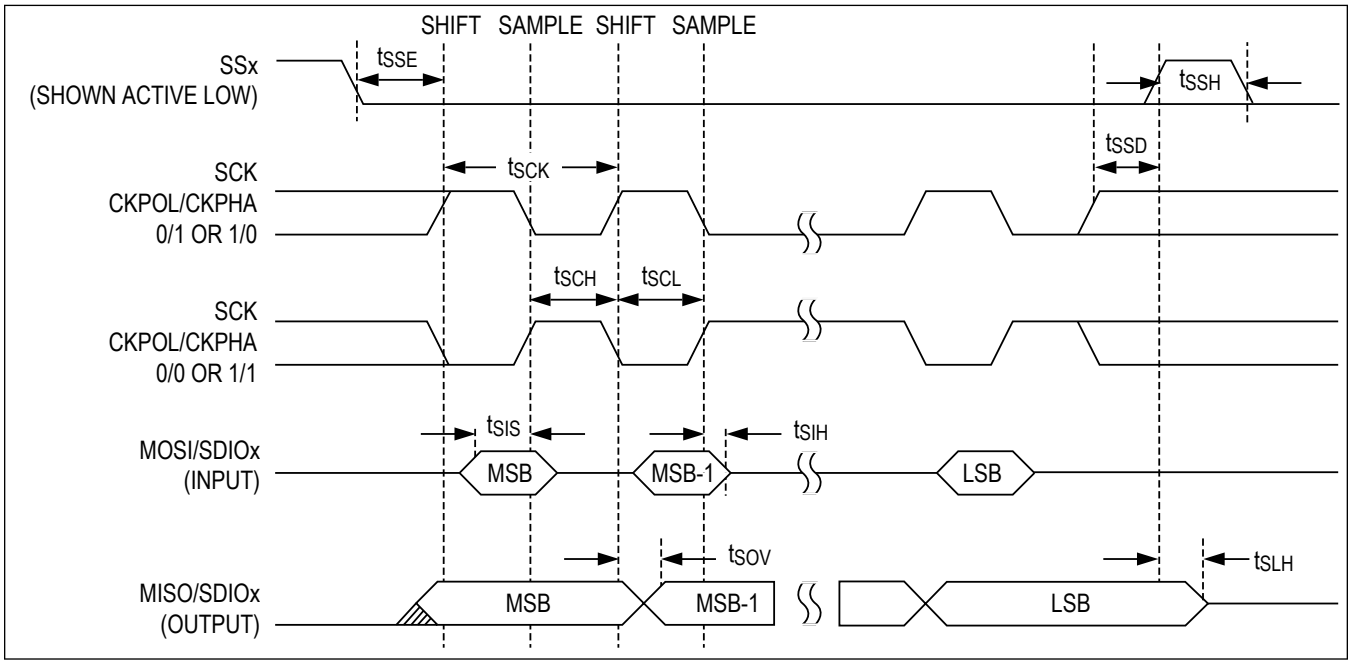


Figure 2. SPI Slave Mode Timing Diagram

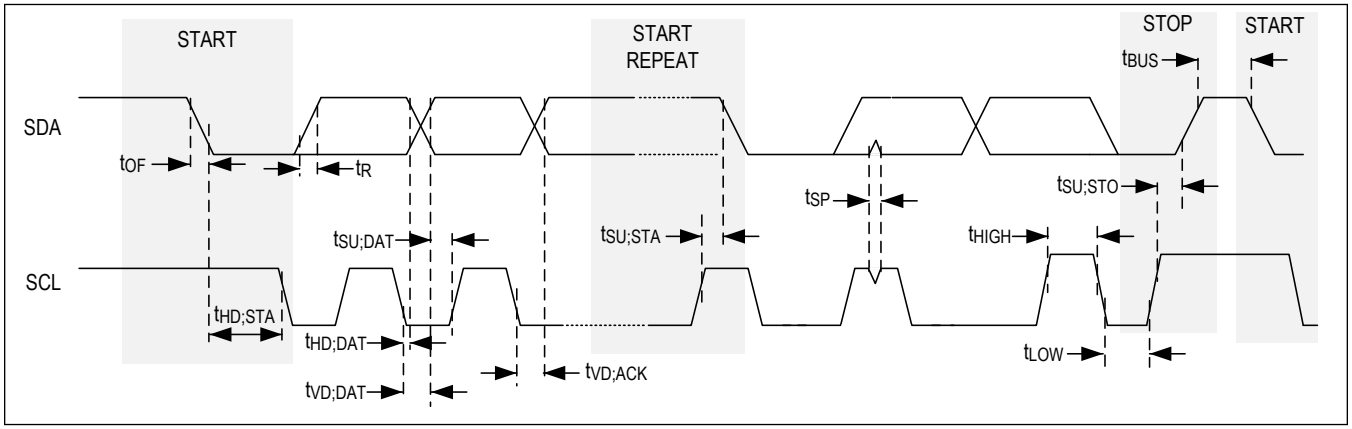


Figure 3. I^2C Timing Diagram

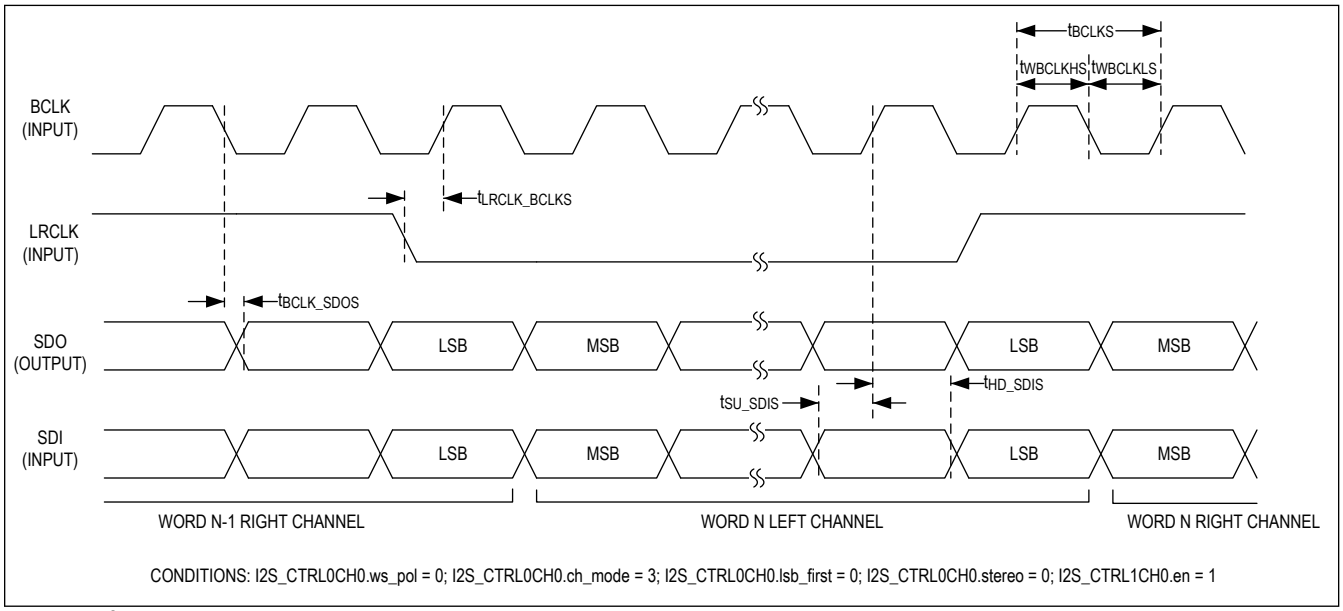


Figure 4. I^2S Timing Diagram

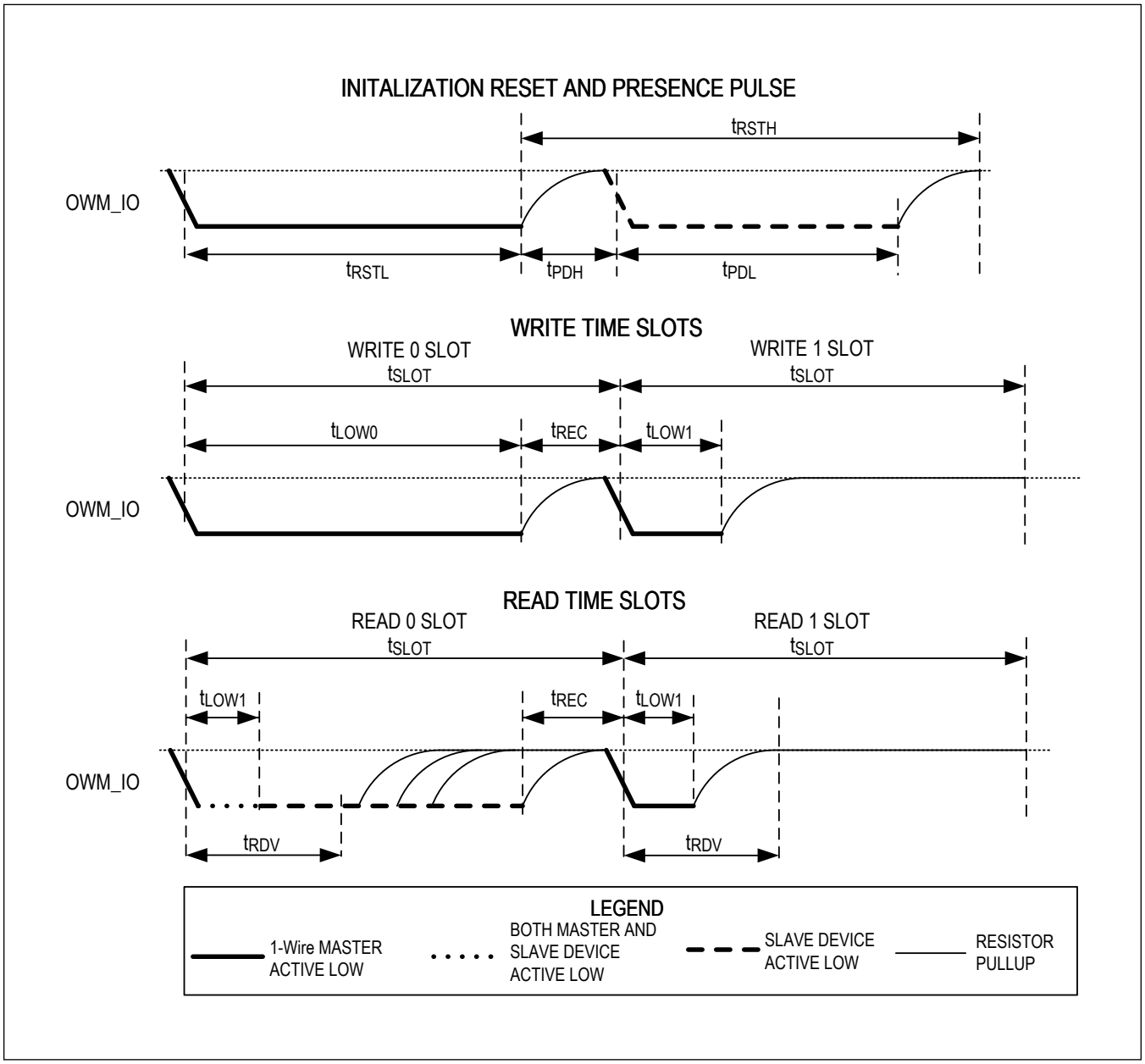
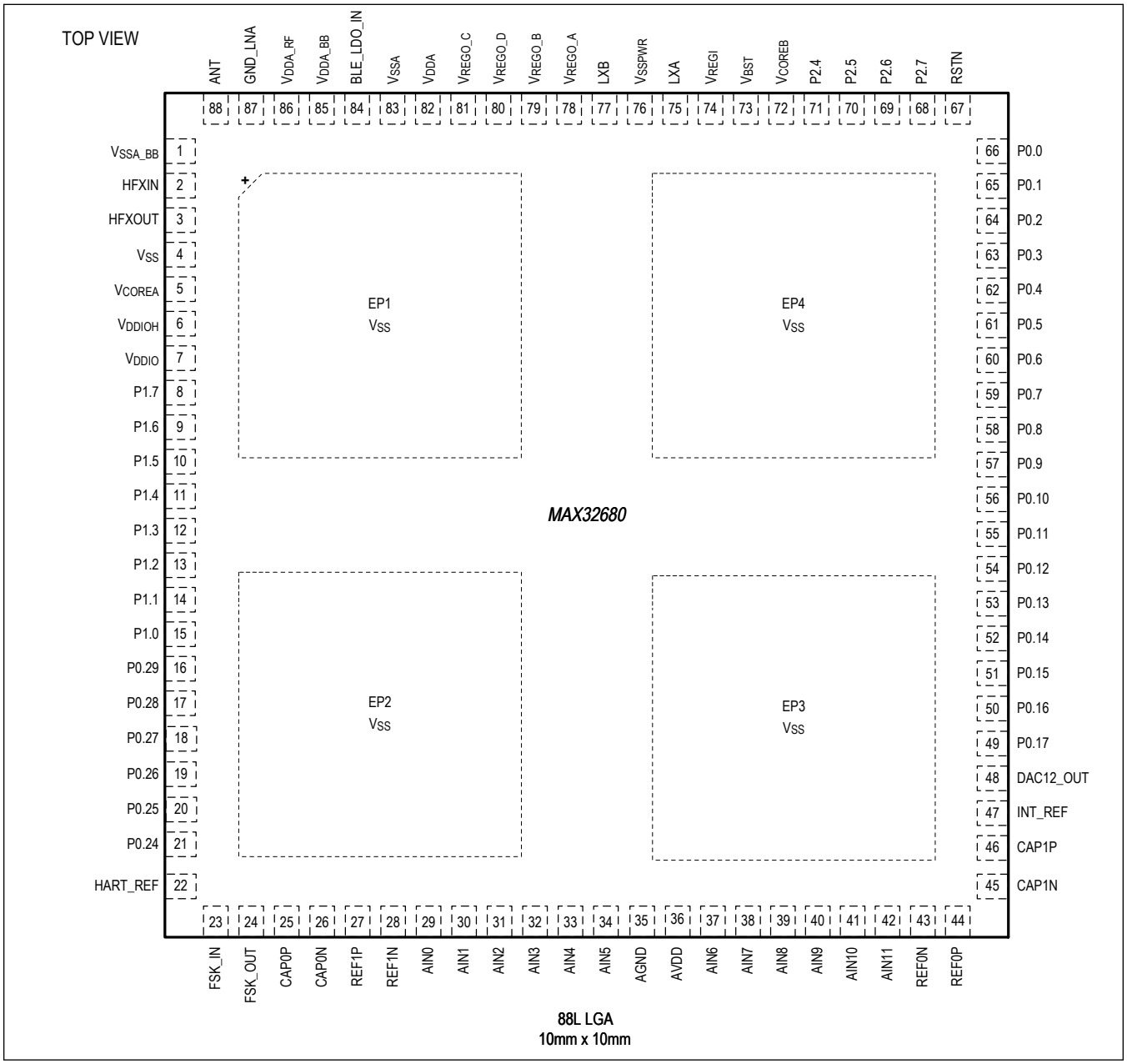


Figure 5. 1-Wire Master Data Timing Diagram

Pin Configuration



88L LGA
10mm x 10mm

Pin Descriptions

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 4	
POWER (See the Applications Information section for bypass capacitor recommendations.)						
74	V_{REGI}	—	—	—	—	Battery Power Supply for the SIMO Switch-Mode Power Supply (SMPS). Bypass device pin C9 with 2 x 47µF capacitors placed as close as possible to the device pin C9 and V_{SSPWR} pins for applications using a coin cell as the battery. See the *Bypass Capacitors* section for more information. If power to the device is cycled, the voltage applied to this device pin must reach V_{REGI} (rising).
84	BLE_LDO_IN	—	—	—	—	Bluetooth LDO Input. Bypass BLE_LDO_IN with a 100nF capacitor to V_{SS} placed as close as possible to the BLE_LDO_IN device pin.
82	V_{DDA}	—	—	—	—	1.8V Analog Power Supply
85	V_{DDA_BB}	—	—	—	—	1.8V Analog Power Supply for the Bluetooth Baseband
86	V_{DDA_RF}	—	—	—	—	1.8V Analog Power Supply for the Bluetooth Radio
5	V_{COREA}	—	—	—	—	Digital Core Supply Voltage A
72	V_{COREB}	—	—	—	—	Digital Core Supply Voltage B
73	V_{BST}	—	—	—	—	Boosted Supply Voltage for the Gate Drive of High-Side Switches. Bypass V_{BST} to LXB with a 3.3nF capacitor.
78	V_{REGO_A}	—	—	—	—	Buck Converter A Voltage Output. Do not connect to external circuits. Bypass V_{REGO_A} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_A} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_A} device pin and the V_{DDA} device pin.
79	V_{REGO_B}	—	—	—	—	Buck Converter B Voltage Output. Do not connect to external circuits. Bypass V_{REGO_B} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_B} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_B} device pin and the closest V_{COREB} device pin.

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 4	
81	V_{REGO_C}	—	—	—	—	Buck Converter C Voltage Output. Do not connect to external circuits. Bypass V_{REGO_C} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_C} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_C} device pin and the closest V_{COREA} device pin.
80	V_{REGO_D}	—	—	—	—	Buck Converter D Voltage Output. Do not connect to external circuits. Bypass V_{REGO_D} with a 22µF capacitor to V_{SS} placed as close as possible to the V_{REGO_D} device pin. This capacitor should be placed on the PCB trace between the V_{REGO_D} device pin and the BLE_LDO_IN device pin.
7	V_{DDIO}	—	—	—	—	GPIO Supply Voltage. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
6	V_{DDIOH}	—	—	—	—	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. Bypass this pin to V_{SS} with a 1.0µF capacitor placed as close as possible to the package.
EP1, EP2, EP3, EP4, 4	V_{SS}	—	—	—	—	Digital Ground/Exposed Pad. This must be connected to V_{SS}. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.
83	V_{SSA}	—	—	—	—	Analog Ground
1	V_{SSA_BB}	—	—	—	—	Bluetooth Baseband Analog Ground
76	V_{SSPWR}	—	—	—	—	Ground for the SIMO SMPS. This device pin is the return path for the the V_{REGI} device pins C6 and C9.
36	AVDD	—	—	—	—	3.0V Analog Power Supply
35	AGND	—	—	—	—	Analog Ground for AVDD
87	GND_LNA	—	—	—	—	Analog Ground
75	LXA	—	—	—	—	Switching Inductor Input A. Connect a 2.2µH inductor between LXA and LXB.
77	LXB	—	—	—	—	Switching Inductor Input B. Connect a 2.2µH inductor between LXA and LXB.
RESET AND CONTROL						
67	RSTN	—	—	—	—	Active-Low, External System Reset Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIOH} supply.

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 4	
CLOCK						
3	HFXOUT	—	—	—	—	32MHz Crystal Oscillator Output
2	HFXIN	—	—	—	—	32MHz Crystal Oscillator Input. Connect a 32MHz crystal between HFXIN and HFXOUT for Bluetooth operation. Optionally, this pin can be configured as the input for an external CMOS-level clock source.
ANTENNA OUTPUT						
88	ANT	—	—	—	—	Antenna for Bluetooth Radio. Attach the single-ended, unbalanced Bluetooth radio antenna.
16-BIT TO 24-BIT Δ-Σ ADC WITH PGA						
44	REF0P	—	—	—	—	Positive Differential Reference 0 Input. REF0P must be more positive than REF0N.
43	REF0N	—	—	—	—	Negative Differential Reference 0 Input. REF0P must be more positive than REF0N.
27	REF1P	—	—	—	—	Positive Differential Reference 1 Input. REF1P must be more positive than REF1N.
28	REF1N	—	—	—	—	Negative Differential Reference 1 Input. REF1P must be more positive than REF1N.
25	CAP0P	—	—	—	—	ADC0 PGA Positive Output. Connect 1nF capacitor across CAP0P and CAP0N.
26	CAP0N	—	—	—	—	ADC0 PGA Negative Output. Connect 1nF capacitor across CAP0P and CAP0N.
46	CAP1P	—	—	—	—	ADC1 PGA Positive Output. Connect 1nF capacitor across CAP1P and CAP1N.
45	CAP1N	—	—	—	—	ADC1 PGA Negative Output. Connect 1nF capacitor across CAP1P and CAP1N.
29	AIN0	—	—	—	—	Channel 0 Analog Input/Positive Differential Reference Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as current source output. When used as a reference input paired with AIN1, AIN0 must be more positive than AIN1.

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 4	
30	AIN1	—	—	—	—	Channel 1 Analog Input/Negative Differential Reference Input. When used as an analog input, may serve as either the positive or negative differential input. May also serve as current source output. When used as a reference input paired with AIN0, AIN0 must be more positive than AIN1.
31	AIN2	—	—	—	—	Channel 2 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
32	AIN3	—	—	—	—	Channel 3 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
33	AIN4	—	—	—	—	Channel 4 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
34	AIN5	—	—	—	—	Channel 5 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
37	AIN6	—	—	—	—	Channel 6 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
38	AIN7	—	—	—	—	Channel 7 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
39	AIN8	—	—	—	—	Channel 8 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
40	AIN9	—	—	—	—	Channel 9 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 4	
41	AIN10	—	—	—	—	Channel 10 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
42	AIN11	—	—	—	—	Channel 11 Analog Input. May serve as either the positive or negative differential input paired with any of the other AINx analog inputs. May also serve as current source output.
12-BIT DAC						
48	DAC12_OUT	—	—	—	—	12-Bit DAC Analog Voltage Output
INTERNAL REFERENCE						
47	INT_REF	—	—	—	—	Internal Reference Output. This reference is used by the 12-bit DAC and the 16-bit to 24-bit ADC0/1. It must be bypassed to V_{SSA} with a 4.7µF capacitor.
GPIO AND ALTERNATE FUNCTION						
66	P0.0	P0.0	UART0A_RX	—	—	UART0 Port Map A Receive
65	P0.1	P0.1	UART0A_TX	—	—	UART0 Port Map A Transmit
64	P0.2	P0.2	TMR0A_IOA	UART0B_CTS	—	Timer 0 I/O 32 Bits or Lower 16 Bits Port Map A; UART0 Clear to Send Port Map B
63	P0.3	P0.3	EXT_CLK/ TMR0A_IOB	—	—	External Clock for Use as SYS_OSC/ Timer 0 Port Map A I/O Upper 16 Bits; UART0 Port Map B Request to Send
62	P0.4	P0.4	SPI0A_SS0	TMR0B_IOAN	—	SPI0 Port Map A Slave Select 0; Timer 0 Port Map B I/O 32 Bits or Lower 16 Bits Inverted Output
61	P0.5	P0.5	SPI0A_MOSI	TMR0B_IOBN	—	SPI0 Port Map A Master-Out Slave-In/ Serial Data 0; Timer 0 Port Map B Upper 16 Bits Inverted Output
60	P0.6	P0.6	SPI0A_MISO	OWM_IO	—	SPI0 Port Map A Master-In Slave-Out/ Serial Data 1; 1-Wire Master Data I/O
59	P0.7	P0.7	SPI0A_SCK	OWM_PE	—	SPI0 Port Map A Clock; 1-Wire Master Pullup Enable Output
58	P0.8	P0.8	SPI0A_SDIO2	TMR0B_IOA	—	SPI0 Port Map A Data 2; Timer 0 Port Map B I/O 32 Bits or Lower 16 Bits
57	P0.9	P0.9	SPI0A_SDIO3	TMR0B_IOB	—	SPI0 Port Map A Data 3; Timer 0 Port Map B I/O Upper 16 Bits
56	P0.10	P0.10	I2C0A_SCL	SPI0B_SS2	—	I2C0 Port Map A Clock; SPI0 Port Map B Slave Select 2
55	P0.11	P0.11	I2C0A_SDA	SPI0B_SS1	—	I2C0 Port Map A Serial Data; SPI0 Port Map B Slave Select 1
54	P0.12	P0.12	UART1A_RX	TMR1B_IOAN	—	UART1 Port Map A Receive; Timer 1 Port Map B 32 Bits or Lower 16 Bits Inverted Output

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 4	
53	P0.13	P0.13	UART1A_TX	TMR1B_IOBN	—	UART1 Port Map A Transmit; Timer 1 Port Map B Upper 16 Bits Inverted Output
52	P0.14	P0.14	TMR1A_IOA	UART1B_CTS	—	Timer 1 Port Map A I/O 32 Bits or Lower 16 Bits; UART1 Port Map B Clear to Send
51	P0.15	P0.15	TMR1A_IOB	UART1B_RTS	—	Timer 1 I/O Port Map A Upper 16 Bits; UART1 Port Map B Request to Send
50	P0.16	P0.16	I2C1A_SCL	PT2	—	I2C1 Port Map A Clock; Pulse Train 2
49	P0.17	P0.17	I2C1A_SDA	PT3	—	I2C1 Port Map A Serial Data; Pulse Train 3
21	P0.24	P0.24	SPI1A_SDIO2	TMR2B_IOA	ADC0_RDY	SPI1 Port Map A Data 2; Timer 2 I/O Port Map B 32 Bits or Lower 16 Bits
20	P0.25	P0.25	SPI1A_SDIO3	TMR2B_IOB	ADC1_RDY	SPI1 Port Map A Data 3; Timer 2 I/O Port Map B Upper 16 Bits
19	P0.26	P0.26	TMR2A_IOA	SPI1B_SS1	—	Timer 2 I/O Port Map A 32 Bits or Lower 16 Bits; SPI1 Port Map B Slave Select 1
18	P0.27	P0.27	TMR2A_IOB	SPI1B_SS2	—	Timer 2 I/O Port Map A Upper 16 Bits; SPI1 Port Map B Slave Select 2
17	P0.28	P0.28	SWDIO	—	—	Serial Wire Debug Data I/O
16	P0.29	P0.29	SWCLK	—	—	Serial Wire Debug Clock
15	P1.0	P1.0	UART2A_RX	RV_TCK	—	UART2 Port Map A Receive; 32-Bit RISC-V Test Port Clock
14	P1.1	P1.1	UART2A_TX	RV_TMS	—	UART2 Port Map A Transmit; 32-Bit RISC-V Test Port Select
13	P1.2	P1.2	I2S0A_SCK	RV_TDI	—	I2S0 Port Map A Bit Clock; 32-Bit RISC-V Test Port Data Input
12	P1.3	P1.3	I2S0A_LRCLK	RV_TDO	—	I2S0 Port Map A Left/Right Clock; 32-Bit RISC-V Test Port Data Output
11	P1.4	P1.4	I2S0A_SDI	TMR3B_IOA	—	I2S0 Port Map A Serial Data Input; Timer 3 I/O Port Map B 32 Bits or Lower 16 Bits
10	P1.5	P1.5	I2S0A_SDO	TMR3B_IOB	—	I2S0 Port Map A Serial Data Output; Timer 3 I/O Upper 16 Bits Port Map B
9	P1.6	P1.6	TMR3A_IOA	BLE_ANT_CTRL2	—	Timer 3 I/O Port Map A 32 Bits or Lower 16 Bits; Bluetooth Antenna Control Line 2
8	P1.7	P1.7	TMR3A_IOB	BLE_ANT_CTRL3	—	Timer 3 I/O Port Map A Upper 16 Bits; Bluetooth Antenna Control Line 3
71	P2.4	P2.4	AIN12/ COMP2N	LPTMR0B_IOA	—	10-Bit Δ-Σ ADC Input 4/Comparator 2 Negative Input; Low-Power Timer 0 I/O Port Map B 32 Bits or Lower 16 Bits
70	P2.5	P2.5	AIN13/ COMP2P	LPTMR1B_IOA	—	10-Bit Δ-Σ ADC Input 5/Comparator 2 Positive Input; Low-Power Timer 1 I/O Port Map B 32 Bits or Lower 16 Bits

PIN	NAME	FUNCTION MODE				FUNCTION
		Primary Signal (Default)	Alternate Function 1	Alternate Function 2	Alternate Function 4	
69	P2.6	P2.6	LPTMR0_CLK/AIN14/ COMP3N	LPUARTB_RX	—	Low-Power Timer 0 External Clock Input/ 10-Bit Δ-Σ ADC Input 6/Comparator 3 Negative Input; Low-Power UART 0 Port Map B Receive
68	P2.7	P2.7	LPTMR1_CLK/AIN15/ COMP3P	LPUARTB_TX	—	Low-Power Timer 1 External Clock Input/ 10-Bit Δ-Σ ADC Input 7/Comparator 3 Positive Input; Low-Power UART 0 Port Map B Transmit
DO NOT CONNECT						
23	FSK_IN	—	—	—	—	Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds.
24	FSK_OUT	—	—	—	—	Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds.
22	HART_REF	—	—	—	—	This pin must be connected to a 0.1µF capacitor.

Detailed Description

The MAX32680 microcontroller (MCU) is an advanced system-on-chip featuring an Arm Cortex-M4F CPU for efficient computation of complex functions and algorithms that is qualified to operate over a temperature range of -40°C to +85°C. The SoC integrates power regulation and management with a SIMO buck regulator system. Onboard is the latest generation Bluetooth 5.2 LE radio, supporting LE Audio, angle of arrival (AoA) and angle of departure (AoD) for direction finding, long-range (coded) modes, and high-throughput modes.

The device offers large onboard memory with 512KB flash and 128KB SRAM, with optional ECC on one 32K SRAM bank. This 32KB bank can be optionally retained in BACKUP mode. An 8KB user OTP area is available, of which 8 bytes are retained even during POWER DOWN mode.

An AFE provides two 12-channel Δ-Σ ADCs with features and specifications that are optimized for precision sensor measurement. Each Δ-Σ ADC can digitize external analog signals as well as system temperature and supplies. An optional PGA with gains of 1x to 32x precedes each ADC. ADC outputs can be optionally converted on the fly from integer to single-precision floating-point format. A 12-bit DAC is also included. The integrated temperature sensor can be used with the internal sense element or an external diode for temperature compensation of sensor outputs. The device also includes a trust protection unit (TPU), providing robust security features such as an AES Engine, TRNG, and secure boot.

Many high-speed interfaces are supported on the device, including SPI, UART, and I^2C serial interfaces, plus one I^2S port for connecting to an audio codec. Additional low-power peripherals include flexible LPTIMER, LPUART, and analog comparators. A four-input, 10-bit ADC is available to monitor analog input from external analog sources.

Arm Cortex-M4 with FPU Processor and RISC-V RV32 Processor

The Arm Cortex-M4 with floating point unit (FPU) processor (CM4) is ideal for low-power system control. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

The Arm Cortex-M4 with FPU DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:

- Four parallel 8-bit add/sub
- Floating point single precision
- Two parallel 16-bit add/sub
- Two parallel MACs
- 32- or 64-bit accumulate
- Signed and unsigned data with or without saturation

The addition of the 32-bit RISC-V coprocessor (RV32) provides the system with ultra-low-power consumption signal processing.

Memory

Internal Flash Memory

512KB of internal flash memory provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 128KB SRAM provides low-power retention of application information in all power modes except POWER DOWN. The SRAM is divided into four banks. SRAM0 and SRAM1 are both 32KB, SRAM2 is 48KB, and SRAM3 is 16KB. SRAM2 and SRAM3 are accessible by the RV32 in LOW POWER mode. For enhanced system reliability, SRAM0 (32KB) can be configured with ECC, single error correction-double error detection (SED-DED). This data-retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining essential data.

Bluetooth 5.2

Bluetooth 5.2 Low Energy Radio

Bluetooth 5.2 LE is the latest version of the Bluetooth wireless communication standard. It is used for wireless headphones and other audio hardware and communication between various smart home and internet of things (IoT) devices. Bluetooth LE communications operate in the unlicensed 2.4GHz industrial-scientific-medical (ISM) band. A frequency-hopping transceiver is used to combat interference and fading. The system operates in the 2.4GHz ISM band at 2400MHz to 2483.5MHz. It uses 40 RF channels that have center frequencies 2402 + k x 2MHz, where k = 0, ..., 39. The Bluetooth stack runs on RV32 so that the CM4 can be freed to run the software. The features of the radio include the following:

- Higher transmit power up to +4.5dbm
- 1Mbps, 2Mbps, and long-range coded (125kbps and 500kbps)
- Increased broadcast capability
  - Advertising packet up to 255 bytes
- On-chip matching network to the antenna
- Antenna control outputs
- Direction finding with AoA and AoD
- Provides hardware on-the-fly encryption and decryption for lower power consumption
- Low transmit current of 4.17mA at 0dbm at 3.3V
- Low receive current of 4.0mA at 3.3V
- Supports mesh networking
- Supports high-quality audio streaming (isochronous)

Bluetooth 5.2 Software Stack

A Bluetooth 5.2 software stack is available for application developers to quickly add support to devices. The Arm Cordio®-B50 software stack is provided in library form and provides application developers access to Bluetooth technology without validation and development of a software stack. The Cordio-B50 software stack interfaces to the Bluetooth link layer running on dedicated hardware. The dedicated hardware for the stack enables the ultimate in power management for IoT applications. Cordio-B50 features the following:

- C library for linking directly into an application development tool
- Change PHY support
  - Host selects the PHY it needs to use at any given time enabling long range or higher bandwidth only when required
    - Bluetooth LE 1M
    - Bluetooth LE Coded S = 2
    - Bluetooth LE Coded S = 8
    - Bluetooth LE 2M
- Bluetooth 5.2 advertising extension support for enabling next-generation Bluetooth beacons
  - Larger packets and advertising channel offloading
  - Packets up to 255 octets long
  - Advertising packet chaining
  - Advertising sets
  - Periodic advertising
  - High-duty cycle, non-connectable advertising
  - Sample applications using standard profiles built on the Cordio-B50 software framework

Comparators

The four AIN[15:12] inputs can be configured as two pairs and deployed as two independent comparators with the following features:

- Comparison events can trigger interrupts
- Events can wake CM4 from SLEEP, LOW POWER, MICRO POWER, STANDBY, or BACKUP operating modes
- Can be active in all power modes

Dynamic Voltage Scaling (DVS) Controller

The DVS controller works using the fixed high-speed oscillator and the V_{COREA} supply voltage to optimally operate the Arm core at the lowest practical voltage. The ability to adaptively adjust the voltage provides a significant reduction in dynamic power consumption.

The DVS controller provides the following features:

- DVS monitoring and adjustment functions
- Continuous monitoring with programmable monitor sample period
- Controlled transition to a programmable operating point
- Independent high and low operating limits for safe, bounded operation
- Independent high, center, and low operating range delay line monitors
- Programmable adjustment rate when an adjustment is required
- Single clock operation
- APB interface provides IP control and status access
- Interrupt capability during error

Clocking Scheme

Multiple clock sources can be selected as the system clock:

- Internal primary oscillator (IPO) at a nominal frequency of 100MHz
- Internal secondary oscillator (ISO) at a nominal frequency of 60MHz
- Configurable internal nanoring oscillator (INRO) at 8kHz, 16kHz, or 30kHz
- Internal baud rate oscillator at 7.3728MHz (IBRO)
- External square-wave clock up to 80MHz
- External RF oscillator at 32MHz (ERFO)—external crystal required

There are multiple external clock inputs:

- LPTMR0 and LPTMR1 can be clocked from unique external sources.
- SYS_CLK can be derived from an external source.

The AFE is configured by SPI1 and is clocked by the built-in Δ-Σ clock generation or the EXT_CLK signal.

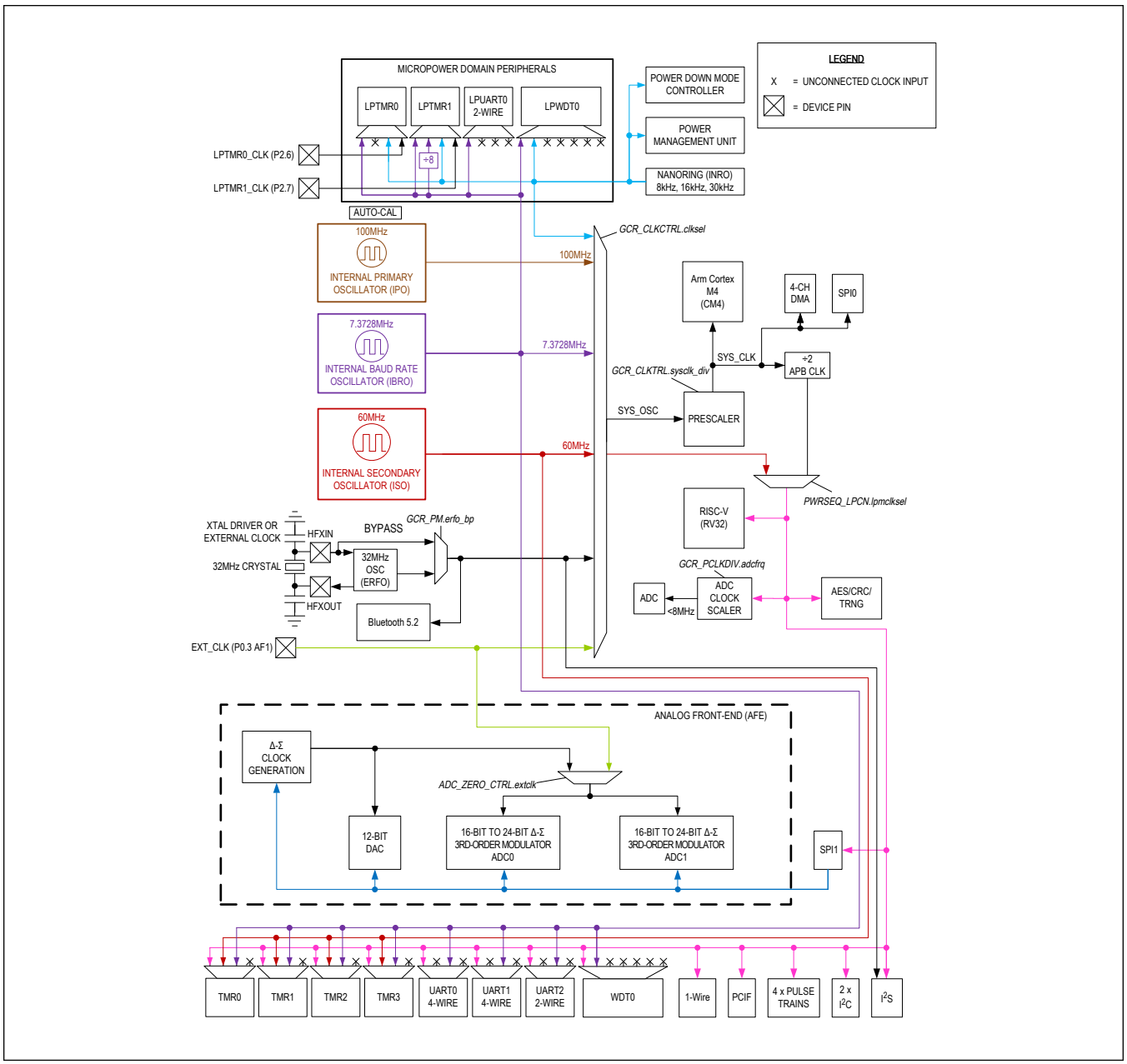


Figure 6. Clocking Scheme Diagram

General-Purpose I/O (GPIO) and Special Function Pins

Most GPIO pins share both a firmware-controlled I/O function and one or more alternate functions associated with peripheral modules. Software can individually enable device pins for GPIO or peripheral alternate function use. Configuring a pin as an alternate function usually supersedes its use as a firmware-controlled I/O. Multiplexing between alternate functions and GPIO can be performed dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or alternate function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be

independently enabled and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector.

When configured as GPIO, all features can be independently enabled or disabled on a per-pin basis. The following features are provided:

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32680 provides up to 36 GPIO pins.

10-Bit ADC for Supply and GPIO Monitoring

The 10-bit Δ-Σ ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from one of the four external analog input signals (AIN15–AIN12) or the internal power supply inputs.

The reference for the ADC can be:

- Internal 1.22V bandgap (V_{BG})
- V_{DDA} analog supply

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel-limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a power mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the CPU is in SLEEP, LOW POWER, or MICRO POWER mode. The four AIN[15:12] inputs can be configured as two pairs and deployed as two independent comparators.

The ADC measures the following voltages:

- AIN[15:12] up to 3.3V
- V_{REGI}
- V_{COREA}
- V_{COREB}
- V_{DDIOH}
- V_{DDIO}
- V_{DDA_RF}
- V_{DDA_BB}
- V_{DDA}

Single-Inductor Multiple-Output (SIMO) Switch-Mode Power Supply (SMPS)

The SIMO SMPS built into the device provides a monolithic power supply architecture for operation from a single lithium (Li+) cell. The SIMO provides four buck regulator outputs that are voltage programmable. This architecture optimizes the power consumption efficiency of the device and minimizes the bill of materials for the circuit design, since only a single inductor/capacitor pair is required.

Power Management

Power Management Unit (PMU)

The PMU provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPUs and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple power domains
- Fast wake-up of powered-down peripherals when activity detected

ACTIVE Mode

In this mode, CM4 and RV32 can execute software, and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low power consumption. CM4 has access to all system SRAM. RV32 has access to SRAM2 and SRAM3. Both CM4 and the RV32 can execute from internal flash simultaneously. SRAM3 can be configured as an instruction cache for RV32.

SLEEP Mode

This mode consumes less power, but wakes faster because software can optionally enable the clocks.

The device status is as follows:

- CM4 is asleep.
- RV32 is asleep.
- Peripherals are on.
- Standard DMA is available for optional use.

LOW POWER Mode (LPM)

This mode is suitable for running the RV32 processor to collect and move data from enabled peripherals.

The device status is a follows:

- The CM4, SRAM0, and SRAM1 are in state retention.
- The RV32 can access the SPI, all UARTS, all timers, I^2C, 1-Wire, pulse train engines, I^2S, CRC, AES, TRNG, PCIF, and comparators, as well as SRAM2 and SRAM3. SRAM3 can be configured to operate as an RV32 instruction cache.
- The transition from LOW POWER mode to ACTIVE mode is faster than the transition from BACKUP mode because system initialization is not required.
- The DMA can access flash.
- IPO can be optionally powered down.
- The following oscillators are enabled:
  - IBRO
  - ERTCO
  - INRO
  - ISO
  - ERFO

MICRO POWER Mode (UPM)

This mode is used for extremely low power consumption while using a minimal set of peripherals to provide the wake-up capability.

The device status is a follows:

- Both CM4 and RV32 are state retained. (System state and all SRAM is maintained.)
- The GPIO pins retain their state.
- All non-MICRO POWER peripherals are state retained.
- IBRO can be optionally powered down.
- The following oscillators are powered down:
  - IPO
  - ISO
  - ERFO
- The following oscillators are enabled:
  - IBRO
  - ERTCO
  - INRO
- The following MICRO POWER mode peripherals are available for use to wake up the device:
  - LPUART0, LPUART1
  - WDT1
  - All four low-power analog comparators

STANDBY Mode

This mode is used to maintain the system operation while keeping time with the RTC.

The device status is as follows:

- Both CM4 and RV32 are state retained. (System state and all SRAM is maintained.)
- The GPIO pins retain their state.
- RTC is on.
- All peripherals are state retained.
- The following oscillators are powered down:
  - IPO
  - ISO
  - IBRO
  - ERFO
- The following oscillators are enabled:
  - ERTCO
  - INRO

BACKUP Mode

This mode is used to maintain the system RAM. The device status is as follows:

- CM4 and RV32 are powered off.
- SRAM0, SRAM1, SRAM2, and SRAM3 can be configured to be state retained as per Table 1.
- All peripherals are powered off.
- The GPIO pins retain their state.
- RTC is on.
- The following oscillators are powered down:
  - IPO
  - ISO
  - IBRO
  - INRO
  - ERFO
- The following oscillators are enabled:
  - ERTCO

Table 1. BACKUP Mode SRAM Retention

RAM BLOCK	RAM SIZE
SRAM0	32KB + ECC
SRAM1	32KB
SRAM2	48KB
SRAM3	16KB

POWER DOWN Mode (PDM)

This mode is used during product level distribution and storage.

The device status is as follows:

- CM4 and RV32 are powered off.
- All peripherals and SRAM are powered down.
- All oscillators are powered down.
- Eight bytes of OTP data are retained.
- Values in the flash are preserved.
- Voltage monitors are operational.

Wake-Up Sources

The wake-up sources from the SLEEP, LOW POWER, MICRO POWER, STANDBY, BACKUP, and POWER DOWN operating modes are summarized in Table 2.

Table 2. Wake-Up Sources

OPERATING MODE	WAKE-UP SOURCE
SLEEP	Any enabled peripheral with interrupt capability; RSTN
LOW POWER (LPM)	SPI0, I2S, I2C, UARTs, timers, watchdog timers, wake-up timer, all comparators, RTC, GPIOs, RSTN, and RV32
MICRO POWER (UPM)	All comparators, LPUART, LPTMR1, LPTIMER2, LPWDT0, RTC, wake-up timer, GPIOs, and RSTN
STANDBY	RTC, wake-up timer, GPIOs, CMP0, and RSTN
BACKUP	RTC, wake-up timer, GPIOs, CMP0, and RSTN
POWER DOWN (PDM)	RSTN

Standard DMA Controller

The standard DMA controller allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 4-channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO, followed immediately by an AHB burst write from the FIFO.

The MAX32680 provides one instance of the standard DMA controller.

Programmable Timers

32-Bit Timer/Counter/PWM (TMR, LPTMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generate pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down auto-reload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- TMR0–TMR3 can be configured as two 16-bit general-purpose timers
- Timer interrupt

The MAX32680 provides six 32-bit timers (TMR0, TMR1, TMR2, TMR3, LPTMR0, and LPTMR1). LPTMR0 and LPTMR1 are capable of operation in the SLEEP, LOW POWER, and MICRO POWER modes.

I/O functionality is supported for all of the timers. Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration. See Table 3 for individual timer features.

Table 3. Timer Configuration Options

INSTANCE	REGISTER ACCESS NAME	SINGLE 32 BIT	DUAL 16 BIT	SINGLE 16 BIT	POWER MODE	CLOCK SOURCE					
						PCLK	ISO	IBRO	INRO	LPTMR0_CLK	LPTMR1_CLK
TMR0	TMR0	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	No	No
TMR1	TMR1	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	No	No
TMR2	TMR2	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	No	No
TMR3	TMR3	Yes	Yes	No	ACTIVE, SLEEP, LOW POWER	Yes	Yes	Yes	No	No	No
LPTMR0	TMR4	No	No	Yes	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	No	Yes	Yes	Yes	No
LPTMR1	TMR5	No	No	Yes	ACTIVE, SLEEP, LOW POWER, MICRO POWER	No	No	Yes	Yes	No	Yes

Watchdog Timer (WDT)

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the windowed WDT, which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution. The windowed timeout period feature provides more detailed monitoring of system operation, requiring the WDT to be reset within a specific time window. See Table 4 for individual timer features.

The MAX32680 provides two instances of the watchdog timer—WDT0 and LPWDT0.

Table 4. Watchdog Timer Configuration Options

INSTANCE NAME	REGISTER ACCESS NAME	POWER MODE	CLOCK SOURCE		
			PCLK	IBRO	INRO
WDT0	WDT0	ACTIVE SLEEP LOW POWER	Yes	Yes	No

Table 4. Watchdog Timer Configuration Options (continued)

LPWDT0	WDT1	ACTIVE SLEEP LOW POWER MICRO POWER	No	Yes	Yes

Pulse Train Engine (PT)

Multiple, independent pulse train generators can provide either a square wave or a repeating pattern from 2 to 32 bits in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level allowing for multibit patterns. Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Safe enable and disable for pulse trains without bit banding
- Multiple pin configurations allow for a flexible layout
- Software can start/synchronize pulse trains independently or as a group
- The frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the pulse train module clock
- The pulse train module clock can be optionally configured by software to be independent of the system AHB clock
- Multiple repetition options
  - Single-shot mode (nonrepeating pattern of 2 to 32 bits)
  - Pattern mode repeats a user-configurable number of times or indefinitely
  - Termination of one pulse train loop count can restart one or more other pulse trains

The pulse train engine feature is an alternate function associated with a GPIO pin. In most cases, enabling the pulse train engine function supersedes the GPIO function.

The MAX32680 provides up to two instances of the pulse train engine peripheral (PT[3:2]).

Serial Peripherals

I2C Interface (I2C)

The I2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many, or many-to-many communications medium. This interface supports standard-mode, fast-mode, fast-mode plus, and high-speed mode I2C speeds. It provides the following features:

- Master or slave mode operation
  - Supports up to four different slave addresses in slave mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1000kbps
  - High-speed mode: 3.4Mbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32680 provides two instances of the I2C peripheral—I2C0, and I2C1.

I²S Interface (I2S)

The I²S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996. It provides the following features:

- Master and slave mode operation
- Support for 4 channels
- 8, 16, 24, and 32-bit frames
- Receive and transmit DMA support
- Wakeup on FIFO status (full/empty/threshold)
- Pulse density modulation support for the receive channel
- Word-select polarity control
- First-bit position selection
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32680 provides one instance of the I²S peripheral (I2S0).

Serial Peripheral Interface (SPI)

The SPI is a highly configurable, flexible, and efficient synchronous interface where multiple SPI devices can coexist on a single bus. The bus uses a single clock signal and numerous data signals, and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and offer the following features:

- SPI modes 0, 1, 2, or 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad data modes supported
- Multiple slave selects on some instances
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and de-assertion timing for leading/trailing SCK edge

The MAX32680 provides one instance of the SPI peripheral—SPI0. See Table 5 for configuration options.

Table 5. SPI Configuration Options

INSTANCE	DATA	SLAVE SELECT LINES	MAXIMUM FREQUENCY MASTER MODE (MHz)	MAXIMUM FREQUENCY SLAVE MODE (MHz)
SPI0	3-wire, 4-wire, dual, or quad data support	3	50	50

UART (UART, LPUART)

The universal asynchronous receiver-transmitter (UART, LPUART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) flow control signaling. Each instance is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun, and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th-bit parity support
- Multidrop support

- Start/stop bit support
- Hardware flow control using RTS/CTS
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32680 provides four instances of the UART peripheral—UART0, UART1, UART2, and LPUART0. LPUART0 is capable of operation in the SLEEP, LOW POWER, and MICRO POWER modes. See Table 6 for configuration options.

Table 6. UART Configuration Options

INSTANCE NAME	REGISTER ACCESS NAME	HARDWARE FLOW CONTROL	POWER MODE	CLOCK SOURCE	
				PCLK	IBRO
UART0	UART0	Yes	ACTIVE SLEEP LOW POWER	Yes	Yes
UART1	UART1	Yes	ACTIVE SLEEP LOW POWER	Yes	Yes
UART2	UART2	No	ACTIVE SLEEP LOW POWER	Yes	Yes
LPUART0	UART3	No	ACTIVE SLEEP LOW POWER MICRO POWER	No	Yes

1-Wire Master (OWM)

Maxim's 1-Wire bus consists of one signal that carries data and supplies power to the slave devices and a ground return. The bus master communicates serially with one or more slave devices through the bidirectional, multidrop 1-Wire bus. The single-contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire master supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line

The OWM supports both standard (15.6kbps) and overdrive (110kbps) speeds.

16-Bit to 24-Bit Δ-Σ ADC with PGA

A low-power, multichannel, 24-bit Δ-Σ ADC has features and specifications optimized for the precision measurement of sensors and other analog signal sources. The architecture includes a low-noise PGA, low-power input buffers, programmable matched current sources, differential/single-ended input multiplexer, and integrated on-chip oscillator.

- PGA with available gains 1x to 128x
  - Very high input impedance
  - Optimizes overall dynamic range
- Low-power input buffers
  - Provide input isolation
- Selectable reference
  - Internal differential (V_{REF})
  - External differential
- Programmable current sources
  - Bias for resistive sensors
  - 16 current levels available
  - Detection of broken sensor wires
- 12 analog inputs

  - 6 differential or 12 single ended
- Sample rates up to 1920 samples per second
- FIR digital filters
  - Provides single-cycle settling in 16ms
  - 90dB of noise rejection at 50Hz and 60Hz
- On-chip clock source
  - No external components required
- External clock capable
- Sample ready interrupts
  - ADC0_RDY and ADC1_RDY

The MAX32680 provides two instances of this ADC (ADC_ZERO, ADC_ONE) that share the multiplexed 12 analog inputs (AIN0–AIN11).

12-Bit DAC

The 12-bit DAC outputs a single-ended voltage. It can be set independently to generate either a static output voltage or to generate a series of preloaded sample outputs at a specified sample rate.

The 12-bit DAC peripheral support the following features:

- Configurable clock rate and output sample rate
- Selectable output voltage reference
- Can be set to output a static voltage level, a preset number of samples at a configurable sample rate, or samples continuously at a configurable sample rate
- Interpolation filter allows for linearly interpolated output samples to be generated between each pair of output samples (2 to 1, 4 to 1, or 8 to 1)
- DAC output samples are pulled from a FIFO to allow continuous sample output generation

Security

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in a dedicated flash region to protect against tampering. Key generation and storage are transparent to the user.

TRNG Non-Deterministic Random Bit Generator (NDRBG)

The device provides a nondeterministic entropy source that can generate cryptographic seeds or strong encryption keys as part of an overall framework for a secure customer application.

Software can use random numbers to trigger asynchronous events that add complexity to program execution to thwart replay attacks or key-search methodologies.

The TRNG can support the system-level validation of many security standards. Maxim Integrated works directly with the customer's validation laboratory to provide the laboratory with any required information. Contact Maxim Integrated for details of compliance with specific standards.

Cyclic Redundancy Check (CRC) Module

A CRC hardware module provides fast calculations and data integrity checks by application software. It supports a user-defined programmable polynomial up to 32-bits. Direct memory access copies data into the CRC module so that CRC calculations on large memory blocks are performed with minimal CPU intervention. Examples of common polynomials are depicted in Table 7.

Table 7. Common CRC Polynomials

ALGORITHM	POLYNOMIAL EXPRESSION	ORDER	POLYNOMIAL	CHECK
CRC-32-ETHERNET	$x^{32}+ x^{26}+ x^{23}+ x^{22}+ x^{16} + x^{12}+ x^{11}+ x^{10}+ x^{8}+ x^{7}+ x^{5}+ x^{4}+ x^{2}+ x^{1}+ x^{0}$	0xEDB8 8320	LSB	0xDEBB 20E3
CRC-CCITT	$x^{16}+ x^{12} + x^{5} + x^{0}$	0x0000 8408	LSB	0x0000 F0B8
CRC-16	$x^{16}+ x^{15} + x^{2} + x^{0}$	0x0000 A001	LSB	0x0000 B001
USB DATA	$x^{16}+ x^{15} + x^{2}+ x^{0}$	0x8005 0000	LSB	0x800D 0000
PARITY	$x^{1}+ x^{0}$	0x0000 0001	MSB	—

Secure Boot

Following every reset, the device performs a secure boot to confirm that the program memory has come from an authenticated source and has not been modified or corrupted. An ECDSA-256 public key is loaded into nonvolatile memory during the initial configuration. The application binary is created and then signed with the corresponding private key before programming the device memory. Following every reset, the memory contents are checked using the ECDSA-256 key. If the contents are validated, the application software is considered trusted, and the device begins code execution. Programs that fail the integrity check indicate intentionally or unintentionally corrupted or modified program memory. The device then transitions to safe mode, which prevents the execution of the customer code. The device can be reloaded with new trusted program memory signed with the private key during the development phase. The JTAG interface can be disabled before deployment to prevent further modification of the program memory.

Debug and Development Interface (SWD, JTAG)

The serial wire debug (SWD) interface is used for code loading and ICE debug activities for the CM4. The JTAG interface is provided for the RV32. All devices in mass production have the debugging/development interface enabled.

Applications Information

Bypass Capacitors

The proper use of bypass capacitors reduces noise generated by the IC into the ground plane. The *Pin Descriptions* table indicates which pins should be connected to bypass capacitors, and the appropriate ground plane.

It is recommended that one instance of a bypass capacitor should be connected to each pin/ball of the IC package. For example, if the *Pin Descriptions* table shows four device pins associated with voltage supply A, a separate capacitor should be connected to each pin for a total of four capacitors.

Capacitors should be placed as close as possible to their corresponding device pins. Pins that recommend more than one value of capacitor per pin should place them in parallel with the lowest value capacitor first, closest to the pin.

Ordering Information

PART	FLASH	SYSTEM RAM	PIN-PACKAGE
MAX32680GLR+	512KB	128KB	88L LGA
MAX32680GLR+T*	512KB	128KB	88L LGA

T = Tape and reel.

** = Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Initial release	—