AS1925, AS1926

DataSheet

Ultra-Low Voltage Microprocessor Supervisory Circuit with Manual Reset

1 General Description

The AS1925/AS1926 microprocessor supervisory circuits were designed to assert a single reset if the monitored supply voltage drops below its reset threshold or if the manual reset is activated. The reset remains asserted for a fixed timeout delay after VCC has risen above the reset threshold and the manual reset is deasserted.

Their small size, excellent circuit reliability, and low supply current (3.5µA) make the AS1925/AS1926 a very low cost solution by eliminating external components and adjustments when used with low-voltage (+0.9 to +1.5V) systems.

The devices are available as the standard products listed in Table 1.

Table 1. Standard Products

Model	Output Type
AS1925	Active-Low Push/Pull, Active-High Push/Pull
AS1926	Active-High Push/Pull, Active-Low Open-Drain

The active-low open-drain reset output requires a pullup resistor that can be connected to a voltage from 0 to VCC. The reset comparator was specifically designed to ignore fast VCC transients.

The devices are available in a 5-pin SOT23 package.

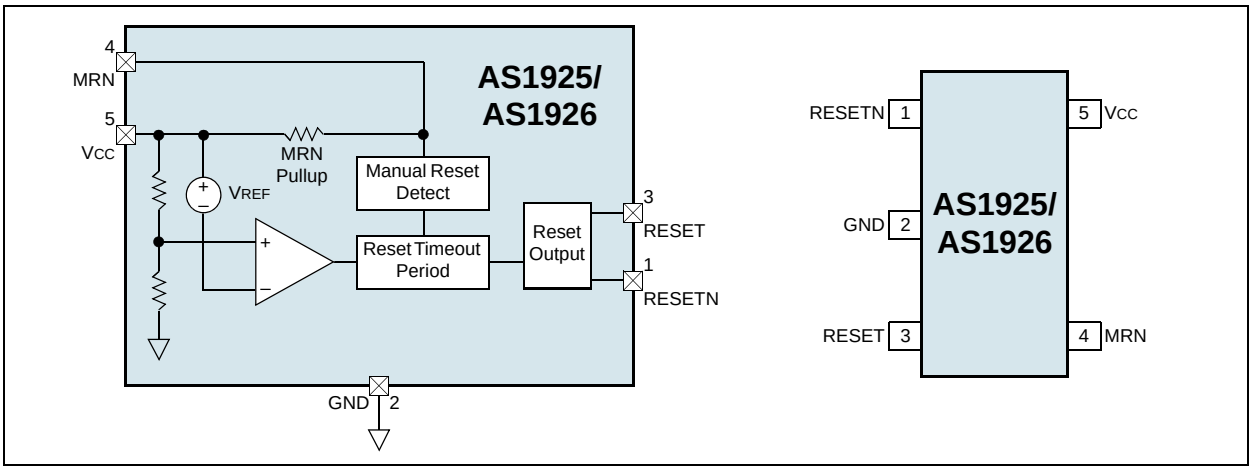
2 Key Features

- Factory-Trimmed Reset Thresholds for Monitoring Supplies from 0.9 to 1.5V
- Low Power Consumption: 3.5µA
- Reset Threshold Accuracy Over Temperature: ±2.5%
- Four Timeout Periods: 1.5ms, 30ms, 210ms, and 1.68s
- Three Reset Output Types:
  - Active-Low Push/Pull
  - Active-High Push/Pull
  - Active Low Open-Drain
- Guaranteed Reset Valid to VCC = 0.55V (Active-Low)
- Manual Reset Input
- Immune to Fast VCC Transients
- 5-pin SOT23 Package

3 Applications

The device is ideal for portable and battery-powered systems, embedded controllers, intelligent instruments, automotive systems, telecommunications equipment, networking equipment, computer workstations and servers, critical CPU monitoring applications, and any low-voltage application.

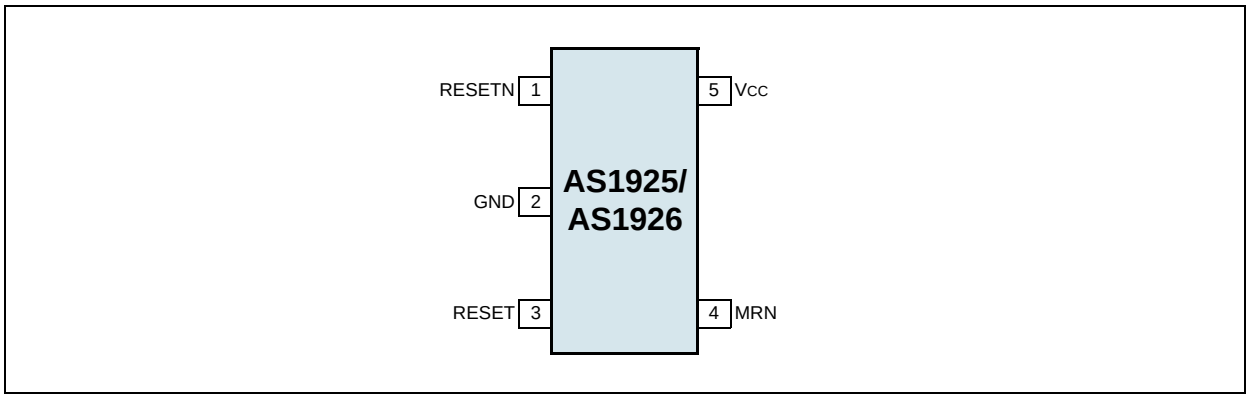
Figure 1. Block Diagram and Pinout



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	RESETN	**Active-Low Reset Output** – AS1925 Push/Pull or AS1926 Open-Drain. RESETN changes from high to low if Vcc drops below the selected reset threshold or MRN is pulled low. RESETN remains low for the reset timeout period (see page 4) after Vcc exceeds the device reset threshold and MRN is released high.
2	GND	**Ground**
3	RESET	**Active-High Push/Pull Reset Output**. RESET changes from low to high when Vcc input drops below the selected reset threshold or MRN is pulled low. RESET remains high for the reset timeout period (see page 4) after Vcc exceeds the device reset threshold and MRN is released high.
4	MRN	**Active-Low Manual Reset Input**. This pin is connected to the internal 20kΩ pullup to Vcc. Pull this pin low to force a reset. The reset remains active as long as MRN is low and for the reset timeout period (see page 4) after MRN goes high. **Note:** If this pin is not used it should be connected to Vcc or left unconnected.
5	Vcc	**Supply Voltage**. Monitored supply voltage.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{CC} to GND	-0.3	+5	V	
MRN, RESETN (Open-Drain) to GND	-0.3	+5	V	
RESETN (Push/Pull), RESET to GND	-0.3	V_{CC} + 0.3	V	
Input Current (All Pins)		20	mA	
RESETN, RESET Output Current		20	mA	
Continuous Power Dissipation (T_{AMB} = +70ºC)		571	mW	Derate 7.1mW/ºC above +70ºC
Operating Temperature Range	-40	+85	ºC	
Junction Temperature		+150	ºC	
Storage Temperature Range	-65	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

V_{CC} = +0.55 to +1.8V, T_{AMB} = -40 to +85ºC (unless otherwise specified). Typ values @ T_{AMB} = +25ºC.

Table 4. Electrical Characteristics

Symbol	Parameter [1]	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage Range [2]		0.75		1.80	V
I_{CC}	Supply Current	V_{CC} = 0.9V, No Load, Reset Not Asserted		3.5	12	µA
		V_{CC} = 1.5V, No Load, Reset Not Asserted		4.5	12	
		V_{CC} = 1.8V, No Load, Reset Not Asserted		5	12	
V_{TH}	Reset Threshold (V_{CC} Falling)	Suffix 14	1.350	1.388	1.425	V
		Suffix 13	1.275	1.313	1.350	
		Suffix 11	1.080	1.110	1.140	
		Suffix 10	1.020	1.050	1.080	
		Suffix 08	0.810	0.833	0.855	
		Suffix 07, T_{AMB} = 0 to +85ºC	0.765	0.788	0.810	
V_{HYS}	Reset Threshold Hysteresis			0.75		%V_{TH}
	V_{CC} to Reset Delay	V_{CC} Falling, Step Signal from (V_{TH} + 10%) to (V_{TH} - 10%) within 1µs		120		µs
t_{RP}	Reset Active Timeout Period	Suffix B	1	1.5	2	ms
		Suffix C	20	30	40	
		Suffix D	140	210	280	
		Suffix E	1120	1680	2240	
V_{IL}	MRN Input Voltage [3]				0.3 × V_{CC}	V
V_{IH}			0.7 × V_{CC}			
	MRN Minimum Input Pulse Width	MRN driven from V_{CC} to 0V [3]	1			µs
	MRN Glitch Rejection	MRN driven from V_{CC} to 0V [3]		150		ns
	MRN to Reset Delay	MRN driven from V_{CC} to 0V [3]		500		ns
	MRN Pullup Resistance to V_{CC}		10	20	26	kΩ
V_{OL}	RESETN Open-Drain Output Voltage	V_{CC} = 0.55V, I_{SINK} = 10µA, Reset Asserted			0.2 × V_{CC}	V
		V_{CC} = 0.83V, I_{SINK} = 80µA, Reset Asserted			0.2 × V_{CC}	
I_{LEAK}	RESETN Open-Drain Output Leakage Current	V_{CC} > VTH, Reset Not Asserted			1	µA
V_{OL}	RESETN Push/Pull Output Voltage	V_{CC} = 0.55V, I_{SINK} = 10µA, Reset Asserted			0.2 × V_{CC}	V
		V_{CC} = 0.83V, I_{SINK} = 80µA, Reset Asserted			0.2 × V_{CC}	
V_{OH}		V_{CC} = 0.83V, I_{SOURCE} = 40µA, Reset Not Asserted	0.8 × V_{CC}			

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter [1]	Conditions	Min	Typ	Max	Units
V_{OH}	RESET Push/Pull Output Voltage	V_{CC} = 0.75V, I_{SOURCE} = 10µA, Reset Asserted	0.8 × V_{CC}			V
		V_{CC} = 0.83V, I_{SOURCE} = 40µA, Reset Asserted	0.8 × V_{CC}			
V_{OL}		V_{CC} = 0.83V, I_{SINK} = 80µA, Reset Not Asserted			0.2 × V_{CC}	

1. 100% production tested at +25ºC. Over-temperature limits are guaranteed by design.
2. The active-low output RESETN $V_{CC(MIN)}$ = 0.55V.
3. For V_{CC} > 0.788V, T_{AMB} = 0 to +85ºC; for V_{CC} > 0.833V, T_{AMB} = -40 to +85ºC.

7 Typical Operating Characteristics

V_{CC} = 1.5V, T_{AMB} = +25ºC (unless otherwise specified).

Figure 3. Supply Current vs. Temperature

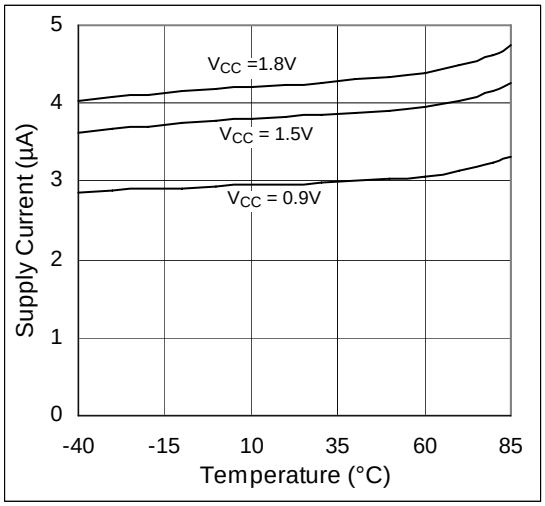


Figure 4. Power Down Reset Delay vs. Temperature

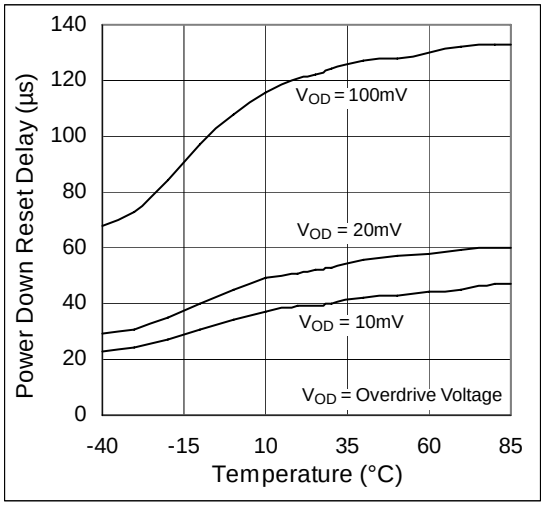


Figure 5. Normalized Reset Timeout Periode vs. Temp.

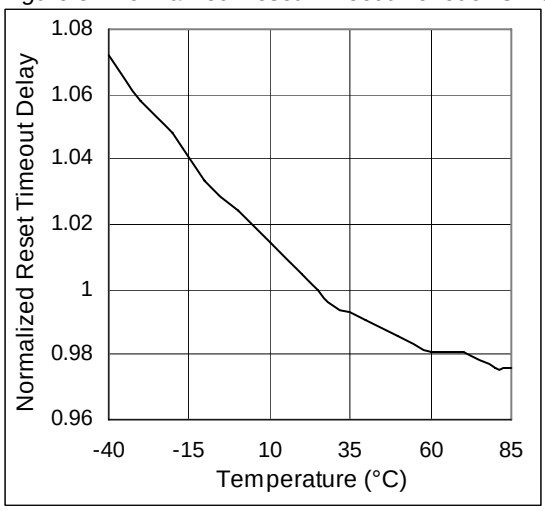


Figure 6. Normalized V_{CC} Reset TH. vs. Temperature

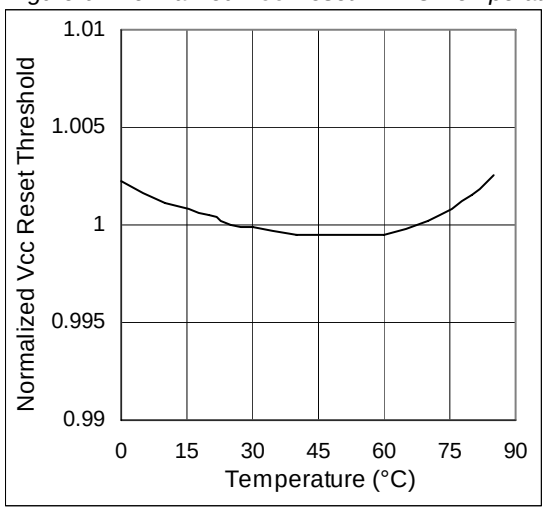


Figure 7. Power-Up/Down Characteristics

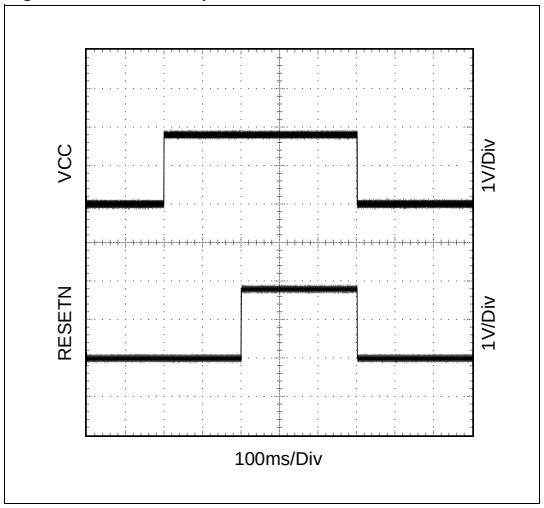
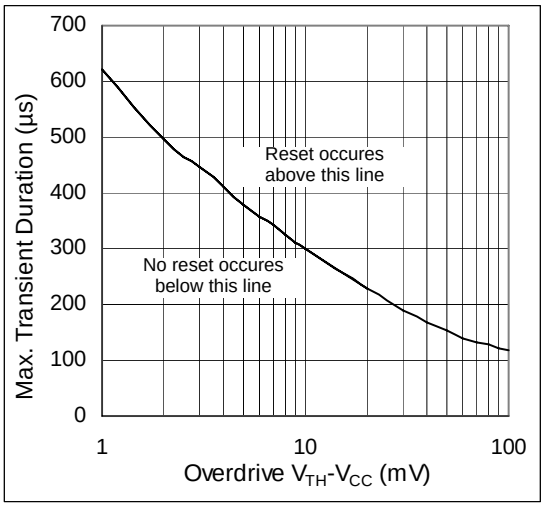


Figure 8. Glitch rejection vs. Supply Voltage



8 Detailed Description

Reset Output

The AS1925/AS1926 assert a reset during power-up, power-down, and brownout conditions if the VCC supply voltage falls below a preset threshold (AS1925/AS1926). The reset remains asserted for a fixed timeout delay (see page 4) once VCC has stabilized.

The devices are available with four timeout options: 1.5ms, 30ms, 210ms, and 1.68s.

The AS1925/AS1926 have two reset outputs (RESETN and RESET); RESETN is the inverse of RESET. The AS1925 has an active-high push/pull output and an active-low push/pull output. The AS1926 has an active-high push/pull output and an active-low open-drain output.

Manual Reset Input

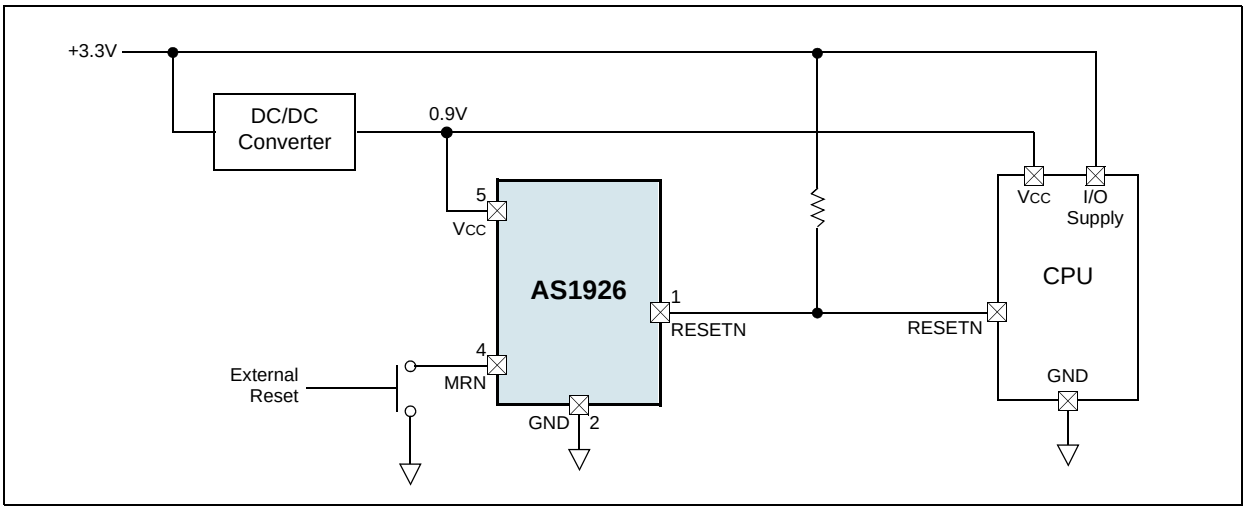
The devices feature a manual reset input (MRN). When pin MRN is pulled low, a reset is asserted and the reset remains asserted as long as MRN is kept low, and for a fixed timeout delay after MRN goes high. MRN is connected to an internal 20kΩ pullup resistor, thus this pin can be left open if it is not used.

MRN can be driven with CMOS logic-level or with open-drain/collector outputs.

To create a manual reset circuit, connect a normally open momentary switch from MRN to ground (see Figure 9 on page 8). External debounce circuitry is not required. If pin MRN is driven via long cables or the device is used in a noisy environment, a 0.1µF capacitor from MRN to ground will provide additional noise immunity.

9 Application Information

Figure 9. Typical Application Diagram



Fast Transient Immunity

The AS1925/AS1926 are virtually immune to fast, falling VCC transients. Figure 8 on page 6 shows typical transient duration versus reset comparator overdrive, for which the devices do not generate a reset pulse. The graph was generated using a falling pulse applied to VCC, starting 0.1V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width that a falling VCC transient can have without causing a reset pulse. As the magnitude of the transient goes further below the reset threshold, the maximum allowable pulse width decreases.

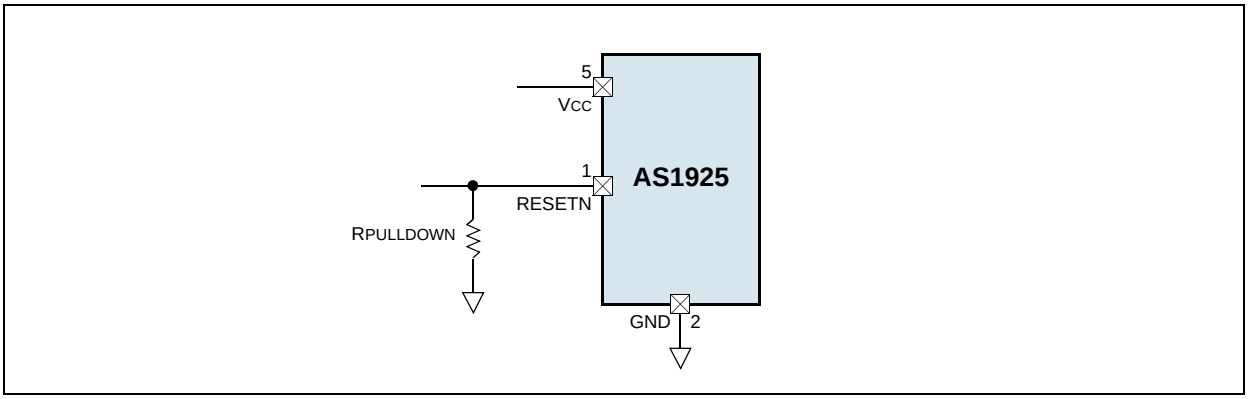
Note: For additional transient immunity, place a 0.1µF bypass capacitor as close as is practical to pin VCC.

Ensuring a Valid Reset Output Down to 0V

If VCC falls below 0.55V, the AS1925 push/pull RESETN output will no longer sink current and becomes an open circuit, which means that high-impedance CMOS-logic inputs connected to RESETN can drift to undetermined voltages. This is not relevant for most applications since most microprocessors and other circuits do not operate with a supply voltage < 0.55V.

In systems where RESETN must be valid down to 0V, adding a pulldown resistor to RESETN (see Figure 10) causes any stray leakage currents to flow to ground, holding RESETN low. The value of the pulldown resistor is not critical; a 200kΩ resistor is large enough not to load RESETN and small enough to pull RESETN to ground.

Figure 10. Reset Valid to VCC = 0V

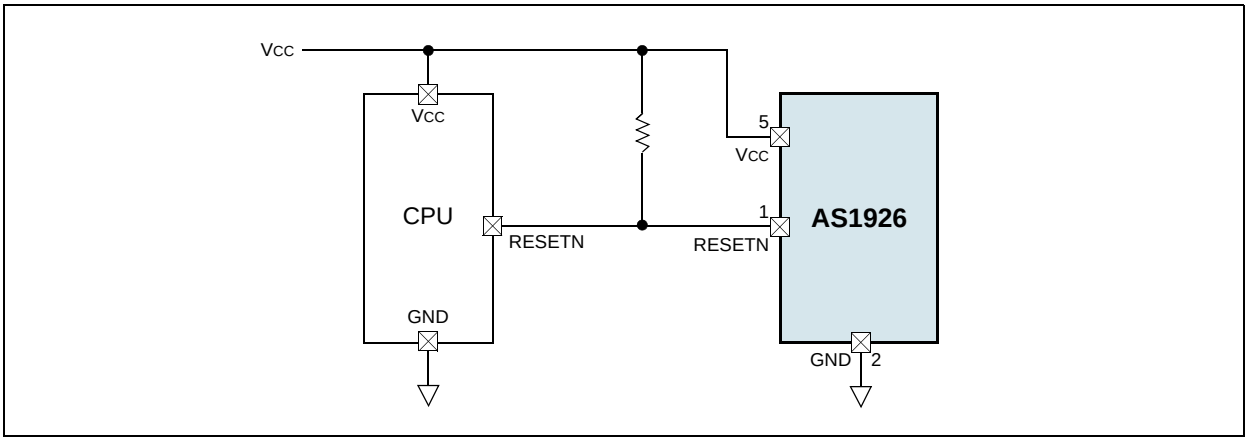


Note: A 200kΩ pullup resistor to VCC is also recommended if the push/pull RESET is required to remain valid for VCC 0.75V.

Interfacing to Bi-Directional Microprocessor Reset Pins

Because the RESETN output of the AS1926 is open drain, this device interfaces easily with microprocessors that have bidirectional reset pins. Connecting the AS1926 RESETN output directly to the microprocessor RESETN pin with a single pullup resistor allows either device to assert reset (Figure 11 on page 9).

Figure 11. Interfacing to Microprocessors with Bidirectional Reset Pins

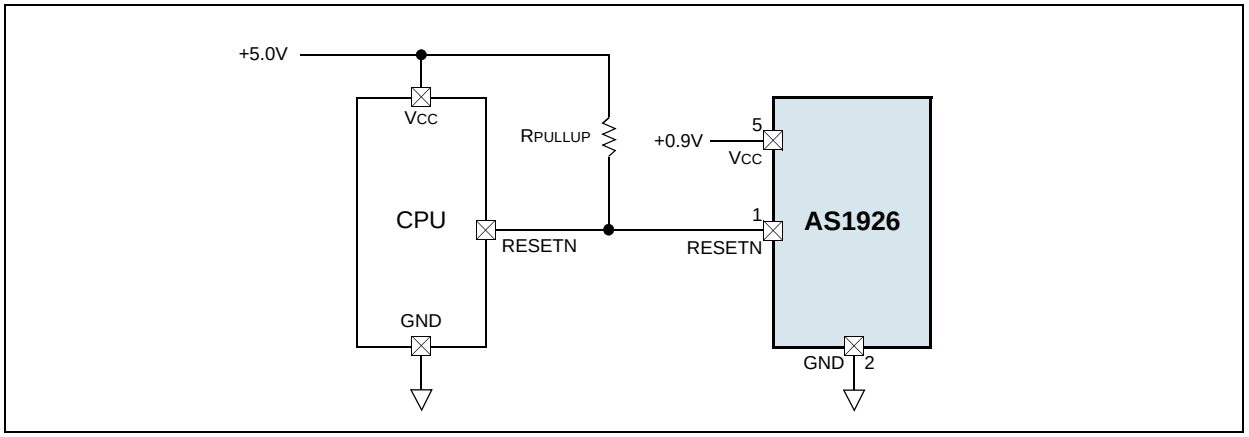


Using the AS1926 Open-Drain RESETN Output with Multiple Supplies

In a typical application, the pullup resistor connected to the AS1926 connects to the voltage being monitored at pin VCC. However, some systems use an open-drain output to level-shift from the monitored supply to reset circuitry powered by another supply (see Figure 12).

As VCC decreases, so does the ability of the AS1926 to sink current at RESETN. RESETN is pulled high as VCC decreases toward 0V. The voltage where this occurs depends on the value of the pullup resistor and the supply voltage to which it is connected.

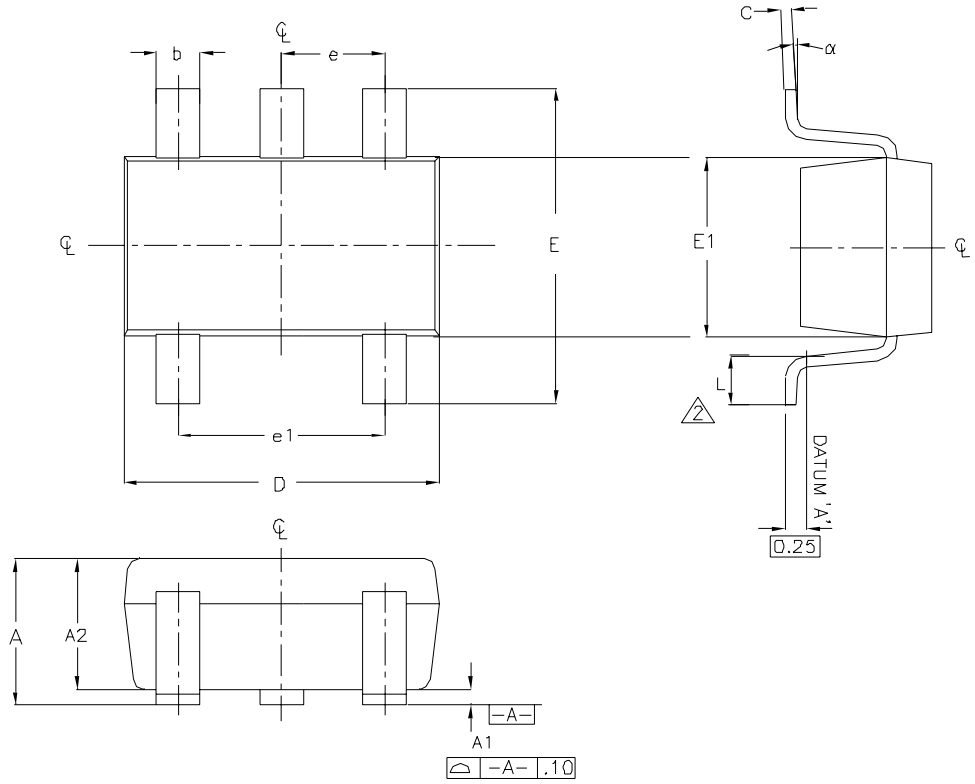
Figure 12. AS1926 Open-Drain RESETN Output with Multiple Supplies



10 Package Drawings and Markings

The AS1925/AS1926 are available in an 5-pin SOT23 package.

Figure 13. 5-pin SOT23 Package



Notes:

1. All dimensions are in millimeters.
2. Foot length is measured at the intercept point between datum A and lead surface.
3. Package outline exclusive of mold flash and metal burr.
4. Package outline inclusive of solder plating.
5. Complies with *EIAJ SC74*.
6. Package ST003 Revision A supercedes SOT34-D-2005 Revision C.

Symbol	Min	Max
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
C	0.09	0.20
D	2.80	3.05
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.55
e	0.95 Ref	
e1	1.90 Ref	
α	0º	8º

11 Ordering Information

The AS1925/AS1926 are available as the standard products shown in Table 5.

Table 5. Ordering Information

Model	Description	Timeout Period	Delivery Form	Package
AS1925-BSTT-xyy[1]	Ultra-Low Reset Threshold with Manual Reset		Tape and Reel	5-pin SOT23
AS1925-BSTT-D07	Ultra-Low Reset Threshold (0.81V) with Manual Reset	140ms Reset	Tape and Reel	5-pin SOT23
AS1926-BSTT-D07	Ultra-Low Reset Threshold (0.81V) with Manual Reset, Open-Drain	140ms Reset	Tape and Reel	5-pin SOT23

1. *xx and y* is a placeholder for variants, e.g., AS1926-BSTT-D07 offers 0.81V (max) reset threshold and a 140ms minimum timeout periode (see Table 6).
Available upon request. Contact austriamicrosystems, AG for more information.

Table 6. Model Variants

Suffix (x)	Reset timout (ms)				Suffix (yy)	Reset Threshold (V)		
	min	typ	max			min	typ	max
B	1	1.5	2		14	1.350	1.388	1.425
C	20	30	40		13	1.275	1.313	1.350
D	140	210	280		11	1.080	1.110	1.140
E	1120	1680	2240		10	1.020	1.050	1.080
					08	0.810	0.833	0.855
					07	0.765	0.788	0.810

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