

## Applications

- Wearable
- Activity tracker
- Smartwatch
- Smartglasses

## Features

- Operating voltage range 2 V to 5.5 V
- Low supply current 1  $\mu$ A
- Integrated test mode
- Single Smart Reset™ push-button input with fixed extended reset setup delay ( $t_{SRC}$ ) from 0.5 s to 10 s in 0.5 s steps (typ.), option with internal input pull-up resistor
- Push-button controlled reset pulse duration
  - Option 1: fully push-button controlled, no fixed or minimum pulse width guaranteed
  - Option 2: defined output reset pulse duration ( $t_{REC}$ ), factory-programmed
- Single reset output
  - Active low or active high
  - Push-pull or open drain with optional pull-up resistor
- Fixed Smart Reset input logic voltage levels
- Operating temperature: -40 °C to +85 °C
- UDFN6 package 1.00 mm x 1.45 mm
- ECOPACK®2 (RoHS compliant, Halogen-Free)

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# 1 Description

The Smart Reset™ devices provide a useful feature which ensures that inadvertent short reset push-button closures do not cause system resets. This is done by implementing an extended Smart Reset input delay time ( $t_{SRC}$ ), which ensures a safe reset and eliminates the need for a specific dedicated reset button.

This reset configuration provides versatility and allows the application to distinguish between a software generated interrupt and a hard system reset. When the input push-button is connected to the microcontroller interrupt input, and is closed for a short time, the processor can only be interrupted. If the system still does not respond properly, continuing to keep the push-button closed for the extended setup time  $t_{SRC}$  causes a hard reset of the processor through the reset output.

The SR1 has one Smart Reset input ( $\overline{SR}$ ) with preset delayed Smart Reset setup time ( $t_{SRC}$ ). The reset output ( $\overline{RST}$ ) is asserted after the Smart Reset input is held active for the selected  $t_{SRC}$  delay time. The  $\overline{RST}$  output remains asserted either until the  $\overline{SR}$  input goes to inactive logic level (i.e. neither fixed nor minimum reset pulse width is set) or the output reset pulse duration is fixed for  $t_{REC}$  (i.e. factory-programmed). The device fully operates over a broad  $V_{CC}$  range from 2.0 V to 5.5 V.

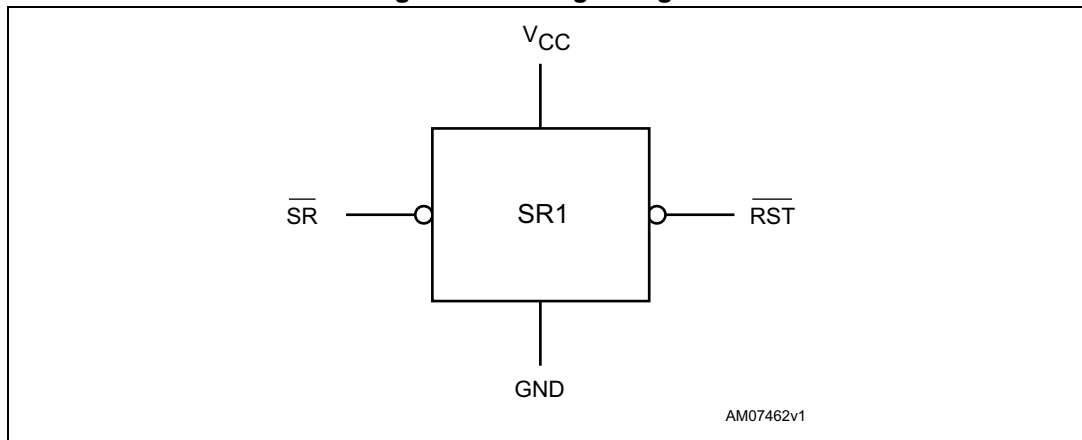
## 1.1 Test mode

After pulling  $\overline{SR}$  up to  $V_{TEST}$  ( $V_{CC} + 1.4$  V) or above, the counter starts to count the initial shortened  $t_{SRC-INI}$  (42 ms, typ.). After  $t_{SRC-INI}$  expires, the  $\overline{RST}$  output either goes down for  $t_{REC}$  (if  $t_{REC}$  option is used) or stays low as long as overvoltage on  $\overline{SR}$  is detected (if  $t_{REC}$  option is not used). This is feedback, and the user only knows that the device is locked in test mode. Each time the  $\overline{SR}$  input is connected to ground in test mode, a shortened  $t_{SRC-SHORT}$  ( $t_{SRC}/128$ ) is used instead of regular  $t_{SRC}$  (0.5 s - 10 s). In this way the device can be quickly tested without repeating test mode triggering. Return to normal mode is possible by performing a new startup of the device (i.e.  $V_{CC}$  goes to 0 V and back to its original state).

The advantages of this solution are its high glitch immunity, user feedback regarding entry into test mode, and testability within the full  $V_{CC}$  range.

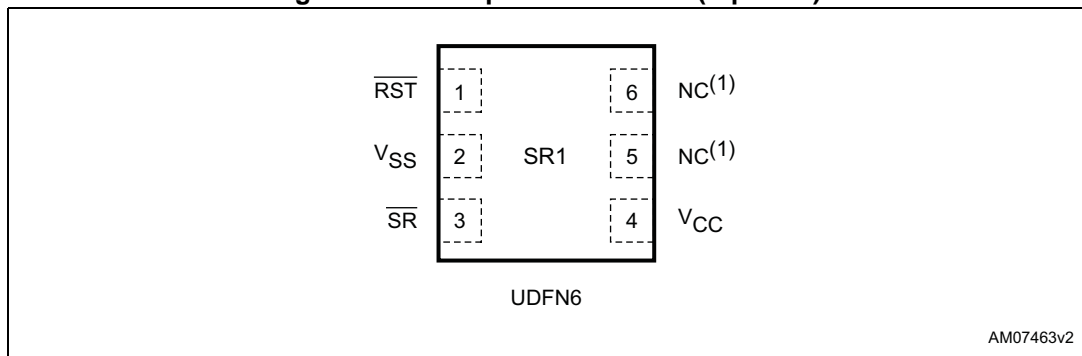
## 1.2 Logic diagram

Figure 1. SR1 logic diagram



## 1.3 Pin connections

Figure 2. UDFN6 pin connections (top view)



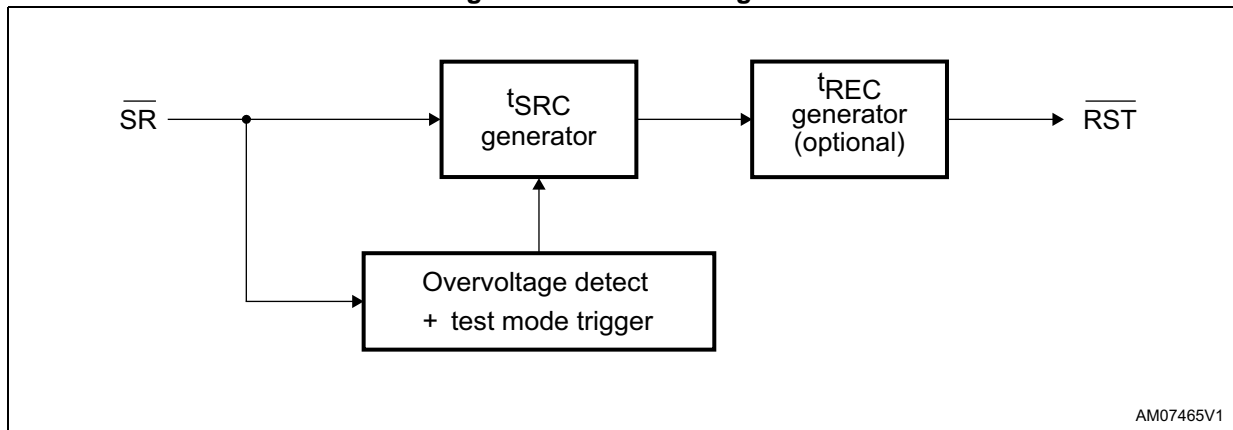
1. Not connected (not bonded); should be connected to  $V_{SS}$ .

## 2 Device overview

Table 1. Signal names

Pin n°	Name	Type	Description
1	$\overline{\text{RST}}$	Output	Reset output, active low, open drain.
2	$V_{\text{SS}}$	Supply ground	Ground
3	$\overline{\text{SR}}$	Input	Smart Reset input, active low.
4	$V_{\text{CC}}$	Supply voltage	Positive supply voltage for the device. A 0.1 $\mu\text{F}$ decoupling ceramic capacitor is recommended to be connected between $V_{\text{CC}}$ and $V_{\text{SS}}$ pins.
5	NC	-	Not connected (not bonded); should be connected to $V_{\text{SS}}$ .
6	NC	-	Not connected (not bonded); should be connected to $V_{\text{SS}}$ .

Figure 3. SR1 block diagram



## 3 Pin descriptions

### 3.1 Power supply ( $V_{CC}$ )

This pin is used to provide power to the Smart Reset device. A 0.1  $\mu\text{F}$  ceramic decoupling capacitor is recommended to be connected between the  $V_{CC}$  and  $V_{SS}$  pins, as close to the SR1 device as possible.

### 3.2 Power-up sequence

In normal mode, if different input side ( $\overline{\text{SR}}$ ) and  $V_{CC}$  voltage domains are used, power-on sequence must avoid meeting the test mode entry condition to avoid inadvertent test mode entry: there should not be logic high present on the  $\overline{\text{SR}}$  input before the  $V_{CC}$  power-up. However  $V_{CC}$  and  $V(\overline{\text{SR}})$  rising at the same time is OK (e.g. if both are in the same voltage domain), the device will then safely start into normal operating mode, with  $\overline{\text{RST}}$  output inactive (in High-Z mode for open-drain option).

### 3.3 Ground ( $V_{SS}$ )

This is the ground pin for the device.

### 3.4 Smart Reset input ( $\overline{\text{SR}}$ )

Push-button Smart Reset input, active low with optional pull-up resistor.  $\overline{\text{SR}}$  input needs to be asserted for at least  $t_{\text{SRC}}$  to assert the reset output ( $\overline{\text{RST}}$ ).

By connecting a voltage higher than  $V_{CC} + 1.4 \text{ V}$  to the  $\overline{\text{SR}}$  input the device enters test mode (see [Section 1: Description on page 3](#) for more information).

### 3.5 Reset output ( $\overline{\text{RST}}$ )

$\overline{\text{RST}}$  is active low or active high, open drain or push-pull reset output with optional internal pull-up resistor.

Output reset pulse width is optional as follows:

- Neither fixed nor minimum output reset pulse duration (releasing the push-button while reset output is active, causes the output to de-assert)
- Fixed, factory-programmed output reset pulse duration for  $t_{\text{REC}}$  independent on Smart Reset input state.

### 3.6 $\overline{\text{RST}}$ output undervoltage behavior (for open-drain option)

High-Z on  $\overline{\text{RST}}$  output below the specified operating voltage range is guaranteed at  $V_{CC}$  power-on or in case that valid  $V_{CC}$  dropped while the device was idle, i.e. while both output and input were inactive.

## 4 Typical application diagrams

Figure 4. Typical application diagram - input, output and SR1 device in one voltage domain

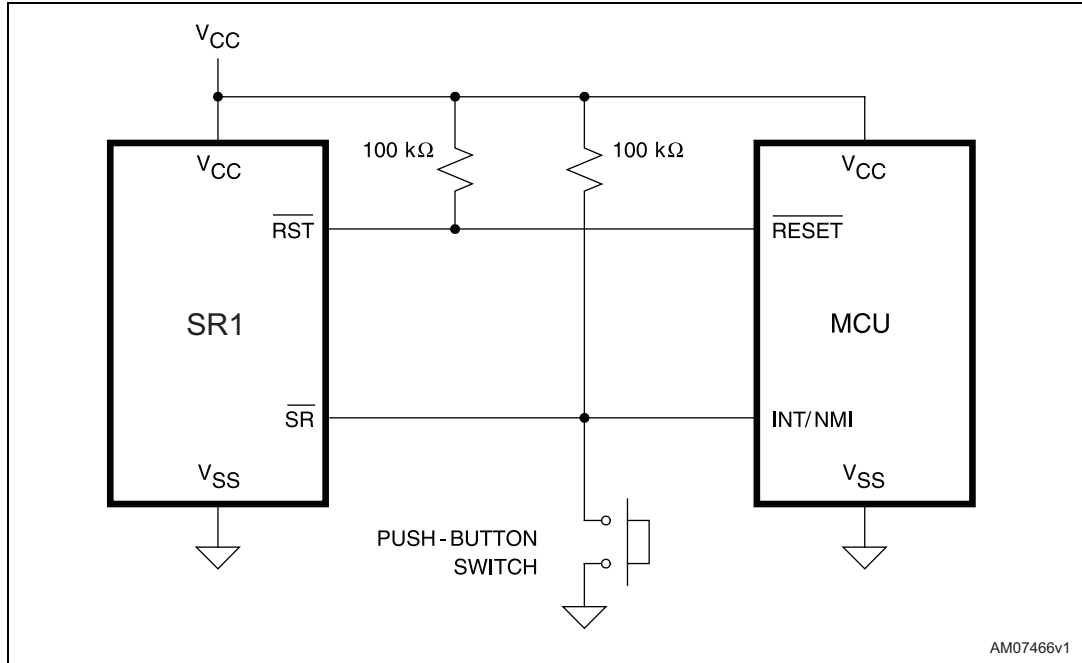
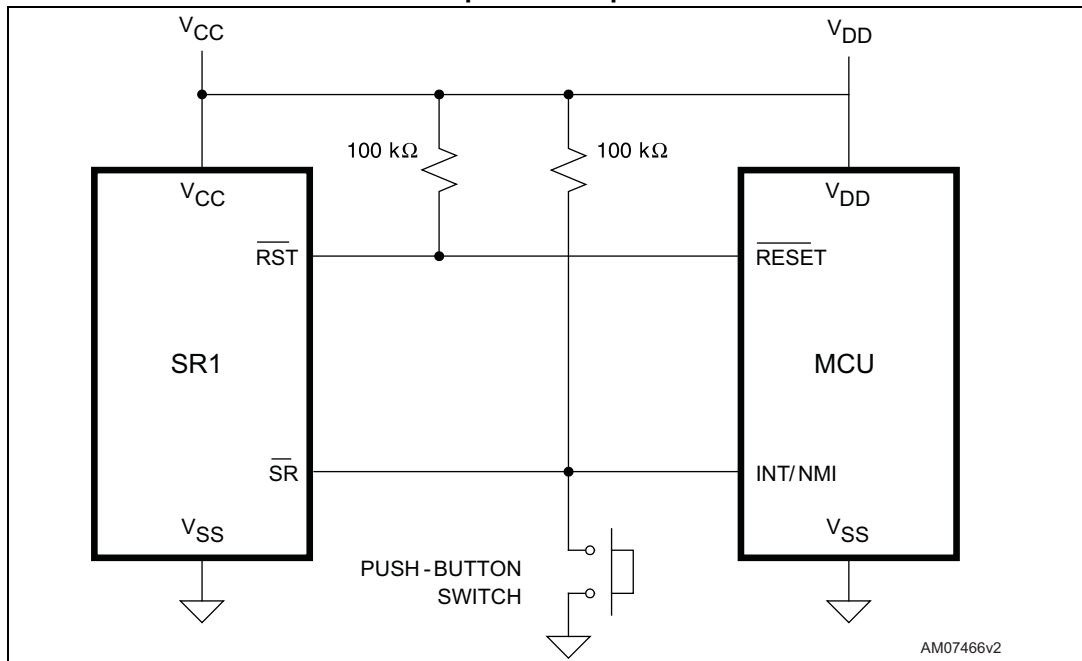
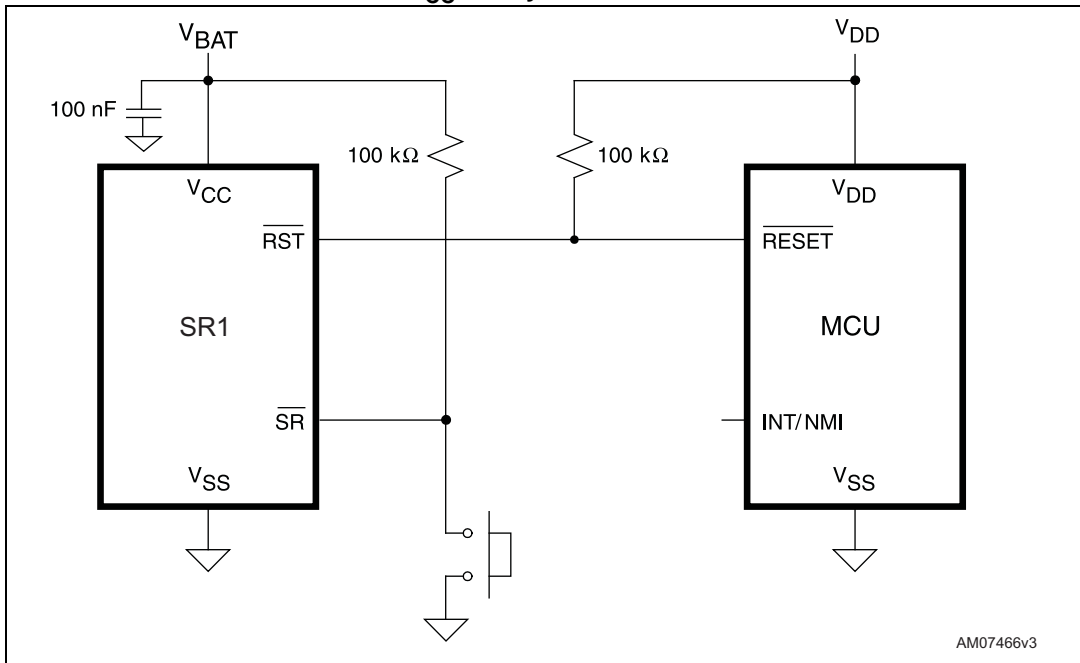


Figure 5. Typical application diagram - SR1 device in a different voltage domain than input and output



1. Open-drain  $\overline{RST}$  output type and fixed  $\overline{SR}$  input logic threshold allows to use the device in different voltage domains. To prevent entering test mode by creating a condition  $V(SR) > V_{CC} + 1.1\text{ V typ.}$ ,  $V_{CC}$  should be powered up before or together with voltage on the SR input.

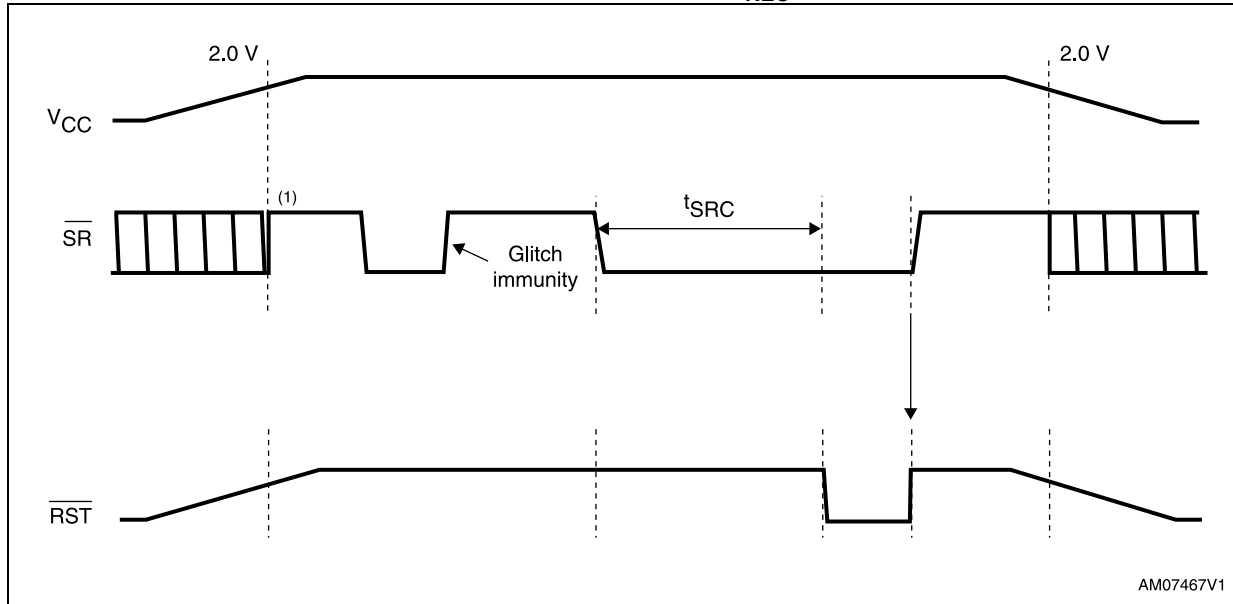
Figure 6. Typical application diagram in different voltage domains -  $\overline{SR}$  input in  $V_{BAT}$  domain like  $V_{CC}$  totally disables the test mode





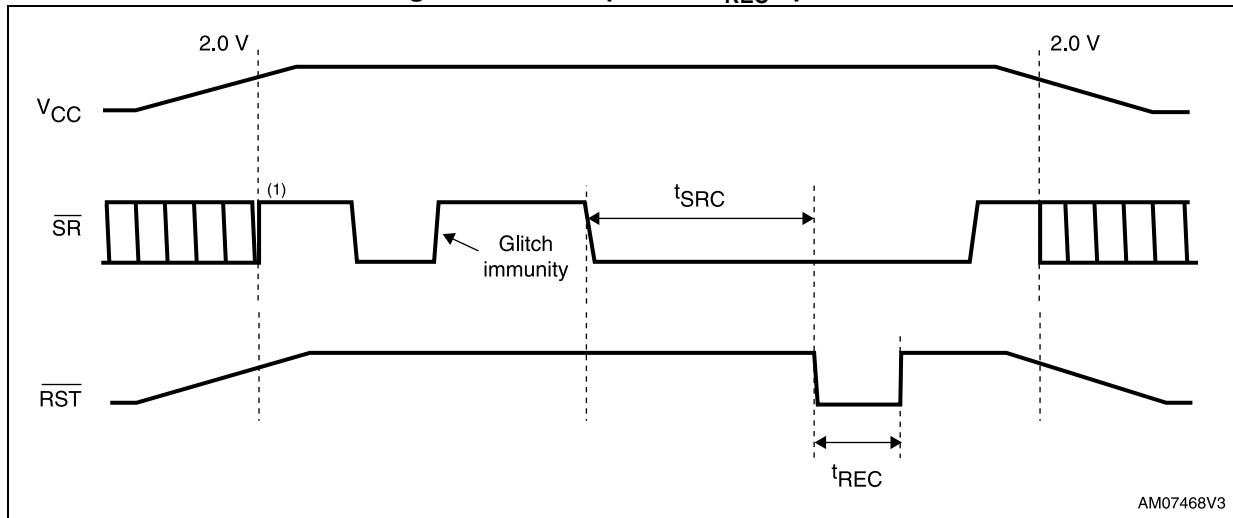
## 5 Timing diagrams

Figure 7.  $\overline{\text{RST}}$  output without  $t_{\text{REC}}$  option



1.  $V_{\text{CC}}$  should be powered up before or together with voltage on the  $\overline{\text{SR}}$  input to prevent entering test mode by creating a condition  $V(\overline{\text{SR}}) > V_{\text{CC}} + 1.1 \text{ V typ.}$

Figure 8.  $\overline{\text{RST}}$  output with  $t_{\text{REC}}$  option



1.  $V_{\text{CC}}$  should be powered up before or together with voltage on the  $\overline{\text{SR}}$  input to prevent entering test mode by creating a condition  $V(\overline{\text{SR}}) > V_{\text{CC}} + 1.1 \text{ V typ.}$

## 6 Typical operating characteristics

Figure 9. Supply current ( $I_{CC}$ ) vs. temperature ( $T_A$ )

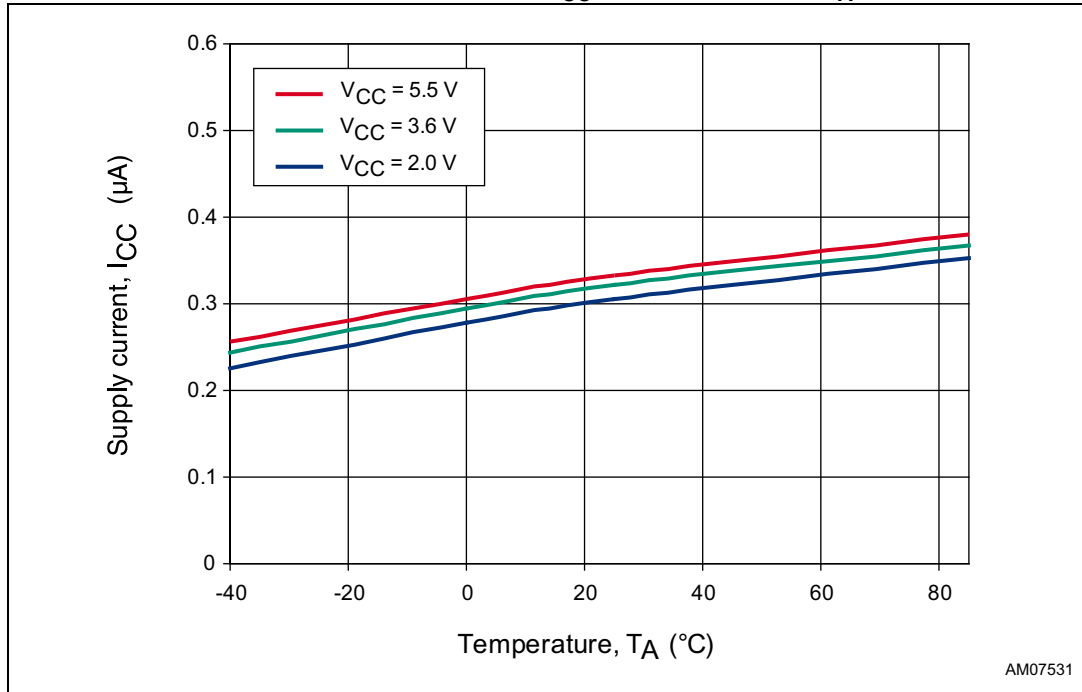


Figure 10. Smart Reset delay ( $t_{SRC}$ ) vs. temperature ( $T_A$ ),  $t_{SRC} = 4.0 s$  (typ.)

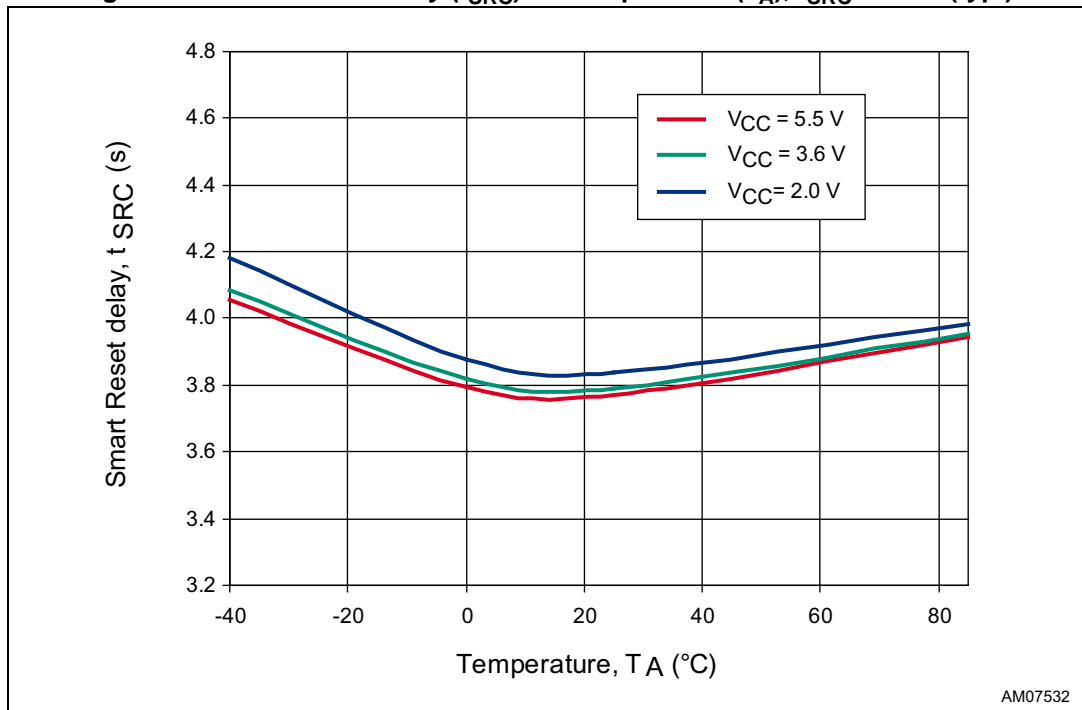


Figure 11. Test mode entry voltage ( $V_{TEST}$ ) vs. temperature ( $T_A$ )

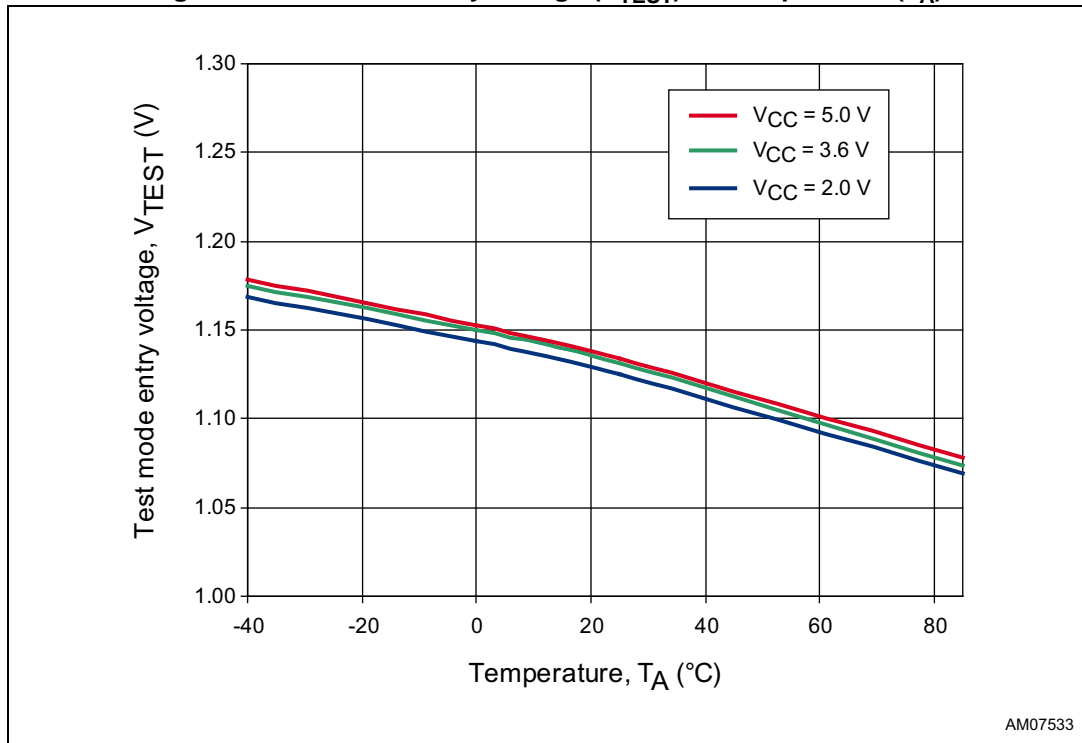
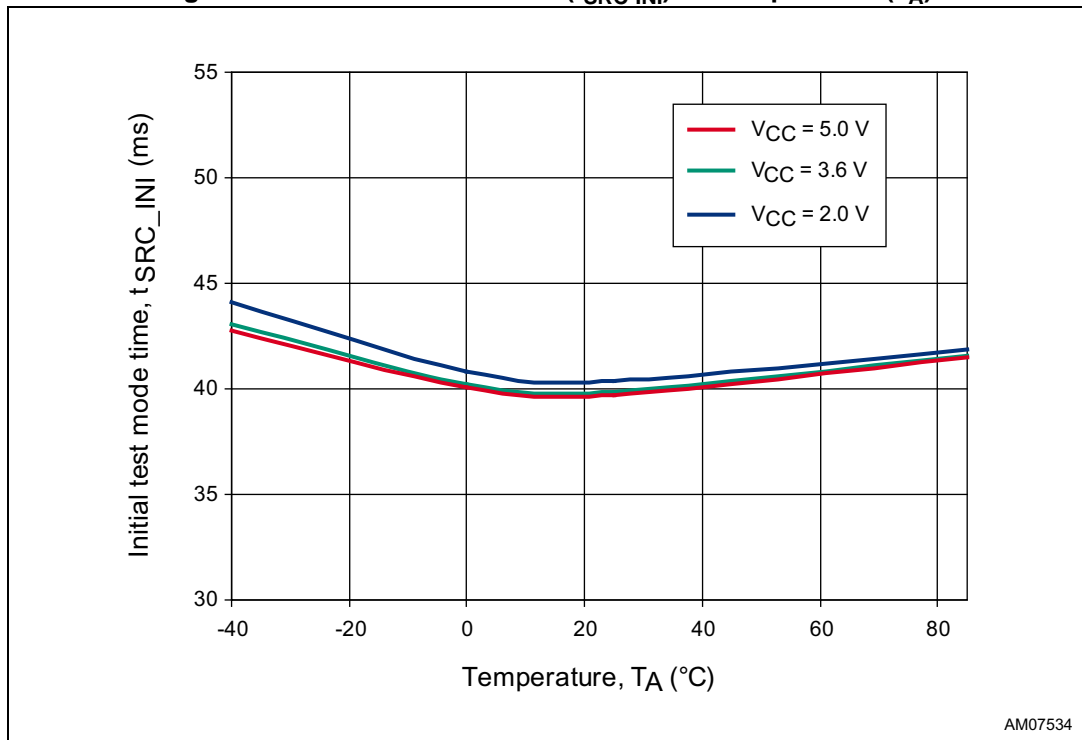


Figure 12. Initial test mode time ( $t_{SRC\_INI}$ ) vs. temperature ( $T_A$ )



## 7 Maximum ratings

Stressing the device above the rating listed in [Table 2: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in [Table 3: Operating and measurement conditions](#) of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality documents.

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$T_{STG}$	Storage temperature ( $V_{CC}$ off)	-55 to +150	°C
$T_{SLD}^{(1)}$	Lead solder temperature for 10 seconds	260	°C
$V_{IO}$	Input or output voltage	-0.3 to 5.5	V
$V_{CC}$	Supply voltage	-0.3 to 7	V
<b>ESD</b>			
$V_{HBM}$	Electrostatic discharge protection, human body model (JESD22-A114-B level 2)	2	kV
$V_{RCDM}$	Electrostatic discharge protection, charged device model, all pins	1	kV
$V_{MM}$	Electrostatic discharge protection, machine model, all pins (JESD22-A115-A level A)	200	V
	Latch-up ( $V_{CC}$ pin, $\overline{SR}$ reset input pin)	EIA/JESD78	

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

## 8 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in [Table 4: DC and AC characteristics](#) are derived from tests performed under the measurement conditions summarized in [Table 3: Operating and measurement conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

**Table 3. Operating and measurement conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	2.0 to 5.5	V
$T_A$	Ambient operating temperature	-40 to +85	°C
$t_R, t_F$	Input rise and fall times	$\leq 5$	ns
	Input pulse voltages	0.2 to 0.8 $V_{CC}$	V
	Input and output timing reference voltages	0.3 to 0.7 $V_{CC}$	V

Table 4. DC and AC characteristics

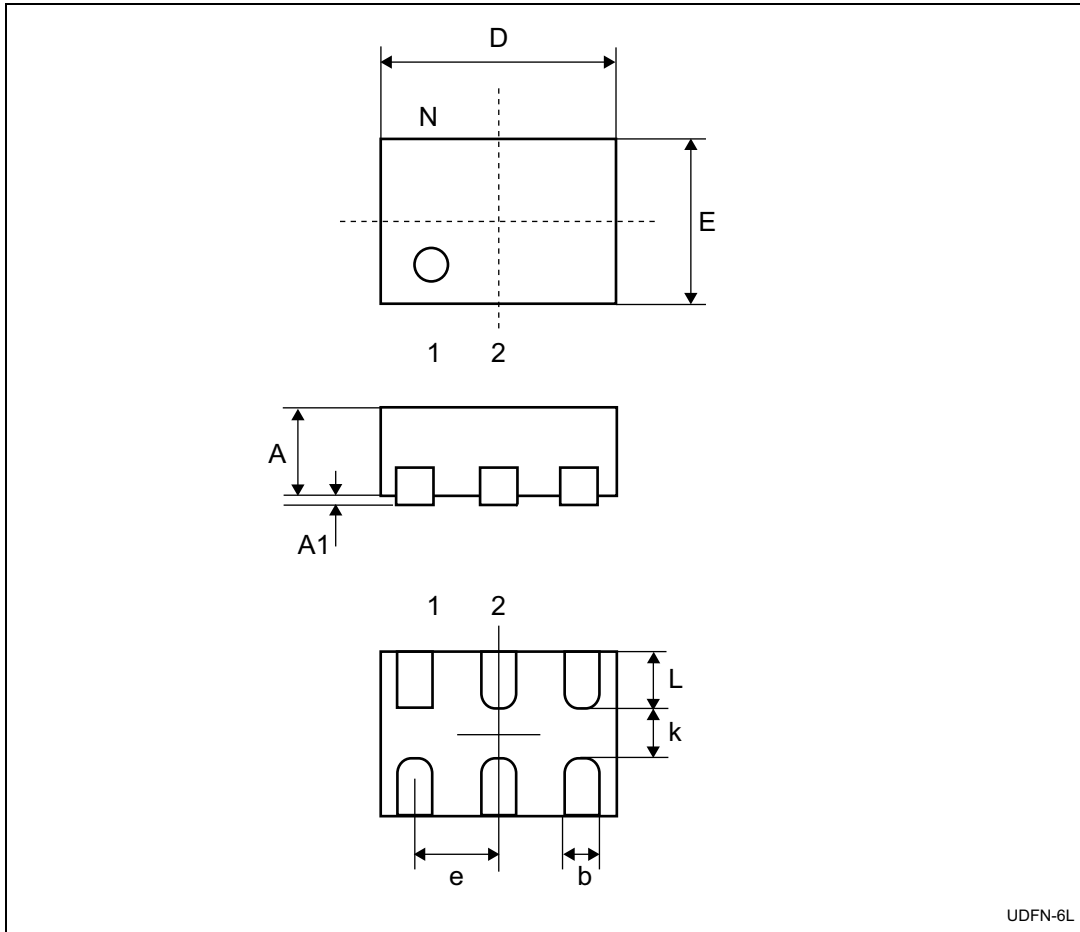
Symbol	Parameter	Test conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
V <sub>CC</sub>	Supply voltage		2.0		5.5	V
I <sub>CC</sub>	Supply current	$\overline{SR} = V_{CC}$ , t <sub>REC</sub> and t <sub>SRC</sub> counter is not running		0.4	1.0	μA
V <sub>OL</sub>	Reset output voltage low	V <sub>CC</sub> ≥ 4.5 V, sinking 3.2 mA			0.3	V
		V <sub>CC</sub> ≥ 3.3 V, sinking 2.5 mA			0.3	V
		V <sub>CC</sub> ≥ 2.0 V, sinking 1 mA			0.3	V
t <sub>REC</sub>	Reset timeout delay, factory-programmed	(device option)	140	210	280	ms
			240	360	480	ms
R <sub>PUO</sub>	Internal output pull-up resistor on RST	(device option)		65		kΩ
I <sub>LO</sub>	Output leakage current	V <sub>RST</sub> = 5.5 V, open drain device option without output pull-up resistor	-0.1		0.1	μA
<b>Smart Reset</b>						
t <sub>SRC</sub>	Smart Reset delay	T <sub>A</sub> = -40 to +85 °C	0.8 x t <sub>SRC</sub>	t <sub>SRC</sub> <sup>(3)</sup>	1.2 x t <sub>SRC</sub>	s
		T <sub>A</sub> = 25 °C	0.9 x t <sub>SRC</sub>		1.1 x t <sub>SRC</sub>	
V <sub>IL</sub>	$\overline{SR}$ input voltage low		V <sub>SS</sub> -0.3		0.3	V
V <sub>IH</sub>	$\overline{SR}$ input voltage high		0.85		5.5	V
R <sub>PUI</sub>	Internal input pull-up resistor on SR	(device option)		65		kΩ
I <sub>LEAK</sub>	$\overline{SR}$ input leakage current	device option without input pull-up resistor	-0.1		0.1	μA
	Input glitch immunity			t <sub>SRC</sub>		s
<b>Test mode</b>						
V <sub>TEST</sub>	Test mode entry voltage		V <sub>CC</sub> +0.9	V <sub>CC</sub> +1.1	V <sub>CC</sub> +1.4	V
t <sub>SRC-INI</sub>	Initial test mode time		28	42	56	ms
t <sub>SRC-SHORT</sub>	Shortened Smart Reset delay			t <sub>SRC</sub> / 128		ms

1. Valid for ambient operating temperature T<sub>A</sub> = -40 to +85 °C, V<sub>CC</sub> = 2.0 to 5.5 V.
2. Typical values are at 25 °C and V<sub>CC</sub> = 3.3 V unless otherwise noted.
3. Factory-programmable in the range of 0.5 s to 10 s typ. in 0.5 s steps.

## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 13. UDFN6, (1.00 x 1.45 x 0.50 mm), 0.50 mm pitch package outline

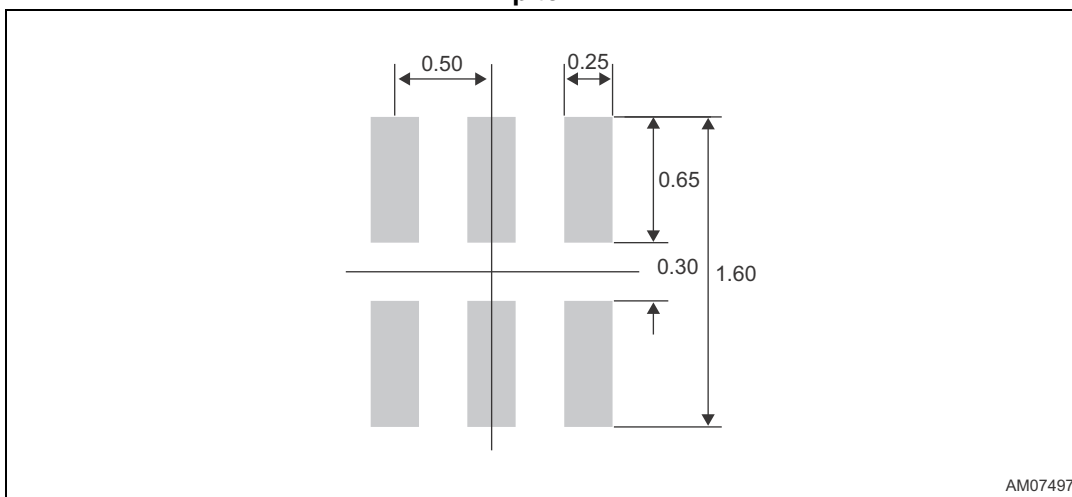


**Table 5. UDFN6, (1.00 x 1.45 x 0.50 mm), 0.50 mm pitch package mechanical data**

Symbol	Dimensions						Note <sup>(1)</sup>
	(mm)			(inches)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
A	0.50	0.55	0.60	0.0197	0.0217	0.0236	
A1	0.00	0.02	0.05	0.000	0.0008	0.0020	
b	0.18	0.25	0.30	0.0071	0.0098	0.0118	
D	1.40	1.45	1.50	0.0551	0.0571	0.0591	
E	0.95	1.00	1.05	0.0374	0.0394	0.0413	
e	0.45	0.50	0.55	0.0177	0.0197	0.0217	
k	0.20			0.0079			
L	0.30	0.35	0.40	0.0118	0.0138	0.0157	

1. Package outline exclusive of any mold flashes dimensions and metal burrs.

**Figure 14. Footprint recommendation for UDFN6 (1.00 x 1.45 x 0.50 mm), 0.50 mm pitch**

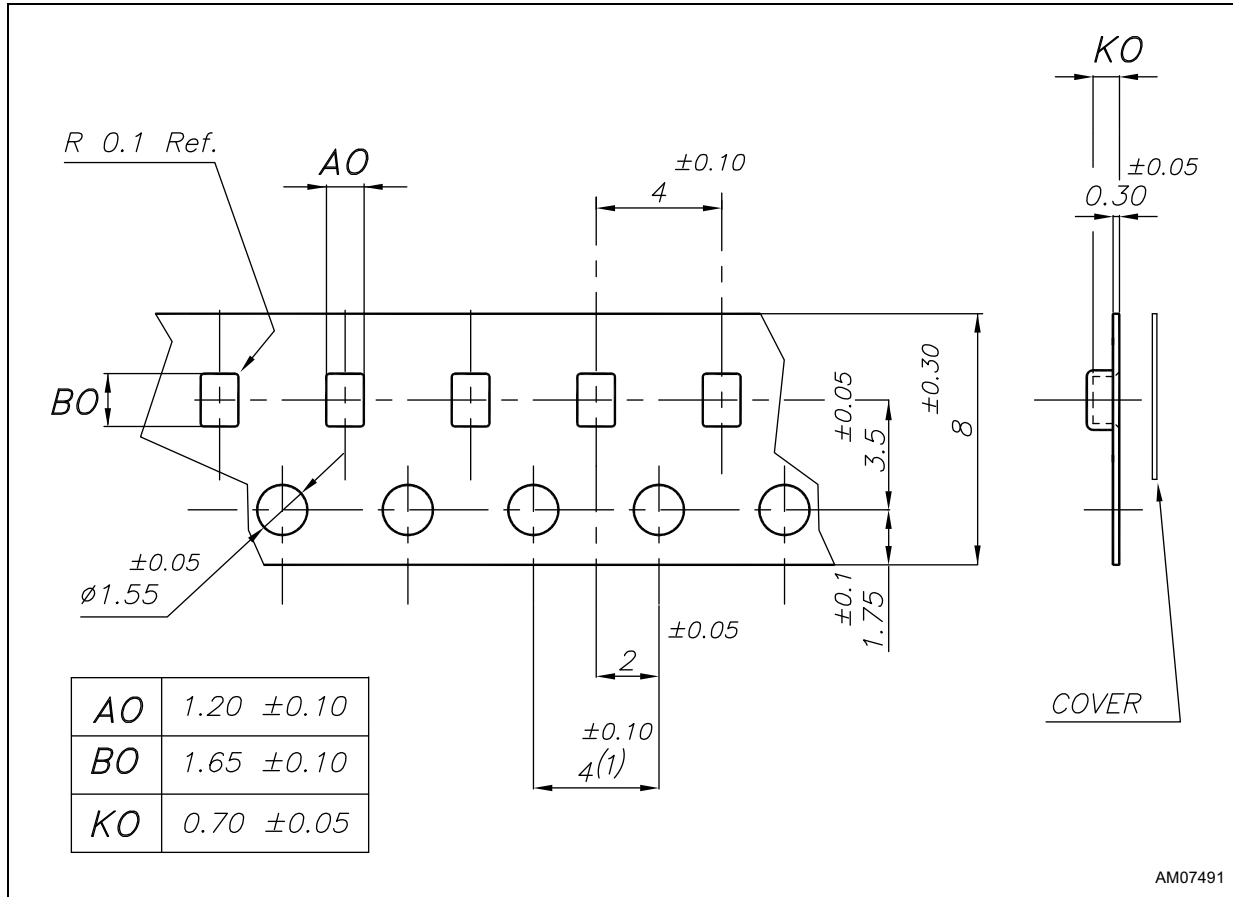


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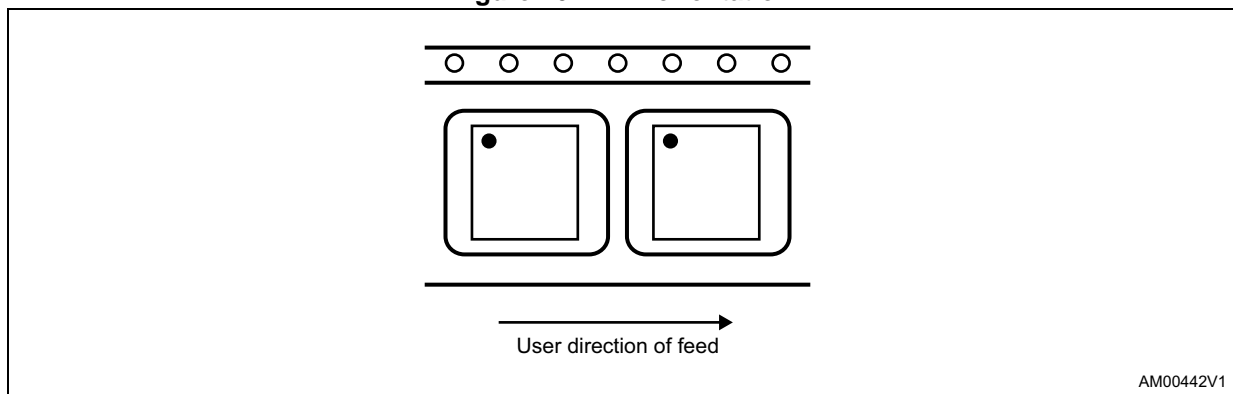
# 10 Tape and reel information

Figure 15. Carrier tape



1. 10-sprocket hole pitch cumulative tolerance ±0.20.

Figure 16. Pin 1 orientation



# 11 Part numbering

**Table 6. Ordering information scheme**

Example:	SR1	H	A	R	U
<b>Device type</b>					
SR1					
<b>Smart Reset setup delay (<math>t_{SRC}</math>)<sup>(1)</sup></b>					
C = factory programmable $t_{SRC} = 1.5$ s (typ.)					
H = factory programmable $t_{SRC} = 4.0$ s (typ.)					
L = factory programmable $t_{SRC} = 6.0$ s (typ.)					
P = factory programmable $t_{SRC} = 7.5$ s (typ.)					
U = factory programmable $t_{SRC} = 10.0$ s (typ.)					
<b>Inputs, outputs type<sup>(2)</sup></b>					
A = active low $\overline{SR}$ input with no pull-up, active low open drain $\overline{RST}$ output with no pull-up					
B = active low $\overline{SR}$ input with pull-up, active low open drain $\overline{RST}$ output with no pull-up					
<b>Reset timeout period (<math>t_{REC}</math>)</b>					
A = factory programmable $t_{REC} = 210$ ms (typ.)					
B = factory programmable $t_{REC} = 360$ ms (typ.)					
R = push-button controlled (no defined $t_{REC}$ )					
<b>Package</b>					
U = UDFN-6L					

1. Smart Reset delay ( $t_{SRC}$ ) is available from 0.5 s to 10 s in 0.5 s steps (typ.). Minimum order quantities may apply. Contact local sales office for availability.
2. Push-pull reset output type also available (active low or active high).  $\overline{SR}$  input and open drain reset output available with optional pull-up resistor. Minimum order quantities may apply. Contact local sales office for availability.

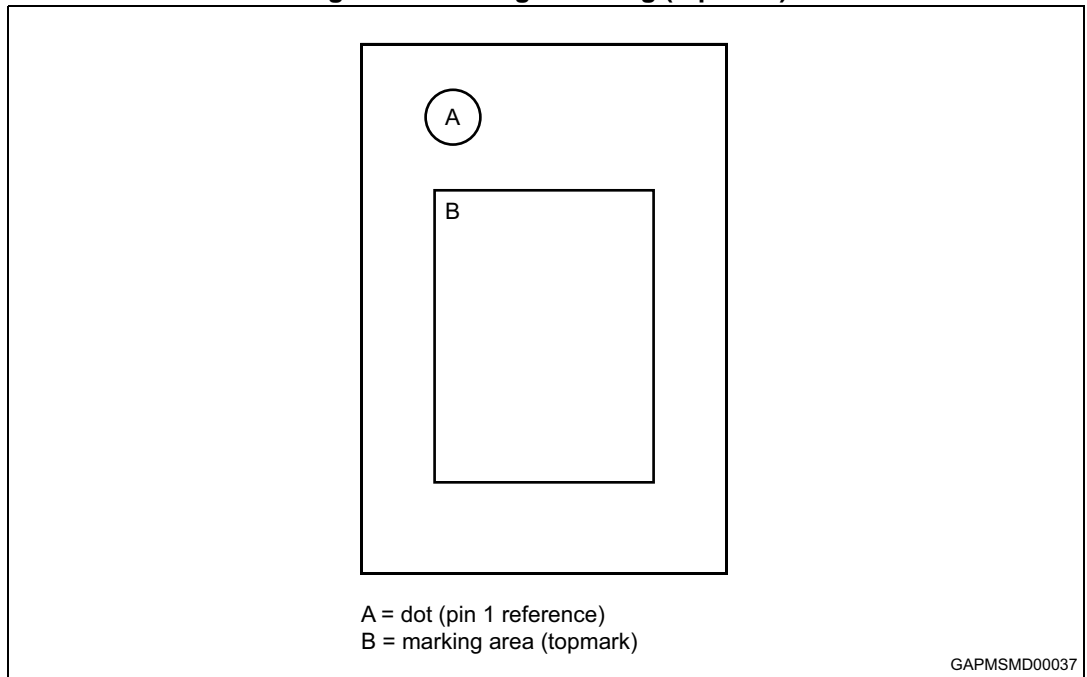
## 12 Package marking information

Table 7. Package marking

Part number	$t_{SRC}$ (s)	Smart Reset inputs <sup>(1)</sup>	Output type <sup>(2)</sup>	$t_{REC}$ option <sup>(3)</sup>	Package	Topmark
SR1CARU	1.5	AL	OD, AL	No $t_{REC}$	UDFN6	CA
SR1HARU	4.0	AL	OD, AL	No $t_{REC}$	UDFN6	HA
SR1LARU	6.0	AL	OD, AL	No $t_{REC}$	UDFN6	LA
SR1PAAU	7.5	AL	OD, AL	210 ms	UDFN6	PB
SR1PARU	7.5	AL	OD, AL	No $t_{REC}$	UDFN6	PA
SR1PBBU	7.5	AL + pull-up	OD, AL	360 ms	UDFN6	PC
SR1UARU	10.0	AL	OD, AL	No $t_{REC}$	UDFN6	UA

1. AL = active low.
2. OD = open drain, AL = active low.
3. No  $t_{REC}$  = push-button controlled reset pulse width, any other value represents typical value of  $t_{REC}$ .

Figure 17. Package marking (top view)



## 13 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
10-Mar-2014	1	Initial release
13-May-2014	2	Modified $t_{REC}$ values <a href="#">Table 4 on page 14</a>

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