

4-Pin Microprocessor Power Supply Supervisors with Manual Reset



FEATURES

- Precision monitoring of
 - +5.0 V ($\pm 5\%$, $\pm 10\%$, $\pm 20\%$),
 - +3.3 V ($\pm 5\%$, $\pm 10\%$),
 - +3.0 V ($\pm 10\%$) and
 - +2.5 V ($\pm 5\%$) power supplies
- Manual reset input
- Offered in two output configurations:
- CAT811: Active LOW reset
- CAT812: Active HIGH reset
- Direct replacements for the MAX811 and MAX812 in applications operating over the industrial temperature range
- Reset valid down to $V_{CC} = 1.0V$
- 6 μA power supply current
- Power supply transient immunity
- Available in SOT-143 packages with Sn or NiPdAu Green Lead finishes.
- Industrial temperature range: -40°C to +85°C

APPLICATION

- Computers, Servers, Laptops
- Cable modems
- Wireless communications
- Embedded control systems
- White goods
- Power meters
- Intelligent instruments
- PDAs and handheld equipment

THRESHOLD SUFFIX SELECTOR DESCRIPTION

Nominal Threshold Voltage	Threshold Suffix Designation
4.63V	L
4.38V	M
4.00V	J
3.08V	T
2.93V	S
2.63V	R
2.32V	Z

DESCRIPTION

The CAT811 and CAT812 are microprocessor supervisory circuits that monitor power supplies. The CAT811 and CAT812 are direct replacements for the MAX811 and MAX812 in applications operating over the industrial temperature range; both have a manual reset input.

These devices generate a reset signal, which is asserted while the power supply voltage is below a preset threshold level and for at least 140ms after the power supply level has risen above that level. The underlying floating gate technology, AE²(TM) used by Catalyst Semiconductor, makes it possible to offer any custom reset threshold value. Seven industry standard threshold levels are offered to support +5.0V, +3.3V, +3.0V and +2.5V systems.

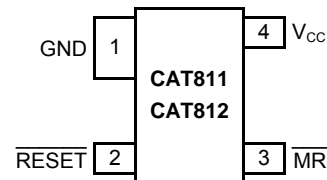
The CAT811 features a RESET push-pull output (active LOW) and the CAT812 features a RESET push-pull output (active HIGH).

Fast transients on the power supply are ignored and the output is guaranteed to be in the correct state at V_{CC} levels as low as 1.0 V.

The CAT811/812 are fully specified over the industrial temperature range (-40°C to 85°C) and are available in a compact 4-pin SOT-143 package.

For Ordering Information details, see page 10.

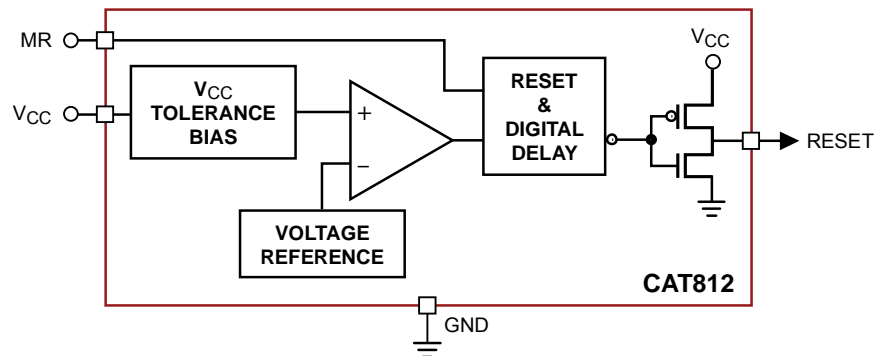
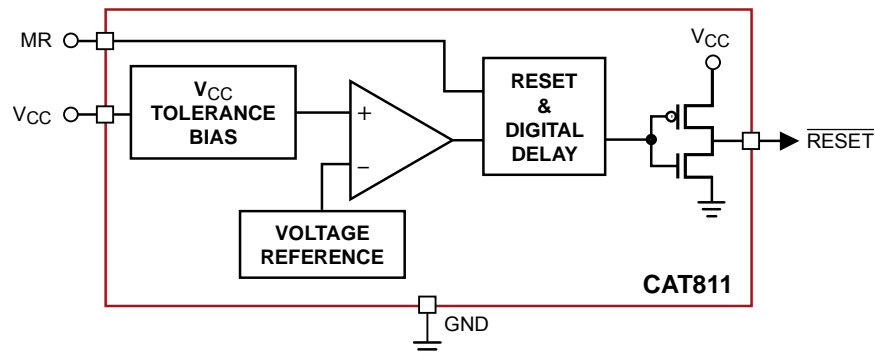
PIN CONFIGURATION



PIN DESCRIPTION

Pin Number		Name	Description
CAT811	CAT812		
1	1	GND	Ground
2	—	$\overline{\text{RESET}}$	Active LOW reset. $\overline{\text{RESET}}$ is asserted if V_{CC} falls below the reset threshold and remains low for at least 140ms after V_{CC} rises above the reset threshold.
—	2	RESET	Active HIGH reset. RESET is asserted if V_{CC} falls below the reset threshold and remains high for at least 140ms after V_{CC} rises above the reset threshold.
3	3	$\overline{\text{MR}}$	Manual Reset Input. A logic LOW on $\overline{\text{MR}}$ asserts $\overline{\text{RESET}}$. RESET remains active as long as $\overline{\text{MR}}$ is LOW and for 140ms after $\overline{\text{MR}}$ returns HIGH. The active low input has an internal 20k Ω pull-up resistor. The input should be left open if not used.
4	4	V_{CC}	Power supply voltage that is monitored.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Parameters	Ratings	Units
Any pin with respect to ground	-0.3 to + 6.0	V
Input Current, V_{CC}	20	mA
Output Current RESET, \overline{RESET}	20	mA
Rate of Raise, V_{CC}	100	V/ μ s
Continuous Power Dissipations Derate 4mW/ $^{\circ}$ C above +70 $^{\circ}$ C (SOT-143)	320	mW
Storage Temperature	-65 to +105	$^{\circ}$ C
Operating Ambient Temperature	-40 to +85	$^{\circ}$ C
Lead Soldering (10 seconds)	+300	$^{\circ}$ C

ELECTRICAL OPERATING CHARACTERISTICS

V_{CC} = Full range, T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C unless otherwise noted. Typical values at T_A = +25 $^{\circ}$ C and V_{CC} = 5V for the L/M/J versions, V_{CC} = 3.3V for the T/S versions, V_{CC} = 3V for the R version and V_{CC} = 2.5V for the Z version.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
V_{CC} Range		T_A = 0 $^{\circ}$ C to +70 $^{\circ}$ C	1.0		5.5	V	
		T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	1.2		5.5		
Supply Current	I_{CC}	T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	V_{CC} < 5.5V, J/L/M		8	20	μ A
			V_{CC} < 3.6V, R/S/T/Z		6	15	
Reset Threshold Voltage	V_{TH}	L Threshold	T_A = +25 $^{\circ}$ C	4.56	4.63	4.70	V
			T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	4.50		4.75	
		M Threshold	T_A = +25 $^{\circ}$ C	4.31	4.38	4.45	
			T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	4.25		4.50	
		J Threshold	T_A = +25 $^{\circ}$ C	3.93	4.00	4.06	
			T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	3.89		4.10	
		T Threshold	T_A = +25 $^{\circ}$ C	3.04	3.08	3.11	
			T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	3.00		3.15	
		S Threshold	T_A = +25 $^{\circ}$ C	2.89	2.93	2.96	
			T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	2.85		3.00	
		R Threshold	T_A = +25 $^{\circ}$ C	2.59	2.63	2.66	
			T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	2.55		2.70	
		Z Threshold	T_A = +25 $^{\circ}$ C	2.28	2.32	2.35	
			T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C	2.25		2.38	

Notes:

- (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

ELECTRICAL OPERATING CHARACTERISTICS (continued)

V_{CC} = Full range, T_A = -40°C to $+85^{\circ}\text{C}$ unless otherwise noted. Typical values at T_A = $+25^{\circ}\text{C}$ and V_{CC} = 5V for the L/M/J versions, V_{CC} = 3.3V for the T/S versions, V_{CC} = 3V for the R version and V_{CC} = 2.5V for the Z version.

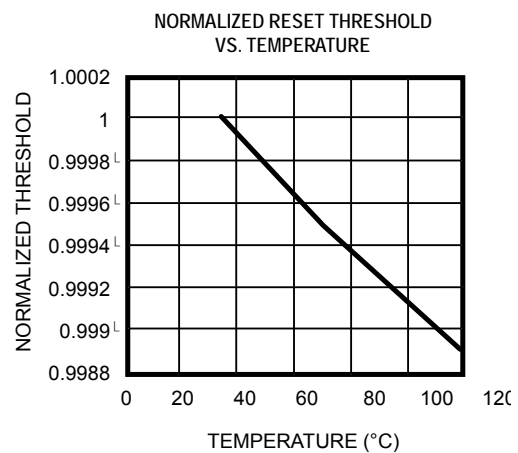
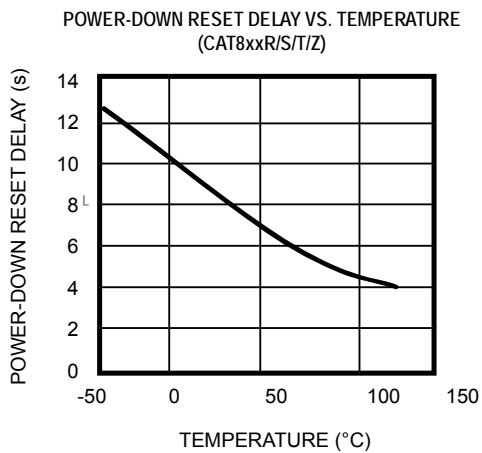
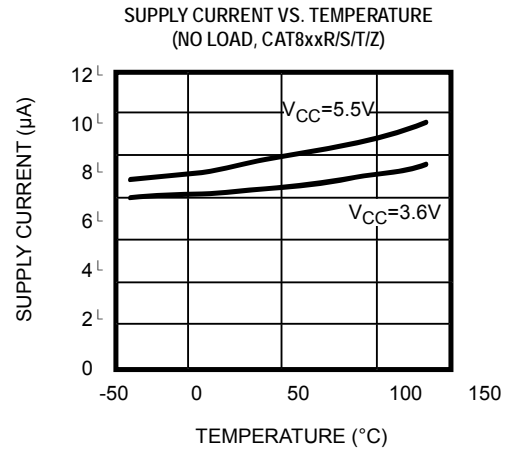
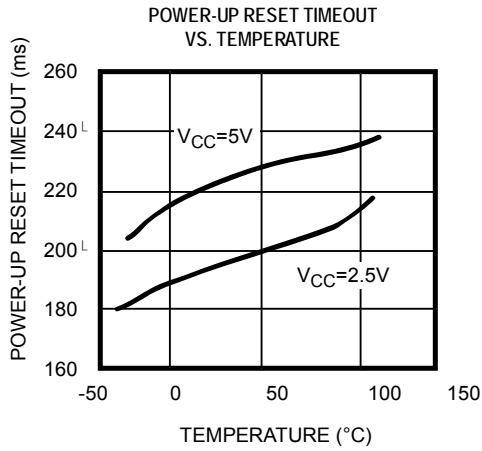
Parameter	Symbol	Conditions	Min	Typ ⁽¹⁾	Max	Units
Reset Threshold Tempco				30		ppm/ $^{\circ}\text{C}$
V_{CC} to Reset Delay ⁽²⁾		$V_{CC} = V_{TH}$ to $(V_{TH} - 100\text{mV})$		20		μs
Reset Active Timeout Period		$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	140	240	400	ms
$\overline{\text{RESET}}$ Output Voltage Low (Push-pull, active LOW, CAT811)	V_{OL}	$V_{CC} = V_{TH\ min}$, $I_{SINK} = 1.2\text{mA}$ CAT811R/S/T/Z			0.3	V
		$V_{CC} = V_{TH\ min}$, $I_{SINK} = 3.2\text{mA}$ CAT811J/L/M			0.4	
		$V_{CC} > 1.0\text{V}$, $I_{SINK} = 50\mu\text{A}$			0.3	
$\overline{\text{RESET}}$ Output Voltage High (Push-pull, active LOW, CAT811)	V_{OH}	$V_{CC} = V_{TH\ max}$, $I_{SOURCE} = 500\mu\text{A}$ CAT811R/S/T/Z	$0.8V_{CC}$			V
		$V_{CC} = V_{TH\ max}$, $I_{SOURCE} = 800\mu\text{A}$ CAT811J/L/M	$V_{CC} - 1.5$			
RESET Output Voltage Low (Push-pull, active HIGH, CAT812)	V_{OL}	$V_{CC} > V_{TH\ max}$, $I_{SINK} = 1.2\text{mA}$ CAT812R/S/T/Z			0.3	V
		$V_{CC} > V_{TH\ max}$, $I_{SINK} = 3.2\text{mA}$ CAT812J/L/M			0.4	
RESET Output Voltage High (Push-pull active HIGH, CAT812)	V_{OH}	$1.8\text{V} < V_{CC} \leq V_{TH\ min}$, $I_{SOURCE} = 150\mu\text{A}$	$0.8V_{CC}$			V
$\overline{\text{MR}}$ Minimum Pulse Width	t_{MR}		10			μs
$\overline{\text{MR}}$ Glitch Immunity		Note 3		100		ns
$\overline{\text{MR}}$ to RESET Propagation Delay	t_{MD}	Note 2		0.5		μs
$\overline{\text{MR}}$ Input Threshold	V_{IH}	$V_{CC} > V_{TH\ (MAX)}$, CAT811/812L/M/J	2.3V			
	V_{IL}				0.8	V
	V_{IH}	$V_{CC} > V_{IH\ (MAX)}$, CAT811/812R/S/T/Z	$0.7V_{CC}$			
	V_{IL}				$0.25V_{CC}$	
$\overline{\text{MR}}$ Pull-up Resistance			10	20	30	k Ω

Notes:

- (1) Production testing done at $T_A = +25^{\circ}\text{C}$; limits over temperature guaranteed by design only.
- (2) $\overline{\text{RESET}}$ output for the CAT811; RESET output for the CAT812
- (3) Glitches of 100ns or less typically will not generate a reset pulse

TYPICAL OPERATING CHARACTERISTICS

V_{CC} = Full range, T_A = -40°C to $+85^{\circ}\text{C}$ unless otherwise noted. Typical values at T_A = $+25^{\circ}\text{C}$ and V_{CC} = 5V for the L/M/J versions, V_{CC} = 3.3V for the T/S versions, V_{CC} = 3V for the R version and V_{CC} = 2.5V for the Z version.



DETAILED DESCRIPTION

RESET TIMING

The reset signal is asserted LOW for the CAT811 and HIGH for the CAT812 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140ms after the power supply voltage has risen above the threshold.

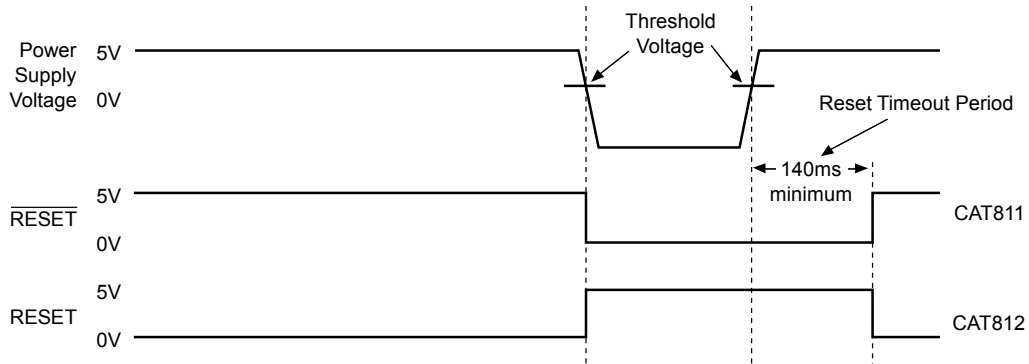


Figure 1. Reset Timing Diagram

V_{CC} TRANSIENT RESPONSE

The CAT811/812 protect μ Ps against brownout failure. Short duration transients of 4 μ s or less and 100mV amplitude typically do not cause a false RESET.

Figure 2 shows the maximum pulse duration of negative-going V_{CC} transients that do not cause a reset condition.

As the amplitude of the transient goes further below the threshold (increasing $V_{TH} - V_{CC}$), the maximum pulse duration decreases. In this test, the V_{CC} starts from an initial voltage of 0.5V above the threshold and drops below it by the amplitude of the overdrive voltage ($V_{TH} - V_{CC}$).

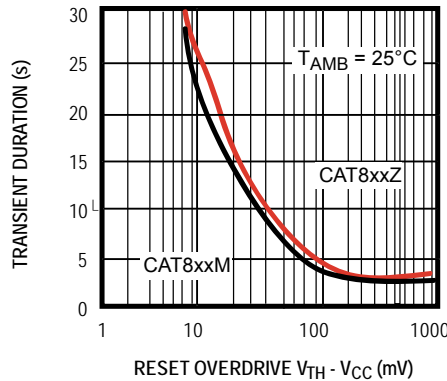


Figure 2. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

VALID RESET WITH V_{CC} UNDER 1.0V

To ensure that the CAT811 $\overline{\text{RESET}}$ pin is in a known state when V_{CC} is under 1.0V, a 100k Ω pull-down resistor between $\overline{\text{RESET}}$ pin and GND is recommended; the value is not critical. For the CAT812, a pull-up resistor from $\overline{\text{RESET}}$ pin to V_{CC} is needed.

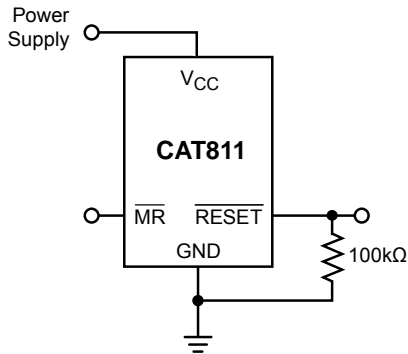


Figure 3. $\overline{\text{RESET}}$ Valid with V_{CC} under 1.0V

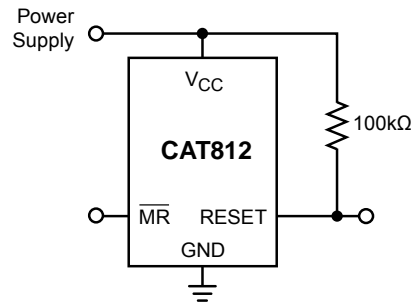


Figure 4. $\overline{\text{RESET}}$ Valid with V_{CC} under 1.1V

BI-DIRECTIONAL RESET PIN INTERFACING

The CAT811/812 can interface with $\mu\text{P}/\mu\text{C}$ bi-directional reset pins by connecting a 4.7k Ω resistor in series with the CAT811/812 reset output and the $\mu\text{P}/\mu\text{C}$ bi-directional reset pin.

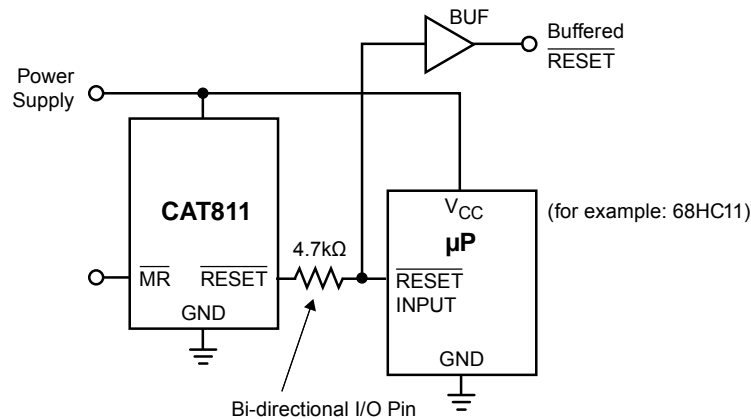


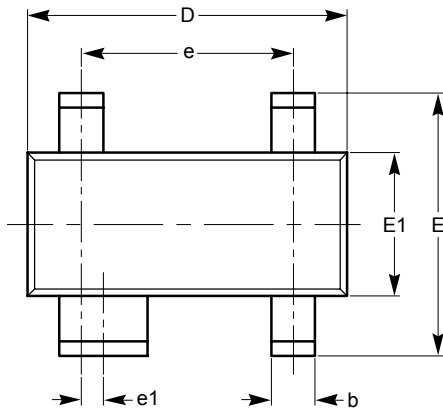
Figure 5. Bi-directional Reset Pin Interfacing

OTHER SUPERVISORY PRODUCTS

Function	CAT1161/3	CAT1162	CAT809	CAT810	CAT811	CAT812
With 16k Bit Serial EEPROM Memory	✓	✓				
Watchdog Timer	✓					
Manual Reset Input	✓	✓			✓	✓
Active Low Reset			✓		✓	
Active High Reset				✓		✓
Dual Polarity Reset Outputs	✓	✓				
Package	8-pin DIP and SOIC	8-pin DIP and SOIC	3-pin SOT-23 and SC70	3-pin SOT-23 and SC70	4-pin SOT-143	4-pin SOT-143

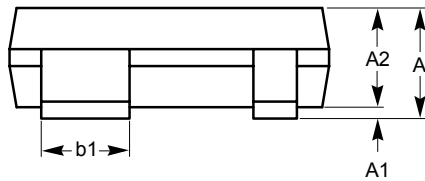
PACKAGE OUTLINE DRAWING

SOT-143 4-Lead (TB)

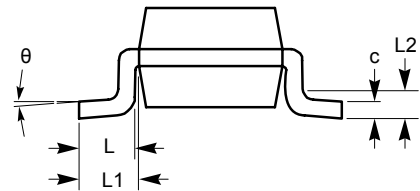


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.22
A1	0.05		0.15
A2	0.75	0.90	1.07
b	0.30		0.50
b2	0.76		0.89
c	0.08		0.20
D	2.80	2.90	3.04
E	2.10		2.64
E1	1.20	1.30	1.40
e	1.92 BSC		
e1	0.20 BSC		
L	0.40	0.50	0.60
L1	0.54 REF		
L2		0.25	
θ	0°		8°



SIDE VIEW



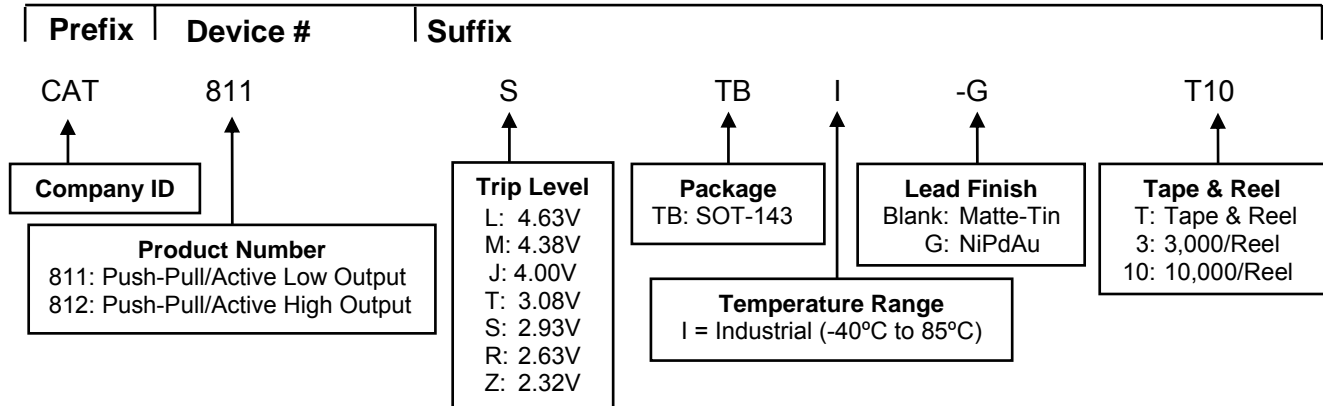
END VIEW

For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC standard TO-253.

EXAMPLE OF ORDERING INFORMATION



For Product Top Mark Codes, click here:
<http://www.catsemi.com/techsupport/producttopmark.asp>

Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu. Contact factory for other package availability.
- (3) This device used in the above example is a CAT811STBI-GT10 (SOT-143 4-Lead, Push-Pull/Active Low Output, trip level of 2.85V to 3.00V, NiPdAu, Tape & Reel, 10,000/Reel)
- (4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Rev.	Reason
10/22/2003	L	Updated Ordering Information
12/22/2003	M	Updated Features Replaced power-up reset timeout vs. temperature graph with updated one Replaced V _{CC} Transient Response graph with updated one
03/22/2004	N	General data sheet updates
03/25/2004	O	Updated Electrical Characteristics (Reset Active Timeout Period Max)
03/25/2004	P	Corrected Pin Configure diagram
09/28/2004	Q	Minor changes
12/28/2005	R	Updated Features Updated Ordering Information Updated Top Marking
04/18/2008	S	Add "MD-" to document number Add Block Diagrams Updated Package Outline Drawing Update Example of Ordering Information

Copyrights, Trademarks and Patents

© Catalyst Semiconductor, Inc.

Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

Adaptive Analog™, Beyond Memory™, DPP™, EZDim™, LDD™, MiniPot™, Quad-Mode™ and Quantum Charge Programmable™

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.



Catalyst Semiconductor, Inc.

Corporate Headquarters

2975 Stender Way

Santa Clara, CA 95054

Phone: 408.542.1000

Fax: 408.542.1200

www.catsemi.com

Document No: MD-3005

Revision: S

Issue date: 04/18/08