



Quad, Low-Power, 500Mbps ATE Driver/Comparator

MAX9963/MAX9964

General Description

The MAX9963/MAX9964 four-channel, low-power, high-speed pin electronics driver and comparator ICs include, for each channel, a three-level pin driver, a dual comparator, and variable clamps. The driver features a wide voltage range and high-speed operation, includes high-Z and active-termination (3rd-level drive) modes, and is highly linear even at low-voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions. The clamps provide damping of high-speed DUT waveforms when the device is configured as a high-impedance receiver. High-speed, differential control inputs compatible with ECL, LVPECL, LVDS, and GTL levels are provided for each channel. ECL/LVPECL or flexible open-collector outputs are available for the comparators.

The A-grade version provides tight matching of gain and offset for the drivers and comparators, allowing reference levels to be shared across multiple channels in cost-sensitive systems. For system designs that incorporate independent reference levels for each channel, the B-grade version is available at reduced cost.

Optional internal resistors at the high-speed inputs provide differential termination of LVDS inputs, while optional internal resistors provide the pullup voltage and source termination for open-collector comparator outputs. These features significantly reduce the discrete component count on the circuit board.

Low-leakage, slew rate, and tri-state/terminate controls are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface.

The MAX9963/MAX9964 operating range is -1.5V to +6.5V, with power dissipation of only 825mW per channel.

These devices are available in a 100-pin, 14mm x 14mm body, 0.5mm pitch TQFP with an exposed 8mm x 8mm die pad on the top (MAX9963) or bottom (MAX9964) of the package for efficient heat removal. The MAX9963/MAX9964 are specified to operate with an internal die temperature of +70°C to +100°C, and feature a die temperature monitor output.

Applications

- Flash Memory Testers
- Commodity DRAM Testers
- Low-Cost Mixed-Signal/System-on-Chip Testers
- Active Burn-In Systems
- Structural Testers

Features

- ◆ Small Footprint—Four Channels in 0.4in²
- ◆ Low Power Dissipation: 825mW/Channel (typ)
- ◆ High Speed: 500Mbps at 3V_{P-P}
- ◆ Low Timing Dispersion
- ◆ Wide -1.5V to +6.5V Operating Range
- ◆ Active Termination (3rd-Level Drive)
- ◆ Low-Leakage Mode: 15nA (max)
- ◆ Integrated Clamps
- ◆ Interface Easily with Most Logic Families
- ◆ Digitally Programmable Slew Rate
- ◆ Internal Logic Termination Resistors
- ◆ Low Gain and Offset Error

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---------------|--------------|---------------|
| MAX9963ADCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963AKCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963AGCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963AHCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963AJCCQ | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963BDCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963BKCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963BGCCQ | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963BHCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9963BJCCQ* | 0°C to +70°C | 100 TQFP-EPR |
| MAX9964ADCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964AKCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964AGCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964AHCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964AJCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964BDCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964BKCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964BGCCQ | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964BHCCQ* | 0°C to +70°C | 100 TQFP-EP** |
| MAX9964BJCCQ* | 0°C to +70°C | 100 TQFP-EP** |

*Future product—contact factory for availability.

**EP = Exposed pad.

Pin Configurations appear at end of data sheet.

Selector Guide appears at end of data sheet.



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ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|--|---|-----------------|
| V _{CC} to GND | -0.3V to +11.5V | DLV ₋ to DTV ₋ | ±10V |
| V _{EE} to GND | -7.0V to +0.3V | CHV ₋ or CLV ₋ to DUT ₋ | ±10V |
| All Other Pins | (V _{EE} - 0.3V) to (V _{CC} + 0.3V) | CH ₋ , NCH ₋ , CL ₋ , NCL ₋ to GND | -2.5V to +5V |
| V _{CC} - V _{EE} | -0.3V to +18V | Current into DHV ₋ , DLV ₋ , DTV ₋ , CHV ₋ , CLV ₋ , CPHV ₋ , CPLV ₋ | ±10mA |
| DUT ₋ to GND | -2.5V to +7.5V | Current into TEMP | -0.5mA to +20mA |
| DATA ₋ , NDATA ₋ , RCV ₋ , NRCV ₋ to GND | -2.5V to +5.0V | DUT ₋ Short Circuit to -1.5V to +6.5V | Continuous |
| DATA ₋ to NDATA ₋ | ±1.5V | Power Dissipation (T _A = +70°C) | |
| RCV ₋ to NRCV ₋ | ±1.5V | MAX9963 ₋ CCQ (derate 167mW/°C above T _A = +70°C) | 13.3W* |
| V _{CCO₋} to GND | -0.3V to +5V | MAX9964 ₋ CCQ (derate 47.6mW/°C above T _A = +70°C) | 3.8W* |
| SCLK, DIN, CS, RST to GND | -1.0V to +5V | Storage Temperature Range | -65°C to +150°C |
| DHV ₋ , DLV ₋ , DTV ₋ , CHV ₋ , CLV ₋ to GND | -2.5V to +7.5V | Junction Temperature | +125°C |
| CPHV ₋ to GND | -2.5V to +8.5V | Lead Temperature (soldering, 10s) | +300°C |
| CPLV ₋ to GND | -3.5V to +7.5V | | |
| DHV ₋ to DLV ₋ | ±10V | | |
| DHV ₋ to DTV ₋ | ±10V | | |

*Dissipation wattage values are based on still air with no heat sink for the MAX9963 and slug soldered to board copper for the MAX9964. Actual maximum power dissipation is a function of the user's heat-extraction technique and will vary.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -5.25V, V_{CCO₋} = 2.5V, SC1 = SC0 = 0, V_{CPHV₋} = 7.2V, V_{CPLV₋} = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|---|------|-------|------|-------|
| POWER SUPPLIES | | | | | | |
| Positive Supply | V _{CC} | | 9.5 | 9.75 | 10.5 | V |
| Negative Supply | V _{EE} | | -6.5 | -5.25 | -4.5 | V |
| Positive Supply | I _{CC} | (Note 2) | | 165 | 200 | mA |
| Negative Supply | I _{EE} | (Note 2) | | -320 | -380 | mA |
| Power Dissipation | P _D | Calculated at typical V _{CC} and V _{EE} (Notes 2, 3) | | 3.3 | 4.0 | W |
| DUT₋ CHARACTERISTICS | | | | | | |
| Operating Voltage Range Maximum | V _{DUT} | (Note 4) | -1.5 | | +6.5 | V |
| Leakage Current in High-Z Mode | I _{DUT} | LLEAK = 0, 0V ≤ V _{DUT₋} ≤ 3V | | | ±1.5 | μA |
| | | LLEAK = 0, V _{DUT₋} = -1.5V, 6.5V | | | ±3 | |
| Leakage Current in Low-Leakage Mode | | LLEAK = 1, 0 ≤ V _{DUT₋} ≤ 3V, T _J < +90°C | | | ±10 | nA |
| | | LLEAK = 1, V _{DUT₋} = -1.5V, T _J < +90°C | | | ±15 | |
| | | LLEAK = 1, V _{DUT₋} = 6.5V, V _{CHV₋} = V _{CLV₋} = -1.5V, T _J < +90°C | | | ±15 | |
| Combined Capacitance | C _{DUT} | Driver in term mode (DUT ₋ = DTV ₋) | | 3 | | pF |
| | | Driver in high-Z mode | | 5 | | |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -5.25V, V_{CCO_} = 2.5V, SC1 = SC0 = 0, V_{CPHV_} = 7.2V, V_{CPLV_} = -2.2V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +70°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------------|---|-------|------|-------|-------|
| Low-Leakage Enable Time | | (Notes 5, 7) | | 20 | | μs |
| Low-Leakage Disable Time | | (Notes 6, 7) | | 20 | | μs |
| Low-Leakage Recovery | | Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Note 7) | | 10 | | μs |
| LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_) | | | | | | |
| Input Bias Current | I _{BIAS} | | | | ±25 | μA |
| Settling Time | | T _o 5mV | | 1 | | μs |
| DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_) | | | | | | |
| Input High Voltage | V _{IH} | | -1.6 | | +3.5 | V |
| Input Low Voltage | V _{IL} | | -2.0 | | +3.1 | V |
| Differential Input Voltage | V _{DIFF} | | ±0.15 | | ±1.00 | V |
| Input Bias Current | I _{BIAS} | MAX996_ _DCCQ, MAX996_ _HCCQ | | | ±25 | μA |
| Input Termination Resistor | | MAX996_ _KCCQ, MAX996_ _GCCQ, and MAX996_ _JCCQ, between signal and complement | 96 | | 104 | Ω |
| SINGLE-ENDED CONTROL INPUTS ($\overline{\text{CS}}$, $\overline{\text{RST}}$, SCLK, DIN) | | | | | | |
| Input High | V _{IH} | | 1.6 | | 3.5 | V |
| Input Low | V _{IL} | | -0.1 | | +0.9 | V |
| SERIAL INTERFACE TIMING (Figure 5) | | | | | | |
| SCLK Frequency | f _{SCLK} | | | | 50 | MHz |
| SCLK Pulse Width High | t _{CH} | | 8 | | | ns |
| SCLK Pulse Width Low | t _{CL} | | 8 | | | ns |
| $\overline{\text{CS}}$ Low to SCLK High Setup | t _{CSS0} | | 3.5 | | | ns |
| $\overline{\text{CS}}$ High to SCLK High Setup | t _{CSS1} | | 3.5 | | | ns |
| SCLK High to $\overline{\text{CS}}$ High Hold | t _{CSH1} | | 3.5 | | | ns |
| DIN to SCLK High Setup | t _{DS} | | 3.5 | | | ns |
| DIN to SCLK High Hold | t _{DH} | | 3.5 | | | ns |
| $\overline{\text{CS}}$ Pulse Width High | t _{CSWH} | | 20 | | | ns |
| TEMPERATURE MONITOR (TEMP) | | | | | | |
| Nominal Voltage | | T _J = +70°C, R _L ≥ 10MΩ | | 3.43 | | V |
| Temperature Coefficient | | | | +10 | | mV/°C |
| Output Resistance | | | | 15 | | kΩ |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +9.75V$, $V_{EE} = -5.25V$, $V_{CCO_} = 2.5V$, $SC1 = SC0 = 0$, $V_{CPHV_} = 7.2V$, $V_{CPLV_} = -2.2V$, $T_J = +85^\circ C$, unless otherwise noted. All temperature coefficients are measured at $T_J = +70^\circ C$ to $+100^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|--------------------|--|----------|-------|------|--------|-----|
| DRIVERS (Note 8) | | | | | | | |
| DC OUTPUT CHARACTERISTICS ($R_L \geq 10M\Omega$) | | | | | | | |
| D _{HV_} , D _{LV_} , D _{TV_} , Output Offset Voltage | V _{OS} | At D _{UT_} with V _{DHV_} , V _{DLV_} , V _{DTV_} independently tested at +1.5V | MAX996_A | | ±15 | mV | |
| | | | MAX996_B | | ±100 | | |
| D _{HV_} , D _{LV_} , D _{TV_} , Output Offset Temperature Coefficient | | | | ±65 | | µV/°C | |
| D _{HV_} , D _{LV_} , D _{TV_} , Gain | A _v | Measured with V _{DHV_} , V _{DLV_} , V _{DTV_} at 0 and 4.5V | MAX996_A | 0.999 | 1.00 | 1.001 | V/V |
| | | | MAX996_B | 0.960 | | 1.001 | |
| D _{HV_} , D _{LV_} , D _{TV_} , Gain Temperature Coefficient | | | | -35 | | ppm/°C | |
| Linearity Error | | 0 ≤ V _{DUT_} ≤ 3V (Note 9) | | | ±5 | mV | |
| | | Full range (Notes 9, 10) | | | ±15 | | |
| D _{HV_} to D _{LV_} Crosstalk | | V _{DLV_} = 0, V _{DHV_} = 200mV, 6.5V | | | ±7 | mV | |
| D _{LV_} to D _{HV_} Crosstalk | | V _{DHV_} = 5V, V _{DLV_} = -1.5V, 4.8V | | | ±8 | mV | |
| D _{TV_} to D _{LV_} and D _{HV_} Crosstalk | | V _{DHV_} = 3V, V _{DLV_} = 0, V _{DTV_} = -1.5V, 6.5V | | | ±2 | mV | |
| D _{HV_} to D _{TV_} Crosstalk | | V _{DTV_} = 1.5V, V _{DLV_} = 0, V _{DHV_} = 1.6V, 3V | | | ±3 | mV | |
| D _{LV_} to D _{TV_} Crosstalk | | V _{DTV_} = 1.5V, V _{DHV_} = 3V, V _{DLV_} = 0, 1.4V | | | ±3 | mV | |
| D _{HV_} , D _{LV_} , D _{TV_} DC Power-Supply Rejection Ratio | PSRR | V _{CC} and V _{EE} independently set to their minimum and maximum values | 40 | | | dB | |
| Maximum DC Drive Current | I _{DUT_} | | ±60 | | ±120 | mA | |
| DC Output Resistance | R _{DUT_} | I _{DUT_} = ±30mA (Note 11) | 49 | 50 | 51 | Ω | |
| DC Output Resistance Variation | ΔR _{DUT_} | I _{DUT_} = ±1mA to ±40mA | | 1 | | Ω | |
| DYNAMIC OUTPUT CHARACTERISTICS (Z _L = 50Ω) | | | | | | | |
| Drive Mode Overshoot | | V _{DLV_} = 0V, V _{DHV_} = 0.1V | | 30 | | mV | |
| | | V _{DLV_} = 0V, V _{DHV_} = 1V | | 40 | | | |
| | | V _{DLV_} = 0V, V _{DHV_} = 3V | | 50 | | | |
| Term Mode Overshoot | | (Note 12) | | 0 | | mV | |
| Settling Time to Within 25mV | | 3V step (Note 13) | | 10 | | ns | |
| Settling Time to Within 5mV | | 3V step (Note 13) | | 20 | | ns | |

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ELECTRICAL CHARACTERISTICS (continued)

(VCC = +9.75V, VEE = -5.25V, VCCO_ = 2.5V, SC1 = SC0 = 0, VCPHV_ = 7.2V, VCPLV_ = -2.2V, TJ = +85°C, unless otherwise noted. All temperature coefficients are measured at TJ = +70°C to +100°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|---|-----|------|-----|-------|
| TIMING CHARACTERISTICS (Note 14) (ZL = 50Ω) | | | | | | |
| Prop Delay, Data to Output | tPDD | | | 2 | | ns |
| Prop Delay Match, tLH vs. tHL | | 3VP-P | | ±50 | | ps |
| Prop Delay Match, Drivers Within Package | | (Note 15) | | 40 | | ps |
| Prop Delay Temperature Coefficient | | | | +3 | | ps/°C |
| Prop Delay Change vs. Pulse Width | | 3VP-P, 40MHz, 2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width | | ±60 | | ps |
| Prop Delay Change vs. Common-Mode Voltage | | V _{DHV_} - V _{DLV_} = 1V, V _{DHV_} = 0 to 6V | | 85 | | ps |
| Prop Delay, Drive to High-Z | tPDDZ | V _{DHV_} = 1.0V, V _{DLV_} = -1.0V, V _{DTV_} = 0 | | 2.9 | | ns |
| Prop Delay, High-Z to Drive | tPDZD | V _{DHV_} = 1.0V, V _{DLV_} = -1.0V, V _{DTV_} = 0 | | 2.9 | | ns |
| Prop Delay, Drive to Term | tPDDT | V _{DHV_} = 3V, V _{DLV_} = 0, V _{DTV_} = 1.5V | | 2.2 | | ns |
| Prop Delay, Term to Drive | tPDTD | V _{DHV_} = 3V, V _{DLV_} = 0, V _{DTV_} = 1.5V | | 1.8 | | ns |
| DYNAMIC PERFORMANCE (ZL = 50Ω) | | | | | | |
| Rise and Fall Time | tR, tF | 0.2VP-P, 20% to 80% | | 330 | | ps |
| | | 1VP-P, 10% to 90% | | 670 | | |
| | | 3VP-P, 10% to 90% | 1.1 | 1.3 | 1.6 | ns |
| | | 5VP-P, 10% to 90% | | 2.0 | | |
| SC1 = 0, SC0 = 1 Slew Rate | | Percent of full speed (SC0 = SC1 = 0), 3VP-P, 20% to 80% | | 75 | | % |
| SC1 = 1, SC0 = 0 Slew Rate | | Percent of full speed (SC0 = SC1 = 0), 3VP-P, 20% to 80% | | 50 | | % |
| SC1 = 1, SC0 = 1 Slew Rate | | Percent of full speed (SC0 = SC1 = 0), 3VP-P, 20% to 80% | | 25 | | % |
| Minimum Pulse Width (Note 16) | | 0.2VP-P | | 650 | | ps |
| | | 1VP-P | | 1.0 | | ns |
| | | 3VP-P | | 2.0 | | |
| | | 5VP-P | | 2.9 | | |
| Data Rate (Note 17) | | 0.2VP-P | | 1700 | | Mbps |
| | | 1VP-P | | 1000 | | |
| | | 3VP-P | | 500 | | |
| | | 5VP-P | | 350 | | |
| Dynamic Crosstalk | | (Note 18) | | 20 | | mVP-P |
| Rise and Fall Time, Drive to Term | tDTR, tDTF | V _{DHV_} = 3V, V _{DLV_} = 0, V _{DTV_} = 1.5V, 10% to 90% (Note 19) | | 1.6 | | ns |
| Rise and Fall Time, Term to Drive | tTDR, tTDF | V _{DHV_} = 3V, V _{DLV_} = 0, V _{DTV_} = 1.5V, 10% to 90% (Note 19) | | 0.7 | | ns |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +9.75V$, $V_{EE} = -5.25V$, $V_{CCO_} = 2.5V$, $SC1 = SC0 = 0$, $V_{CPHV_} = 7.2V$, $V_{CPLV_} = -2.2V$, $T_J = +85^{\circ}C$, unless otherwise noted. All temperature coefficients are measured at $T_J = +70^{\circ}C$ to $+100^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---------------|---|---------------------------------|---------|-----------|-----------|-------------------|
| COMPARATORS (Note 20) | | | | | | | |
| DC CHARACTERISTICS | | | | | | | |
| Input Voltage Range | V_{IN} | (Note 4) | | -1.5 | | +6.5 | V |
| Differential Input Voltage | V_{DIFF} | | | ± 8 | | | V |
| Hysteresis | V_{HYST} | | | | 0 | | mV |
| Input Offset Voltage | V_{OS} | $V_{DUT_} = 1.5V$ | MAX996_A | | | ± 15 | mV |
| | | | MAX996_B | | | ± 100 | |
| Input Offset Voltage Temperature Coefficient | | | | | ± 50 | | $\mu V/^{\circ}C$ |
| Common-Mode Rejection Ratio (Note 21) | CMRR | $V_{DUT_} = 0, 3V$ | | 47 | 78 | | dB |
| | | $V_{DUT_} = 0, 6.5V$ | | 54 | 78 | | |
| | | $V_{DUT_} = -1.5V, 6.5V$ | | 44 | 61 | | |
| Linearity Error (Note 9) | | $V_{DUT_} = 0$ to 3V | | | ± 3 | | mV |
| | | $V_{DUT_} = 6.5V$ | | | | ± 15 | |
| | | $V_{DUT_} = -1.5V$ | | | | ± 25 | |
| V_{CC} Power-Supply Rejection Ratio | PSRR | $V_{DUT_} = -1.5V, 6.5V$ (Note 22) | | 57 | 82 | | dB |
| V_{EE} Power-Supply Rejection Ratio (Note 22) | PSRR | $V_{DUT_} = 0, 6.5V$ | | 44 | 70 | | dB |
| | | $V_{DUT_} = -1.5V$ | | 33 | 45 | | |
| AC CHARACTERISTICS (Note 23) | | | | | | | |
| Minimum Pulse Width | $t_{PW(min)}$ | (Note 24) | MAX996_ _GCCQ | | 0.75 | | ns |
| | | | MAX996_ _HCCQ, MAX996_ _JCCQ | | 1.3 | | |
| Prop Delay | t_{PDL} | | | | 2.2 | | ns |
| Prop Delay Temperature Coefficient | | | | | +6 | | ps/ $^{\circ}C$ |
| Prop Delay Match, High/Low vs. Low/High | | | | | ± 25 | | ps |
| Prop Delay Match, Comparators Within Package | | (Note 15) | | | 35 | | ps |
| Prop Delay Dispersion vs. Common-Mode Input (Note 25) | | $V_{CHV_} = V_{CLV_} = 0, 6.4V$ | | | ± 75 | | ps |
| | | $V_{CHV_} = V_{CLV_} = -1.4V$ | | | ± 175 | | |
| Prop Delay Dispersion vs. Overdrive | | 100mV to 2V | | | 200 | | ps |
| Prop Delay Dispersion vs. Pulse Width | | 2.5ns to 22.5ns pulse width, relative to 12.5ns pulse width | MAX996_ _GCCQ | | ± 35 | | ps |
| | | | MAX996_ _HCCQ, MAX996_ _JCCQ | | ± 70 | | |
| Prop Delay Dispersion vs. Slew Rate | | 0.5V/ns to 2V/ns slew rate | | | 100 | | ps |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +9.75V$, $V_{EE} = -5.25V$, $V_{CCO_} = 2.5V$, $SC1 = SC0 = 0$, $V_{CPHV_} = 7.2V$, $V_{CPLV_} = -2.2V$, $T_J = +85^\circ C$, unless otherwise noted. All temperature coefficients are measured at $T_J = +70^\circ C$ to $+100^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------|---|--------------------|--------------------|--------------------|----------------|
| Waveform Tracking 10% to 90% | | $V_{DUT_} = 1.0V_{P-P}$, $t_R = t_F = 1.0ns$ 10% to 90%, relative to timing at 50% point | Term mode | 250 | | ps |
| | | | High-Z mode | 500 | | |
| OPEN-COLLECTOR LOGIC OUTPUTS ($CH_$, $NCH_$, $CL_$, $NCL_$: MAX996_ $_DCCQ$, MAX996_ $_KCCQ$, and MAX996_ $_GCCQ$) | | | | | | |
| $V_{CCO_}$ Voltage Range | $V_{VCCO_}$ | | 0 | 3.5 | | V |
| Output Low-Voltage Compliance | | Set by I_{OUT} , R_{TERM} , and $V_{CCO_}$ | -0.5 | | | V |
| Output High Voltage | V_{OH} | $I_{CH_} = I_{NCH_} = I_{CL_} = I_{NCL_} = 0mA$, MAX996_ $_GCCQ$ | $V_{CCO_} - 0.10$ | $V_{CCO_} - 0.04$ | | V |
| Output Low Voltage | V_{OL} | $I_{CH_} = I_{NCH_} = I_{CL_} = I_{NCL_} = 0mA$, MAX996_ $_GCCQ$ | | | $V_{CCO_} - 0.38$ | V |
| Output Voltage Swing | | | 0.30 | 0.33 | 0.40 | V |
| Termination Resistor | R_{TERM} | Single-ended measurement from $V_{CCO_}$ to $CH_$, $NCH_$, $CL_$, $NCL_$, MAX996_ $_GCCQ$ | 47.5 | 52.5 | | Ω |
| Differential Rise Time | t_R | 20% to 80% | 350 | | | ps |
| Differential Fall Time | t_F | 20% to 80% | 350 | | | ps |
| OPEN-EMITTER LOGIC OUTPUTS ($CH_$, $NCH_$, $CL_$, $NCL_$: MAX996_ $_HCCQ$ and MAX996_ $_JCCQ$) | | | | | | |
| $V_{CCO_}$ Voltage Range | $V_{VCCO_}$ | | -0.1 | +3.5 | | V |
| $V_{CCO_}$ Supply Current | $I_{VCCO_}$ | All outputs 50Ω to ($V_{VCCO_} - 2V$) | 330 | | | mA |
| Output High Voltage | V_{OH} | 50Ω to ($V_{VCCO_} - 2V$) | $V_{CCO_} - 0.9$ | | | V |
| Output Low Voltage | V_{OL} | 50Ω to ($V_{VCCO_} - 2V$) | $V_{CCO_} - 1.7$ | | | V |
| Output Voltage Swing | | 50Ω to ($V_{VCCO_} - 2V$) | 750 | 850 | 950 | mV |
| Differential Rise Time | t_R | 20% to 80% | 600 | | | ps |
| Differential Fall Time | t_F | 20% to 80% | 600 | | | ps |
| CLAMPS | | | | | | |
| High Clamp Input Voltage Range | $V_{CPH_}$ | | -0.3 | +7.5 | | V |
| Low Clamp Input Voltage Range | $V_{CPL_}$ | | -2.5 | +5.3 | | V |
| Clamp Offset Voltage | V_{OS} | At DUT_ with $I_{DUT_} = 1mA$, $V_{CPHV_} = 0$ | | | ± 100 | mV |
| | | At DUT_ with $I_{DUT_} = -1mA$, $V_{CPLV_} = 0$ | | | ± 100 | |
| Offset Voltage Temperature Coefficient | | | ± 0.5 | | | mV/ $^\circ C$ |
| Clamp Power-Supply Rejection | PSRR | V_{CC} and V_{EE} independently varied full range, $I_{DUT_} = 1mA$, $V_{CPHV_} = 0$ | 40 | | | dB |
| | | V_{CC} and V_{EE} independently varied full range, $I_{DUT_} = -1mA$, $V_{CPLV_} = 0$ | 40 | | | |

Quad, Low-Power, 500Mbps ATE Driver/Comparator

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +9.75V$, $V_{EE} = -5.25V$, $V_{CCO_} = 2.5V$, $SC1 = SC0 = 0$, $V_{CPHV_} = 7.2V$, $V_{CPLV_} = -2.2V$, $T_J = +85^{\circ}C$, unless otherwise noted. All temperature coefficients are measured at $T_J = +70^{\circ}C$ to $+100^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|--------|--|------|----------|------|------------------|
| Voltage Gain | A_V | | 0.96 | | 1.00 | V/V |
| Voltage-Gain Temperature Coefficient | | | | -100 | | ppm/ $^{\circ}C$ |
| Clamp Linearity | | $I_{DUT} = 1mA$, $V_{CPLV_} = -1.5V$, $V_{CPHV_} = -0.3$ to $6.5V$ | | ± 10 | | mV |
| | | $I_{DUT} = -1mA$, $V_{CPHV_} = 6.5V$, $V_{CPLV_} = -1.5$ to $5.3V$ | | ± 10 | | |
| Short-Circuit Output Current | | $V_{CPHV_} = 0$, $V_{CPLV_} = -1.5V$, $V_{DUT_} = 6.0V$ | 50 | | 95 | mA |
| | | $V_{CPLV_} = 5V$, $V_{CPHV_} = 6.5V$, $V_{DUT_} = -1.0V$ | -95 | | -50 | |
| Clamp DC Impedance | | $V_{CPHV_} = 3V$, $V_{CPLV_} = 0$, $I_{DUT} = -5mA$ and $-15mA$ | 50 | | 55 | Ω |
| | | $V_{CPHV_} = 3V$, $V_{CPLV_} = 0$, $I_{DUT} = 5mA$ and $15mA$ | 50 | | 55 | |

Note 1: All MIN and MAX limits are 100% tested in production.

Note 2: Total for quad device at worst-case setting. $R_L \geq 10M\Omega$. The applicable supply currents are measured with typical supply voltages.

Note 3: Does not include internal dissipation of the comparator outputs. With output loads of 50Ω to $(V_{VCCO_} - 2V)$, this adds $240mW$ (typ) to the total chip power (MAX996__{HCCQ}, MAX996__{JCCQ}).

Note 4: Externally forced voltages may exceed this range provided that the absolute maximum ratings are not exceeded.

Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 6: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 7: Based on simulation results only.

Note 8: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 9: Relative to straight line between 0 and 3V.

Note 10: Full ranges are $-1.3V \leq V_{DHFV_} \leq 6.5V$, $-1.5V \leq V_{DTV_} \leq 6.5V$, $-1.5V \leq V_{DLV_} \leq 6.3V$.

Note 11: Nominal target value is 50Ω . Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 12: $V_{DTV_} = 1.5V$, $R_S = 50\Omega$. External signal driven into T-line is a 0 to 3V edge with 1.2ns rise time (10% to 90%). Measurement is made using the comparator.

Note 13: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 14: Prop delays are measured from the crossing point of the differential input signals to the 50% point of expected output swing. Rise time of the differential inputs DATA_ and RCV_ is 250ps (10% to 90%).

Quad, Low-Power, 500Mbps ATE Driver/Comparator

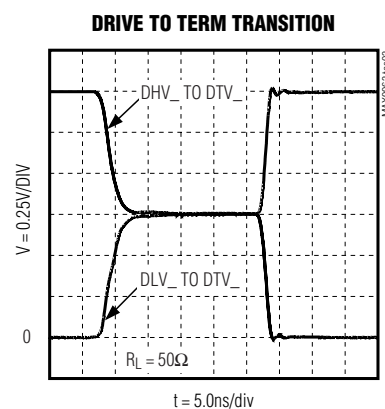
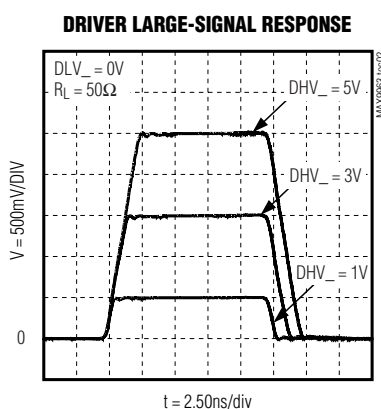
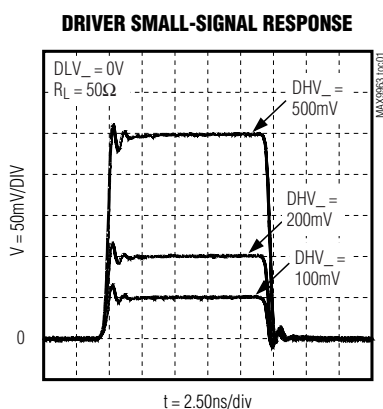
MAX9963/MAX9964

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +9.75V$, $V_{EE} = -5.25V$, $V_{CCO_} = 2.5V$, $SC1 = SC0 = 0$, $V_{CPHV_} = 7.2V$, $V_{CPLV_} = -2.2V$, $T_J = +85^\circ C$, unless otherwise noted. All temperature coefficients are measured at $T_J = +70^\circ C$ to $+100^\circ C$, unless otherwise noted.) (Note 1)

- Note 15:** Rising edge to rising edge or falling edge to falling edge.
- Note 16:** Specified amplitude is programmed. At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at $DATA_$.
- Note 17:** Specified amplitude is programmed. Maximum data rate specified in transitions per second. A square wave that reaches at least 95% of its programmed amplitude may be generated at one-half this frequency.
- Note 18:** Crosstalk from any driver to the other three channels. Aggressor channel is driving 3V_{P-P} into a 50Ω load. Victim channels are in term mode with $V_{DTV_} = 1.5V$.
- Note 19:** Indicative of switching speed from $DHV_$ or $DLV_$ to $DTV_$ and $DTV_$ to $DHV_$ or $DLV_$ when $V_{DLV_} < V_{DTV_} < V_{DHV_}$. If $V_{DTV_} < V_{DLV_}$ or $V_{DTV_} > V_{DHV_}$, switching speed is degraded by approximately a factor of 3.
- Note 20:** Both high and low comparators are tested.
- Note 21:** Change in offset voltage over input range.
- Note 22:** Change in offset voltage with power supplies independently set to their minimum and maximum values.
- Note 23:** Unless otherwise noted, all prop delays are measured at 40MHz, $V_{DUT_} = 0$ to 2V, $V_{CHV_} = V_{CLV_} = 1V$, slew rate = 2V/ns, $Z_S = 50\Omega$, driver in term mode with $V_{DTV_} = 0V$. Comparator outputs are terminated with 50Ω to GND at scope input with $V_{CCO_} = 2V$. Open-collector outputs are also terminated (internally or externally) with $R_{TERM} = 50\Omega$ to $V_{CCO_}$. Measured from $V_{DUT_}$ crossing calibrated $CHV_/CLV_$ threshold to the crossing point of differential outputs.
- Note 24:** $V_{DUT_} = 0$ to 1V, $V_{CHV_} = V_{CLV_} = 0.5V$. At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.
- Note 25:** Relative to propagation delay at $V_{CHV_} = V_{CLV_} = 1.5V$. $V_{DUT_} = 200mV_{P-P}$. Overdrive = 100mV.

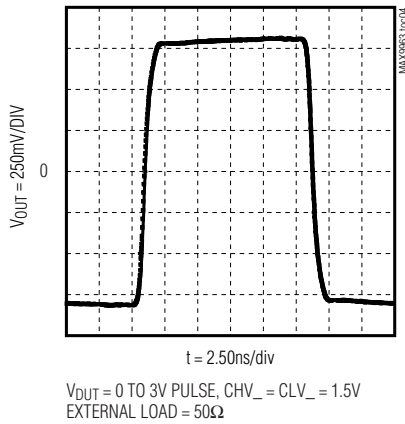
Typical Operating Characteristics



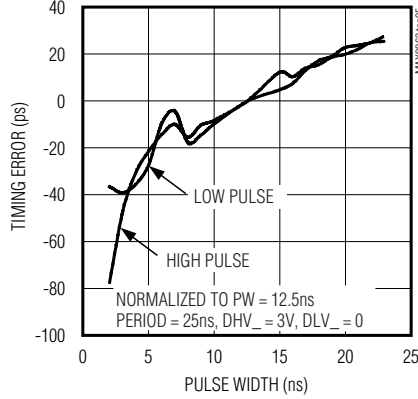
Quad, Low-Power, 500Mbps ATE Driver/Comparator

Typical Operating Characteristics (continued)

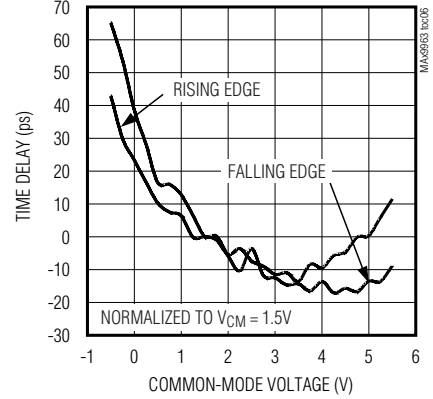
COMPARATOR DIFFERENTIAL OUTPUT RESPONSE, MAX996__JCCQ



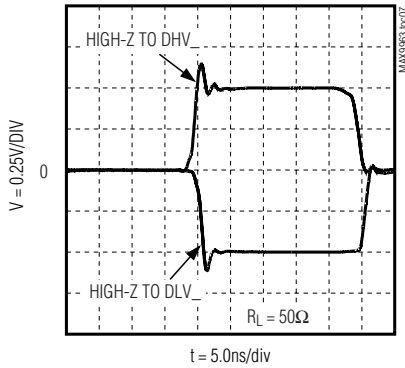
DRIVER TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



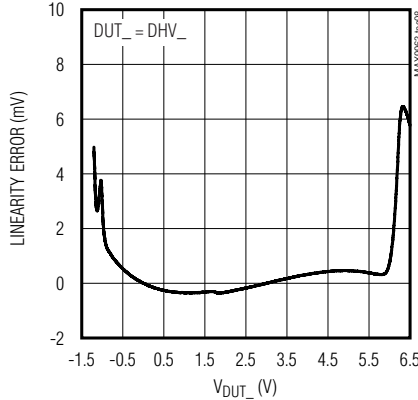
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



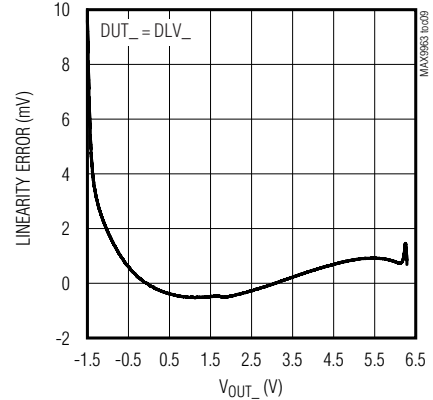
HIGH-Z TO DRIVE TRANSITION



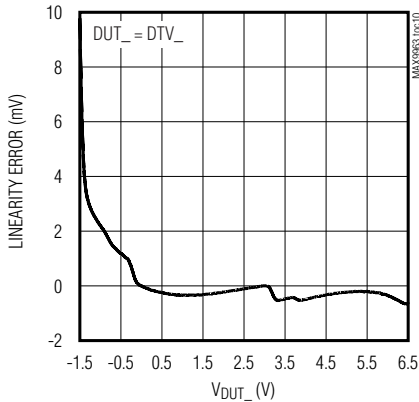
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



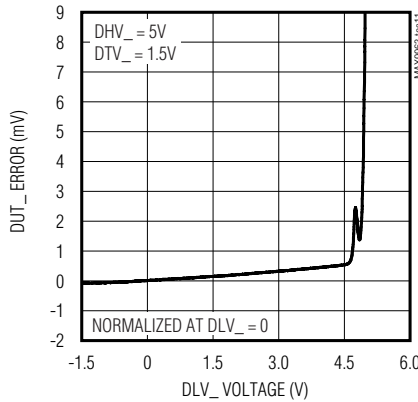
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



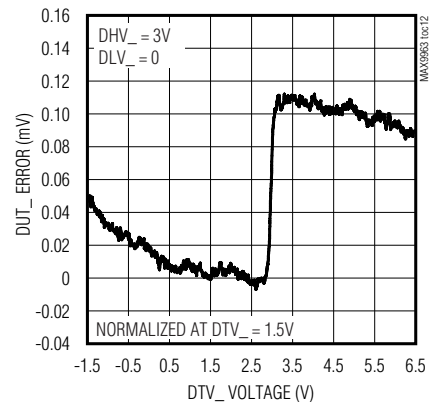
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



CROSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



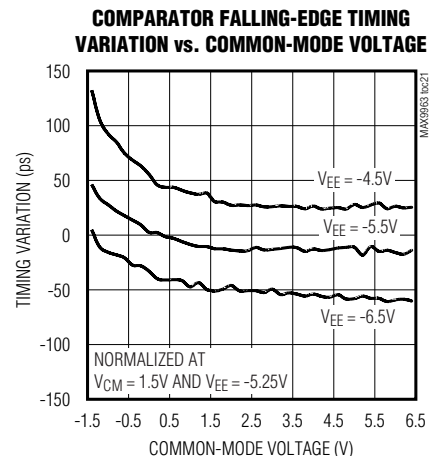
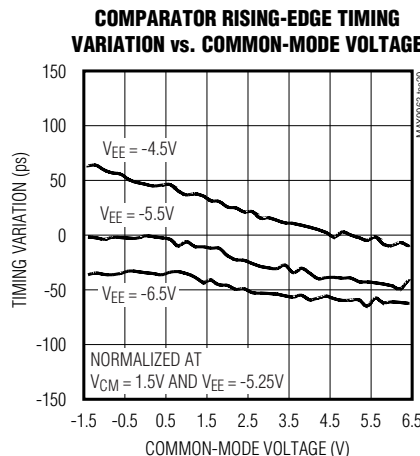
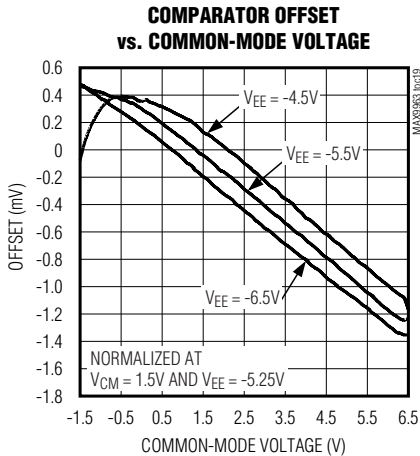
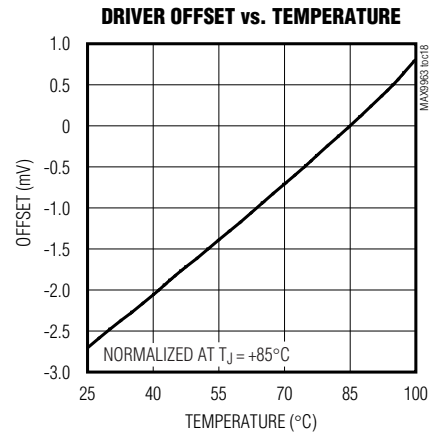
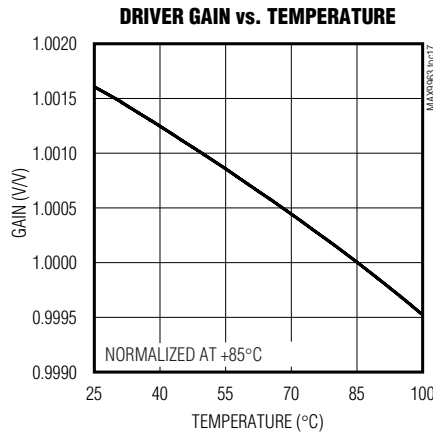
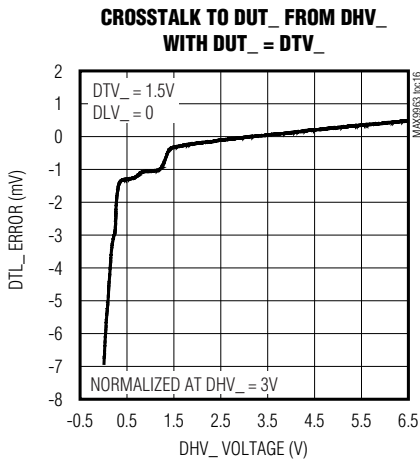
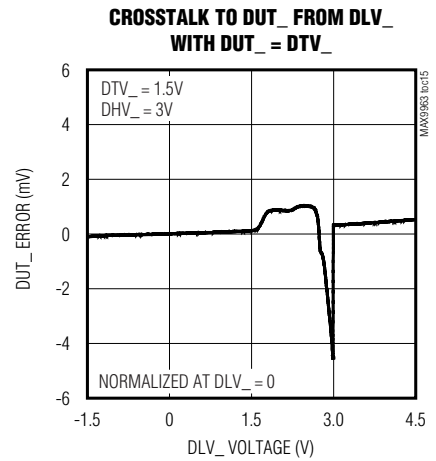
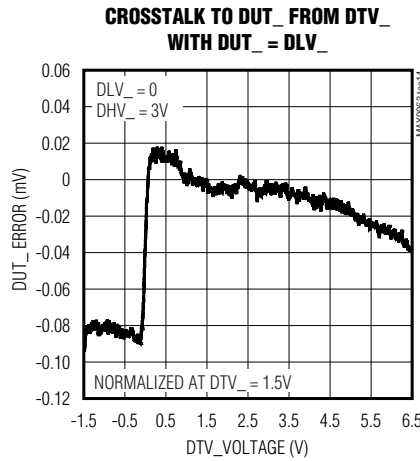
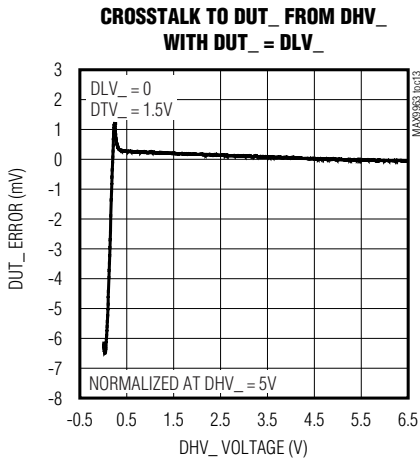
CROSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



Quad, Low-Power, 500Mbps ATE Driver/Comparator

Typical Operating Characteristics (continued)

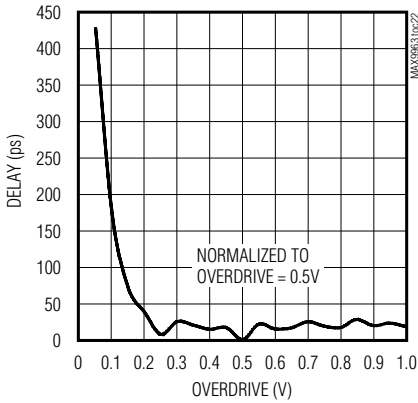
MAX9963/MAX9964



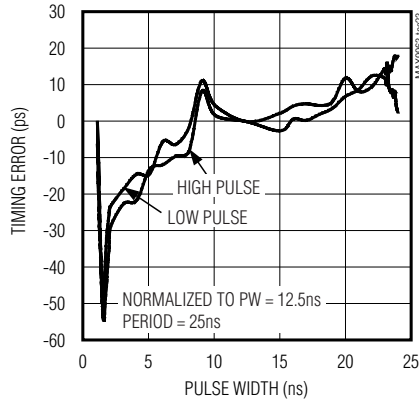
Quad, Low-Power, 500Mbps ATE Driver/Comparator

Typical Operating Characteristics (continued)

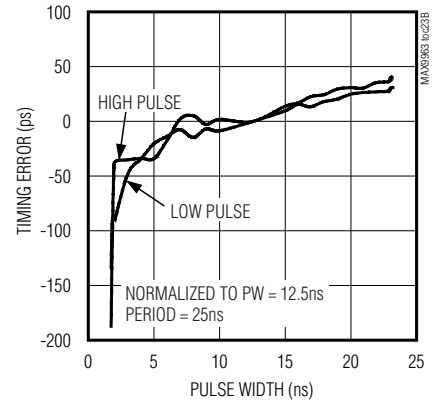
COMPARATOR TIMING VARIATION vs. OVERDRIVE



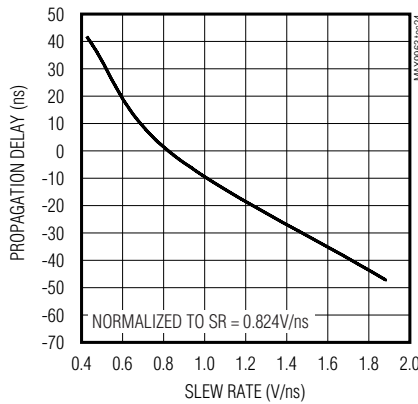
COMPARATOR TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH, MAX996_GCCQ



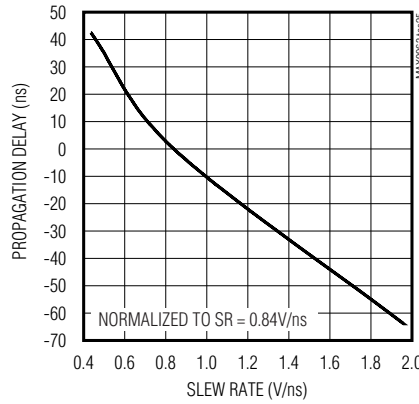
COMPARATOR TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH, MAX996_JCCQ



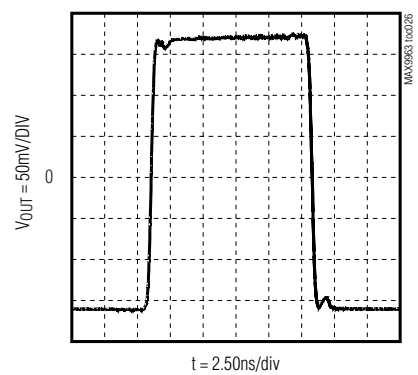
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_RISING



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE, DUT_FALLING

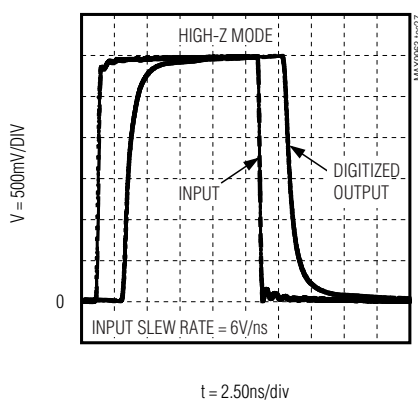


COMPARATOR DIFFERENTIAL OUTPUT RESPONSE, MAX996_GCCQ

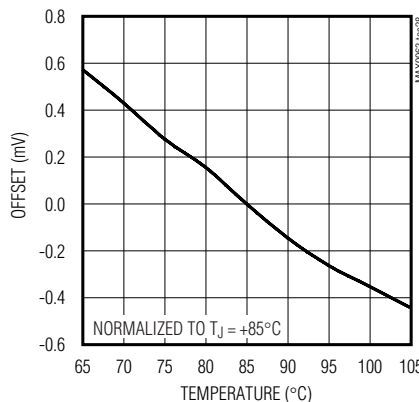


V_{OUT} = 0 TO 3V PULSE, CHV₋ = CLV₋ = 1.5V
EXTERNAL LOAD = 50Ω

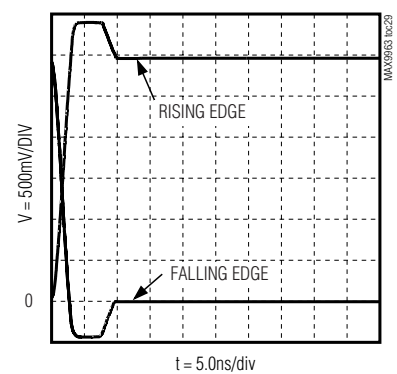
COMPARATOR RESPONSE vs. HIGH SLEW RATE OVERDRIVE



COMPARATOR OFFSET vs. TEMPERATURE



CLAMP RESPONSE

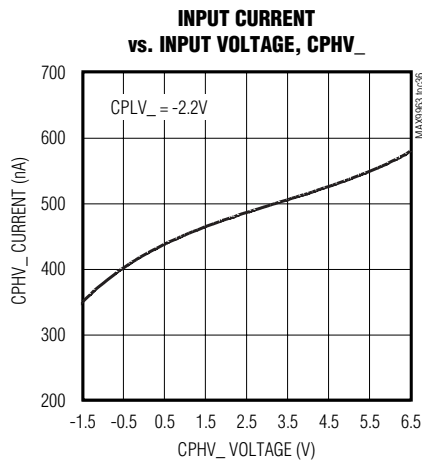
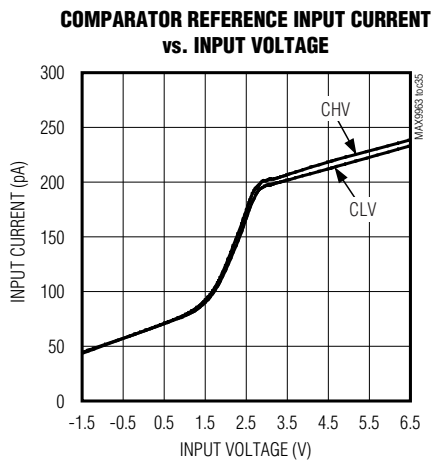
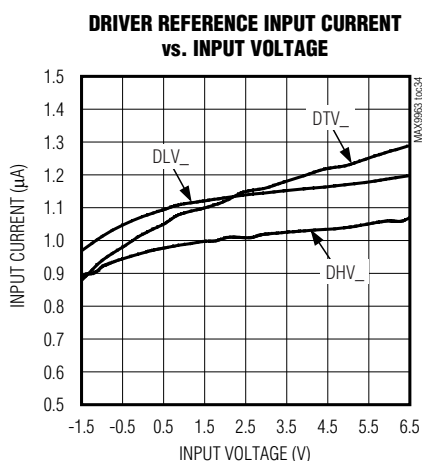
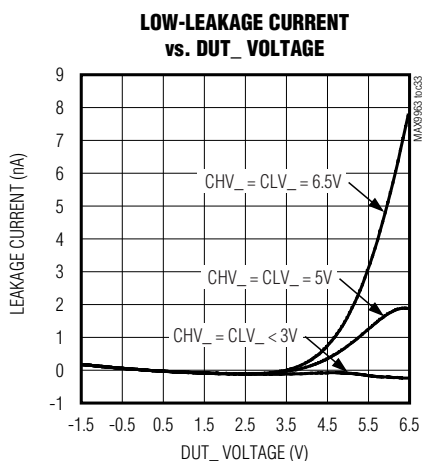
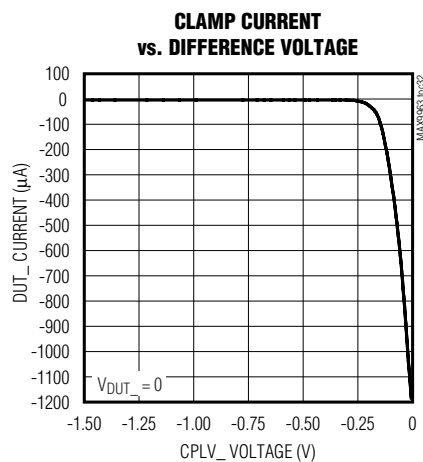
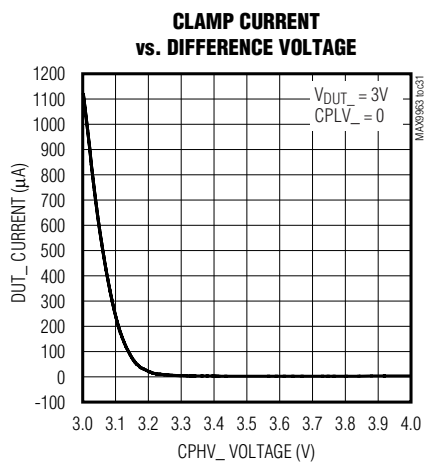
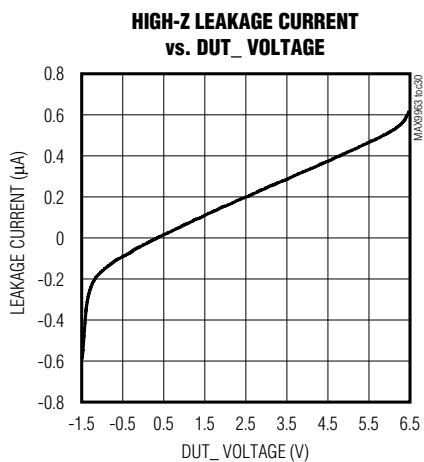


V_{OUT} = 0 TO 3V SQUARE WAVE
R_S = 25Ω
CPLV₋ = -0.1V, CPHV₋ = +3.1V

Quad, Low-Power, 500Mbps ATE Driver/Comparator

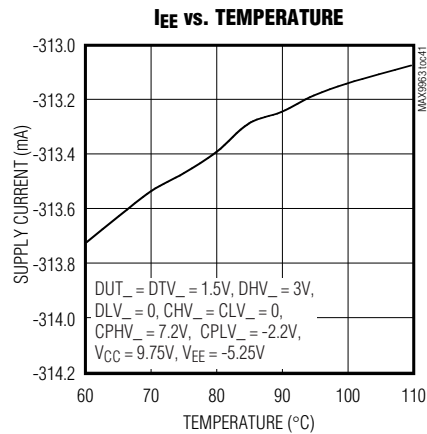
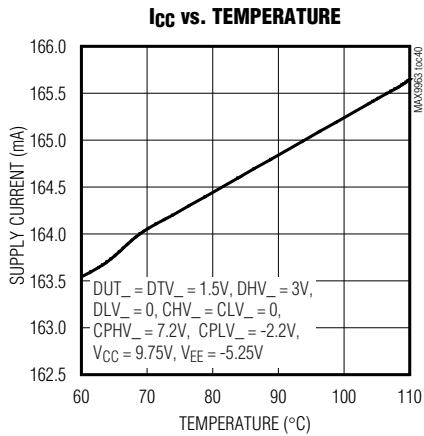
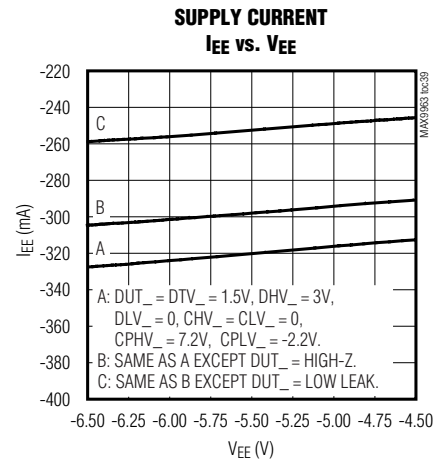
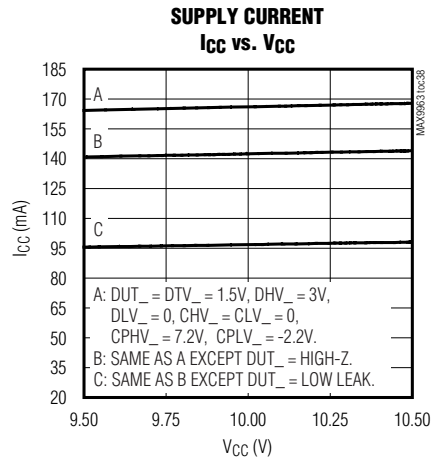
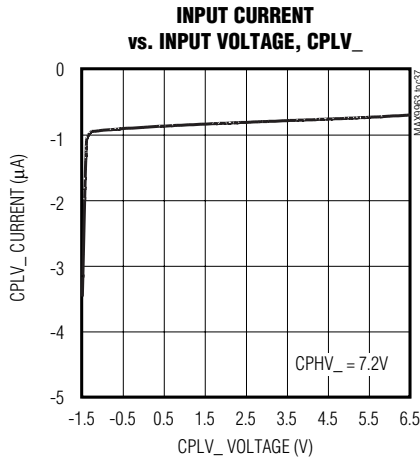
Typical Operating Characteristics (continued)

MAX9963/MAX9964



Quad, Low-Power, 500Mbps ATE Driver/Comparator

Typical Operating Characteristics (continued)



Quad, Low-Power, 500Mbps ATE Driver/Comparator

Pin Description

MAX9963/MAX9964

| PIN | | NAME | FUNCTION |
|--|--|-------------------------|--|
| MAX9963 | MAX9964 | | |
| 1 | 25 | VCCO34 | Collector Voltage Input, Channels 3 and 4. For open-collector outputs, this is the pullup voltage for the internal termination resistors. For open-emitter outputs, this is the collector voltage of the output transistors. Not internally connected on open-collector versions without internal termination resistors. VCCO34 services both channel 3 and channel 4. |
| 2 | 24 | DATA4 | Channel 4 Multiplexer Control Inputs. Differential controls DATA4 and NDATA4 select driver 4's input from DHV4 or DLV4. Drive DATA4 above NDATA4 to select DHV4. Drive NDATA4 above DATA4 to select DLV4. |
| 3 | 23 | NDATA4 | |
| 4 | 22 | RCV4 | Channel 4 Multiplexer Control Inputs. Differential controls RCV4 and NRCV4 place channel 4 into receive mode. Drive RCV4 above NRCV4 to place channel 4 into receive mode. Drive NRCV4 above RCV4 to place channel 4 into drive mode. |
| 5 | 21 | NRCV4 | |
| 6 | 20 | DATA3 | Channel 3 Multiplexer Control Inputs. Differential controls DATA3 and NDATA3 select driver 3's input from DHV3 or DLV3. Drive DATA3 above NDATA3 to select DHV3. Drive NDATA3 above DATA3 to select DLV3. |
| 7 | 19 | NDATA3 | |
| 8 | 18 | RCV3 | Channel 3 Multiplexer Control Inputs. Differential controls RCV3 and NRCV3 place channel 3 into receive mode. Drive RCV3 above NRCV3 to place channel 3 into receive mode. Drive NRCV3 above RCV3 to place channel 3 into drive mode. |
| 9 | 17 | NRCV3 | |
| 10, 27, 54, 55, 60, 61, 65, 66, 71, 72, 99 | 16, 27, 54, 55, 60, 61, 65, 66, 71, 72, 99 | V _{EE} | Negative Power-Supply Input |
| 11, 28, 51, 56, 62, 64, 70, 75, 98 | 15, 28, 51, 56, 62, 64, 70, 75, 98 | GND | Ground Connection |
| 12 | 14 | $\overline{\text{RST}}$ | Reset Input. Asynchronous reset input for the serial register. $\overline{\text{RST}}$ is active low and asserts low-leakage mode. At power-up, hold $\overline{\text{RST}}$ low until V _{CC} and V _{EE} have stabilized. |
| 13 | 13 | $\overline{\text{CS}}$ | Chip-Select Input. Serial-port activation input. $\overline{\text{CS}}$ is active low. |
| 14 | 12 | SCLK | Serial Clock Input. Clock for serial port. |
| 15 | 11 | DIN | Data Input. Serial port data input. |
| 16, 26, 52, 58, 68, 74, 100 | 10, 26, 52, 58, 68, 74, 100 | V _{CC} | Positive Power-Supply Input |
| 17 | 9 | NRCV2 | Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 into receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode. |
| 18 | 8 | RCV2 | |
| 19 | 7 | NDATA2 | Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2. |
| 20 | 6 | DATA2 | |

Quad, Low-Power, 500Mbps ATE Driver/Comparator

Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---------|---------|--------|--|
| MAX9963 | MAX9964 | | |
| 21 | 5 | NRCV1 | Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 into receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode. |
| 22 | 4 | RCV1 | |
| 23 | 3 | NDATA1 | Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1. |
| 24 | 2 | DATA1 | |
| 25 | 1 | VCCO12 | Collector Voltage Input, Channels 1 and 2. For open-collector outputs, this is the pullup voltage for the internal termination resistors. For open-emitter outputs, this is the collector voltage of the output transistors. Not internally connected on open-collector versions without internal termination resistors. VCCO12 services both channel 1 and channel 2. |
| 29 | 97 | NCL2 | Channel 2 Low-Comparator Output. Differential output of channel 2 low comparator. |
| 30 | 96 | CL2 | |
| 31 | 95 | NCH2 | Channel 2 High-Comparator Output. Differential output of channel 2 high comparator. |
| 32 | 94 | CH2 | |
| 33 | 93 | NCL1 | Channel 1 Low-Comparator Output. Differential output of channel 1 low comparator. |
| 34 | 92 | CL1 | |
| 35 | 91 | NCH1 | Channel 1 High-Comparator Output. Differential output of channel 1 high comparator. |
| 36 | 90 | CH1 | |
| 37 | 89 | CPHV2 | Channel 2 High-Clamp Reference Input |
| 38 | 88 | CPLV2 | Channel 2 Low-Clamp Reference Input |
| 39 | 87 | DHV2 | Channel 2 Driver-High Reference Input |
| 40 | 86 | DLV2 | Channel 2 Driver-Low Reference Input |
| 41 | 85 | DTV2 | Channel 2 Driver-Termination Reference Input |
| 42 | 84 | CHV2 | Channel 2 High-Comparator Reference Input |
| 43 | 83 | CLV2 | Channel 2 Low-Comparator Reference Input |
| 44 | 82 | CPHV1 | Channel 1 High-Clamp Reference Input |
| 45 | 81 | CPLV1 | Channel 1 Low-Clamp Reference Input |
| 46 | 80 | DHV1 | Channel 1 Driver-High Reference Input |
| 47 | 79 | DLV1 | Channel 1 Driver-Low Reference Input |
| 48 | 78 | DTV1 | Channel 1 Driver-Termination Reference Input |
| 49 | 77 | CHV1 | Channel 1 High-Comparator Reference Input |
| 50 | 76 | CLV1 | Channel 1 Low-Comparator Reference Input |
| 53 | 73 | DUT1 | Channel 1 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp. |
| 57, 69 | 57, 69 | N.C. | No Connection. Leave open. |
| 59 | 67 | DUT2 | Channel 2 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp. |
| 63 | 63 | TEMP | Temperature Monitor Output |

Quad, Low-Power, 500Mbps ATE Driver/Comparator

Pin Description (continued)

MAX9963/MAX9964

| PIN | | NAME | FUNCTION |
|---------|---------|-------|---|
| MAX9963 | MAX9964 | | |
| 67 | 59 | DUT3 | Channel 3 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp. |
| 73 | 53 | DUT4 | Channel 4 Device Under Test Input/Output. Combined I/O for driver, comparator, and clamp. |
| 76 | 50 | CLV4 | Channel 4 Low-Comparator Reference Input |
| 77 | 49 | CHV4 | Channel 4 High-Comparator Reference Input |
| 78 | 48 | DTV4 | Channel 4 Driver-Termination Reference Input |
| 79 | 47 | DLV4 | Channel 4 Driver-Low Reference Input |
| 80 | 46 | DHV4 | Channel 4 Driver-High Reference Input |
| 81 | 45 | CPLV4 | Channel 4 Low-Clamp Reference Input |
| 82 | 44 | CPHV4 | Channel 4 High-Clamp Reference Input |
| 83 | 43 | CLV3 | Channel 3 Low-Comparator Reference Input |
| 84 | 42 | CHV3 | Channel 3 High-Comparator Reference Input |
| 85 | 41 | DTV3 | Channel 3 Driver-Termination Reference Input |
| 86 | 40 | DLV3 | Channel 3 Driver-Low Reference Input |
| 87 | 39 | DHV3 | Channel 3 Driver-High Reference Input |
| 88 | 38 | CPLV3 | Channel 3 Low-Clamp Reference Input |
| 89 | 37 | CPHV3 | Channel 3 High-Clamp Reference Input |
| 90 | 36 | CH4 | Channel 4 High-Comparator Output. Differential output of channel 4 high comparator. |
| 91 | 35 | NCH4 | |
| 92 | 34 | CL4 | Channel 4 Low-Comparator Output. Differential output of channel 4 low comparator. |
| 93 | 33 | NCL4 | |
| 94 | 32 | CH3 | Channel 3 High-Comparator Output. Differential output of channel 3 high comparator. |
| 95 | 31 | NCH3 | |
| 96 | 30 | CL3 | Channel 3 Low-Comparator Output. Differential output of channel 3 low comparator. |
| 97 | 29 | NCL3 | |

Detailed Description

The MAX9963/MAX9964 four-channel, high-speed pin electronics driver and comparator ICs for automatic test equipment include, for each channel, a three-level pin driver, a dual comparator, and variable clamps (Figure 1). The driver features a -1.5V to +6.5V operating range and high-speed operation, including high-Z and active termination (3rd-level drive) modes, which is highly linear even at low-voltage swings. The comparator provides low timing dispersion regardless of changes in input slew rate and pulse width. The clamps provide damping of high-speed DUT_ waveforms when the device is configured as a high-impedance receiver.

Each of the four channels has high-speed, differential inputs compatible with ECL, LVPECL, LVDS, and GTL

signal levels, with optional 100Ω differential input terminations. Optional internal resistors at DATA_ and RCV_ provide differential termination of LVDS inputs. Optional internal resistors at CH_ and CL_ provide the pullup voltage and source termination for open-collector comparator outputs. These options significantly reduce the discrete component count on the circuit board.

The MAX9963/MAX9964 are available in two grade options. An A-grade version provides tighter matching of gain and offset of the drivers, and tighter offset matching of the comparators. This allows reference levels to be shared across multiple channels in cost-sensitive systems. A B-grade version provides lower cost for system designs that incorporate independent reference levels for each channel.

Quad, Low-Power, 500Mbps ATE Driver/Comparator

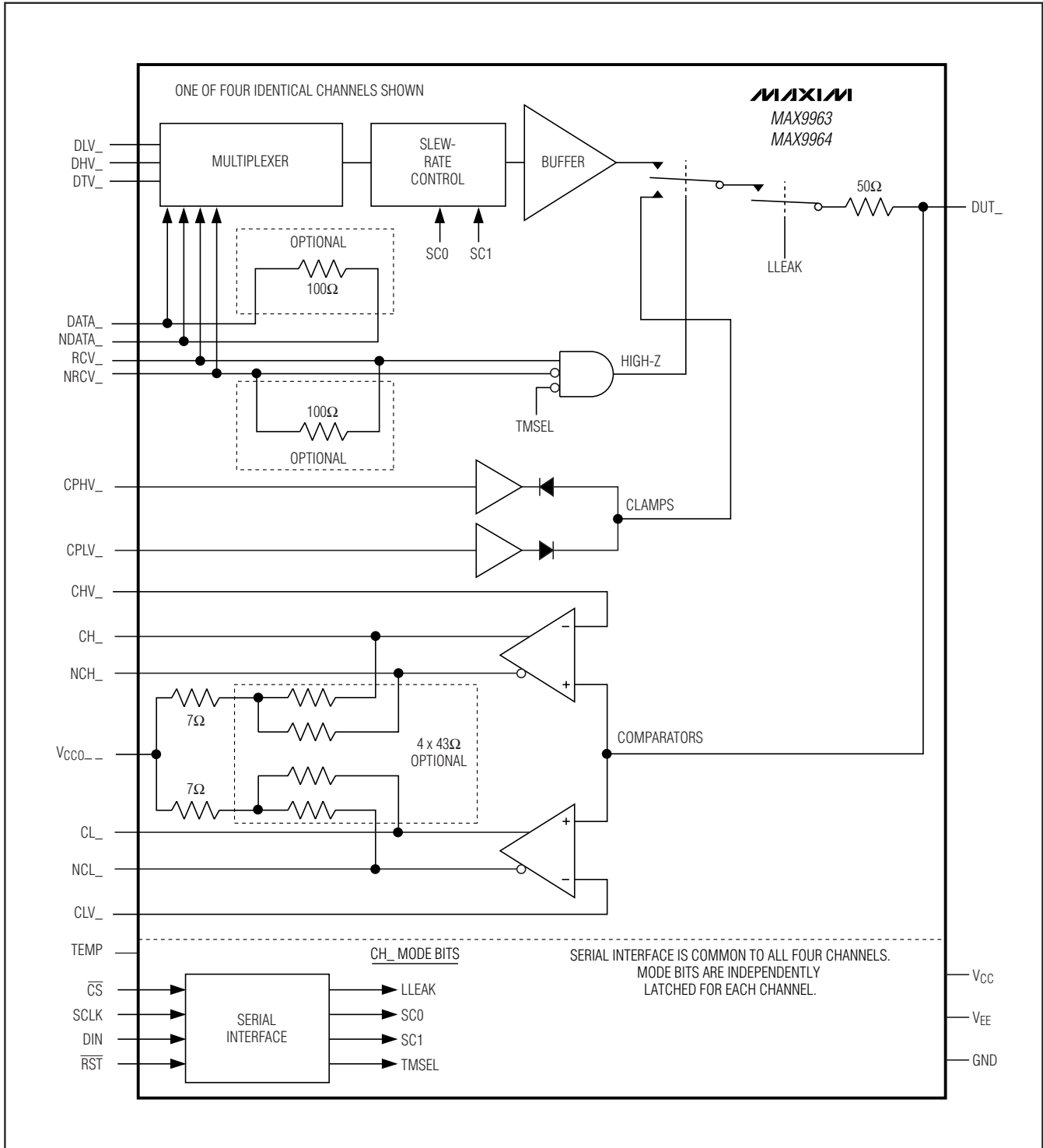


Figure 1. MAX9963/MAX9964 Block Diagram

Quad, Low-Power, 500Mbps ATE Driver/Comparator

MAX9963/MAX9964

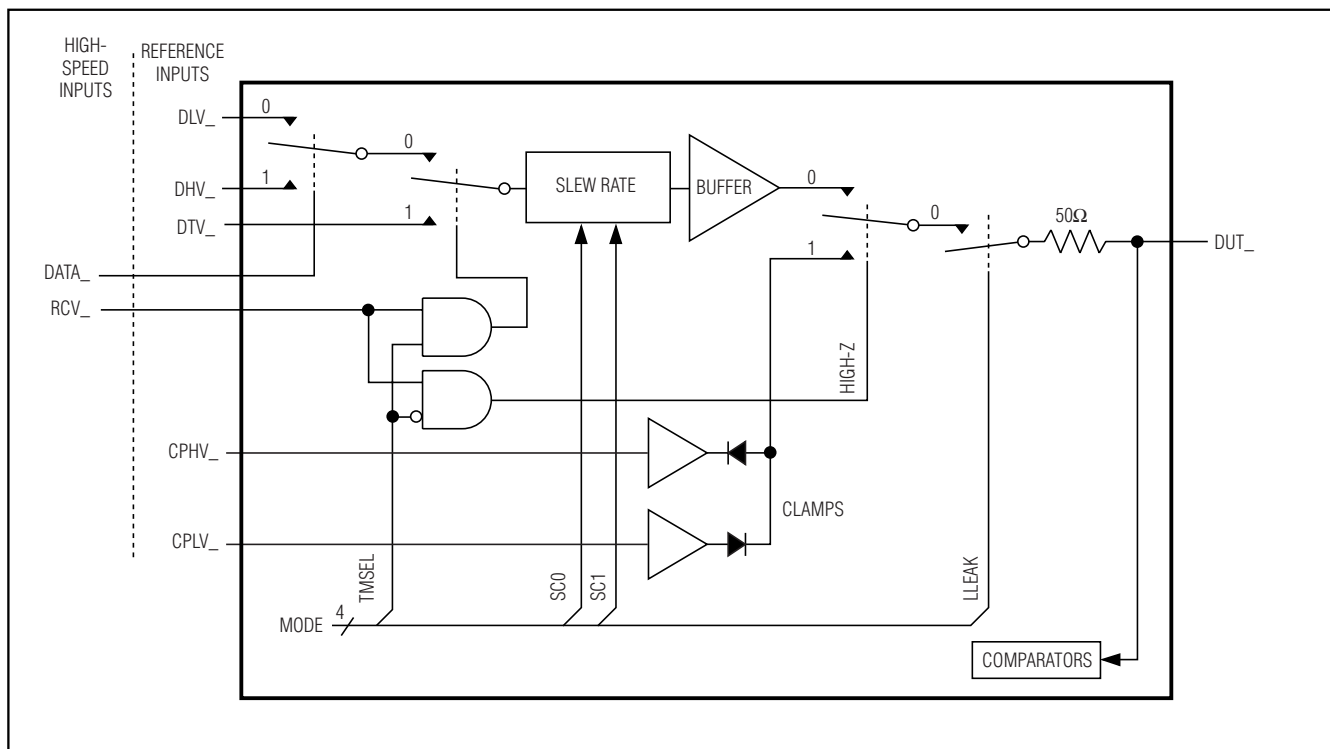


Figure 2. Simplified Driver Channel

Table 1. Slew Rate Logic

| SC1 | SC0 | DRIVER SLEW RATE (%) |
|-----|-----|----------------------|
| 0 | 0 | 100 |
| 0 | 1 | 75 |
| 1 | 0 | 50 |
| 1 | 1 | 25 |

Table 2. Driver Logic

| EXTERNAL CONNECTIONS | | INTERNAL CONTROL REGISTER | | DRIVER OUTPUT |
|----------------------|------|---------------------------|-------|------------------------------|
| DATA_ | RCV_ | TMSEL | LLEAK | |
| 1 | 0 | X | 0 | Drive to DHV_ |
| 0 | 0 | X | 0 | Drive to DLV_ |
| X | 1 | 1 | 0 | Drive to DTV_ (term mode) |
| X | 1 | 0 | 0 | High-impedance (high-z) mode |
| X | X | X | 1 | Low-leakage mode |

The MAX9963/MAX9964 modal operation is programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs, DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_, and mode control bit TMSEL. A slew rate circuit controls the slew rate of the buffer input. One of four possible slew rates can be selected (Table 1). The slew rate of the internal multiplexer sets the 100% driver slew rate (see the Driver Large-Signal Response graph in the *Typical Operating Characteristics*).

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed in low-leakage mode (Figure 2, Table 2). In high-impedance mode, the clamps are connected. This switching is controlled by high-speed input RCV_ and mode control bits TMSEL and LLEAK. In high-impedance mode, the bias current at DUT_ is less than 3μA, while the node maintains its ability to track high-speed signals. In

Quad, Low-Power, 500Mbps ATE Driver/Comparator

low-leakage mode, the bias current at DUT₋ is further reduced to less than 15nA, and signal tracking slows.

The nominal driver output resistance is 50Ω. Contact the factory for different resistance values within the 45Ω to 51Ω range.

Clamps

A pair of voltage clamps (high and low) can be configured to limit the voltage at DUT₋, and to suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using external connections CPHV₋ and CPLV₋. The clamps are enabled only when the driver is in the high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT₋ voltage range. The optimal clamp voltages are application specific and must be empirically determined. If clamping is not desired, set the clamp voltages at least 0.7V outside the expected

Table 3. Comparator Logic

| DUT ₋ > CHV ₋ | DUT ₋ > CLV ₋ | CH ₋ | CL ₋ |
|-------------------------------------|-------------------------------------|-----------------|-----------------|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

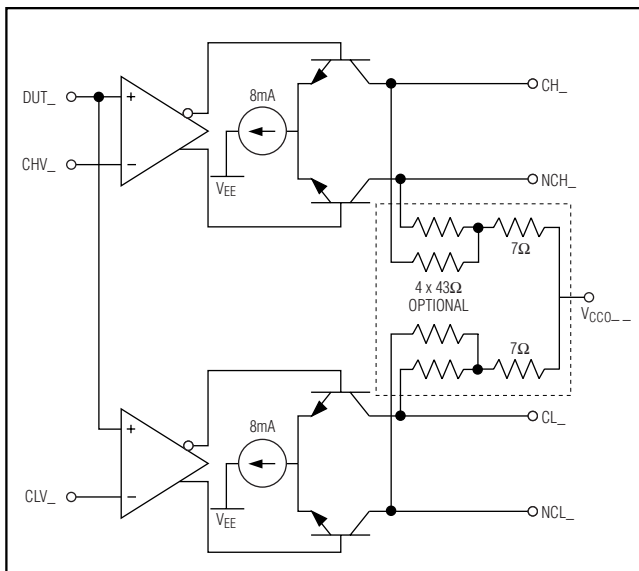


Figure 3. Open-Collector Comparator Outputs

DUT₋ voltage range; overvoltage protection remains active without loading DUT₋.

Comparators

The MAX9963/MAX9964 have two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT₋ and the other input connected to either CHV₋ or CLV₋ (Figure 1). Comparator outputs are a logical result of the input conditions, as indicated in Table 3.

Three configurations are available for the comparator differential outputs to ease interfacing with a wide variety of logic families. An open-collector configuration switches an 8mA current source between the two outputs. This configuration is available with and without internal termination resistors connected to VCCO₋ (Figure 3). For versions without internal termination resistors, leave VCCO₋ unconnected and add the required external resistors. These resistors are typically 50Ω to the pullup voltage at the receiving end of the output trace. Alternate configurations can be used, provided that the Absolute Maximum Ratings are not exceeded. For versions with internal terminations, connect VCCO₋ to the desired VOH voltage. Each output provides a nominal 400mV_{P-P} swing and 50Ω source termination.

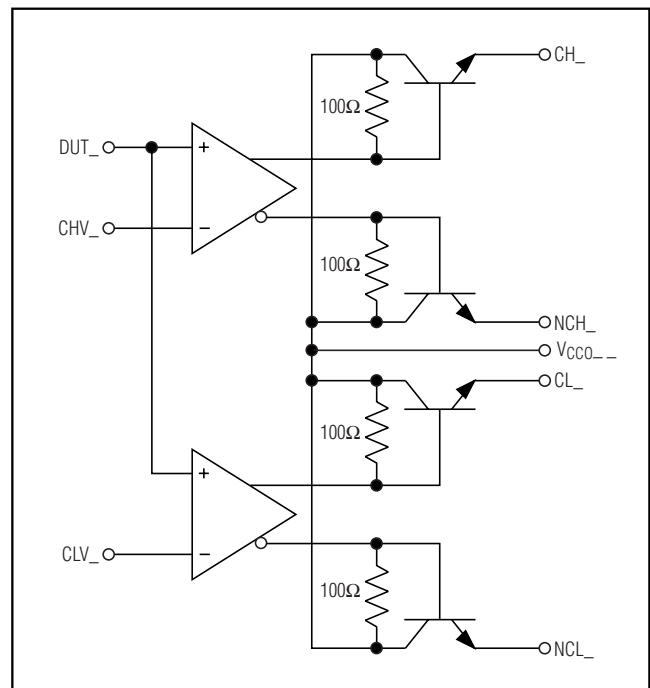


Figure 4. Open-Emitter Comparator Outputs

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MAX9963/MAX9964

Table 4. Shift Register Functions

| BIT | NAME | DESCRIPTION |
|-----|-------|---|
| D7 | 1E | Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to zero to make no changes to channel 1. |
| D6 | 2E | Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to zero to make no changes to channel 2. |
| D5 | 3E | Channel 3 Write Enable. Set to 1 to update the control byte for channel 3. Set to zero to make no changes to channel 3. |
| D4 | 4E | Channel 4 Write Enable. Set to 1 to update the control byte for channel 4. Set to zero to make no changes to channel 4. |
| D3 | LLEAK | Low-Leakage Select. Set to 1 to put driver and clamps into a low-leakage mode. Comparators remain active in low-leakage mode. Set to zero for normal operation. |
| D2 | SC1 | Driver Slew-Rate Select. SC1 and SC0 set the driver slew rate. See Table 1. |
| D1 | SC0 | |
| D0 | TMSEL | Driver Termination Select. Set to 1 to force the driver output to the DTV_ voltage (term mode) when RCV_ = 1. Set to zero to place the driver into a high-impedance state (high-Z mode) when RCV_ = 1. See Table 2. |

An open-emitter configuration is also available (Figure 4). Connect an external collector voltage to $V_{CCO_}$ and add external pulldown resistors. These resistors are typically 50Ω to $V_{CCO_} - 2V$ at the receiving end of the output trace. Alternate configurations can be used, provided that the Absolute Maximum Ratings are not exceeded.

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with \overline{RST} places the MAX9963/MAX9964 into a very-low-leakage state in which the DUT_ input current is less than 10nA over the 0 to 3V range. In this mode, the comparators still function at full speed but the driver and clamps are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is programmed independently for each channel.

If DUT_ is driven with a high-speed signal while LLEAK is asserted, leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal output voltage of 3.43V at a die temperature of +70°C (343K). The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 15kΩ (typ).

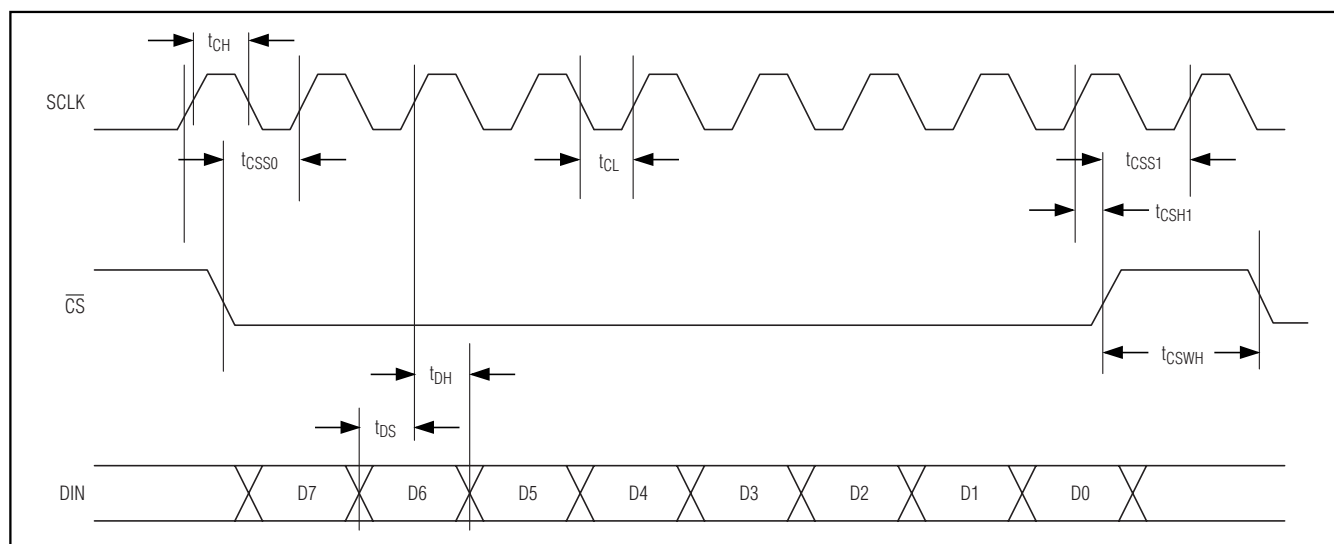


Figure 5. Serial Interface Timing

Quad, Low-Power, 500Mbps ATE Driver/Comparator

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9963/MAX9964 modes (Figure 6). Control data flow into an 8-bit shift register (MSB first) and are latched when \overline{CS} is taken high, as shown in Figure 5. Data from the shift register are then loaded into any or all of a group of four quad latches, determined by bits D4 through D7, as indicated in Figure 6 and Table 4. The quad latches contain the 4 mode bits for each channel of the quad pin driver. The mode bits, in conjunction with external inputs $DATA_{-}$ and RCV_{-} , manage the features of each channel, as shown in Tables 1 and 2. \overline{RST} sets $LLEAK=1$ for all channels, forcing them into low-leakage mode. All other bits are unaffected. At power-up, hold \overline{RST} low until V_{CC} and V_{EE} have stabilized.

Heat Removal

These devices require heat removal under normal circumstances through the exposed pad, either by soldering to circuit board copper (MAX9964) or by use of an external heat sink (MAX9963). The exposed pad is electrically at V_{EE} potential for both package types, and must be either connected to V_{EE} or isolated.

Chip Information

TRANSISTOR COUNT: 6499

PROCESS: Bipolar

Package Information

For the latest package outline information, go to www.maxim-ic.com/packages.

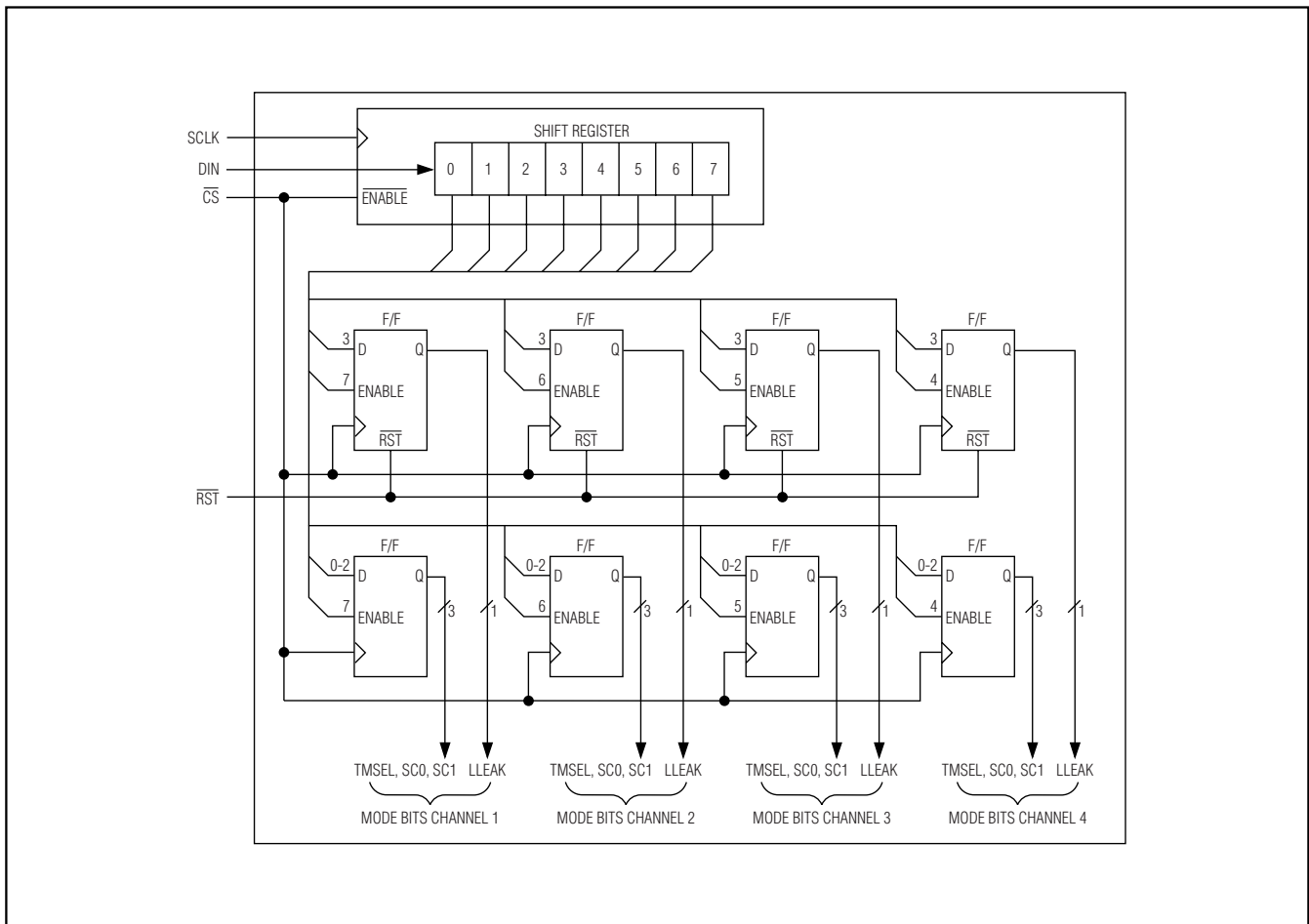


Figure 6. Serial Interface

Quad, Low-Power, 500Mbps ATE Driver/Comparator

Selector Guide

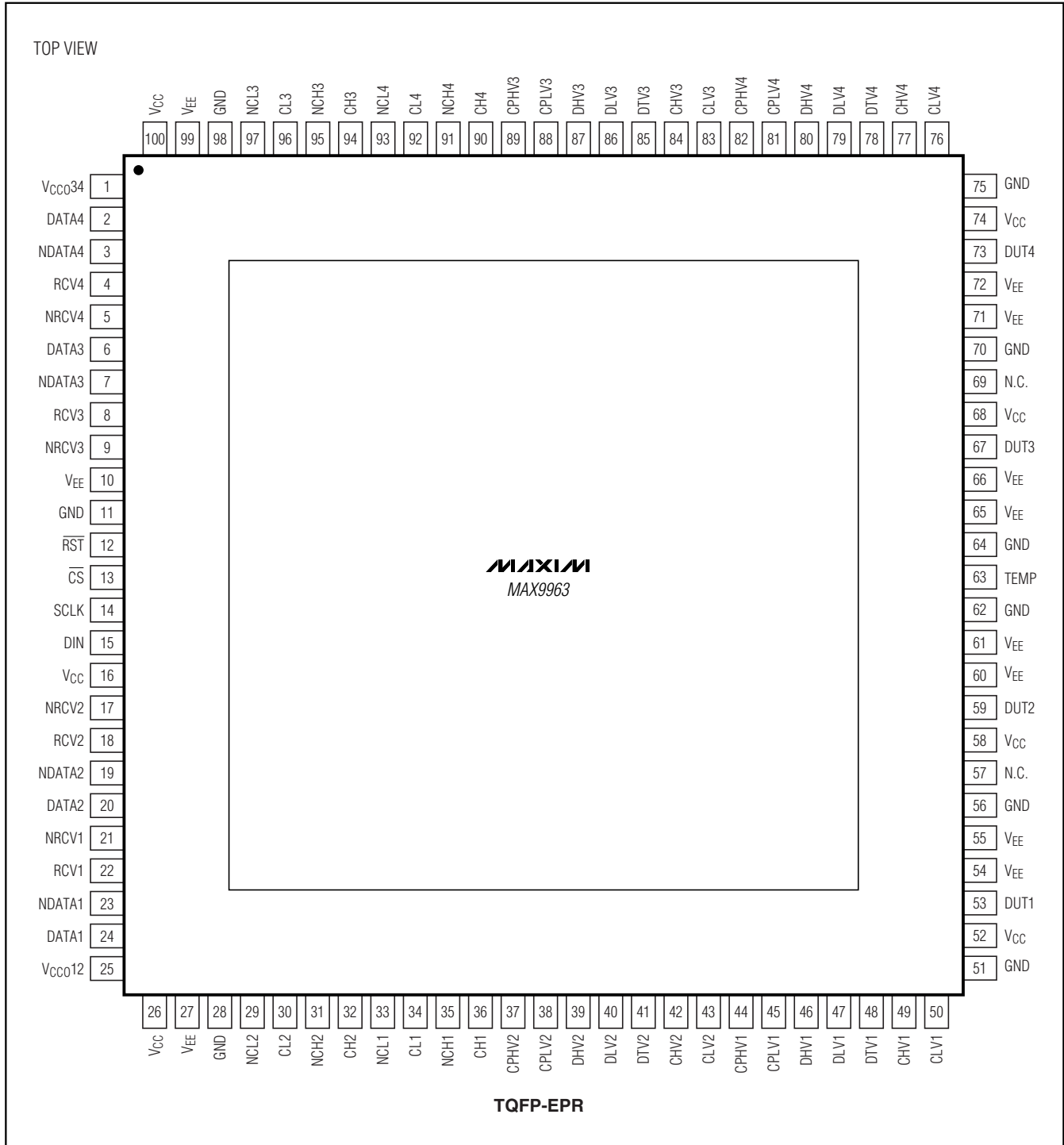
MAX9963/MAX9964

| PART | ACCURACY GRADE | COMPARATOR OUTPUT TYPE | COMPARATOR OUTPUT TERMINATION | HIGH-SPEED DIGITAL INPUT TERMINATION | HEAT EXTRACTION | PIN-PACKAGE |
|---------------|----------------|------------------------|-------------------------------|--------------------------------------|-----------------|--------------|
| MAX9963ADCCQ* | A | Open collector | None | None | Top | 100 TQFP-EPR |
| MAX9963AKCCQ* | A | Open collector | None | 100Ω LVDS | Top | 100 TQFP-EPR |
| MAX9963AGCCQ* | A | Open collector | 50Ω to V _{CCO__} | 100Ω LVDS | Top | 100 TQFP-EPR |
| MAX9963AHCCQ* | A | Open emitter | None | None | Top | 100 TQFP-EPR |
| MAX9963AJCCQ | A | Open emitter | None | 100Ω LVDS | Top | 100 TQFP-EPR |
| MAX9963BDCCQ* | B | Open collector | None | None | Top | 100 TQFP-EPR |
| MAX9963BKCCQ* | B | Open collector | None | 100Ω LVDS | Top | 100 TQFP-EPR |
| MAX9963BGCCQ | B | Open collector | 50Ω to V _{CCO__} | 100Ω LVDS | Top | 100 TQFP-EPR |
| MAX9963BHCCQ* | B | Open emitter | None | None | Top | 100 TQFP-EPR |
| MAX9963BJCCQ* | B | Open emitter | None | 100Ω LVDS | Top | 100 TQFP-EPR |
| MAX9964ADCCQ* | A | Open collector | None | None | Bottom | 100 TQFP-EP |
| MAX9964AKCCQ* | A | Open collector | None | 100Ω LVDS | Bottom | 100 TQFP-EP |
| MAX9964AGCCQ* | A | Open collector | 50Ω to V _{CCO__} | 100Ω LVDS | Bottom | 100 TQFP-EP |
| MAX9964AHCCQ* | A | Open emitter | None | None | Bottom | 100 TQFP-EP |
| MAX9964AJCCQ* | A | Open emitter | None | 100Ω LVDS | Bottom | 100 TQFP-EP |
| MAX9964BDCCQ* | B | Open collector | None | None | Bottom | 100 TQFP-EP |
| MAX9964BKCCQ* | B | Open collector | None | 100Ω LVDS | Bottom | 100 TQFP-EP |
| MAX9964BGCCQ | B | Open collector | 50Ω to V _{CCO__} | 100Ω LVDS | Bottom | 100 TQFP-EP |
| MAX9964BHCCQ* | B | Open emitter | None | None | Bottom | 100 TQFP-EP |
| MAX9964BJCCQ* | B | Open emitter | None | 100Ω LVDS | Bottom | 100 TQFP-EP |

*Future product—contact factory for availability.

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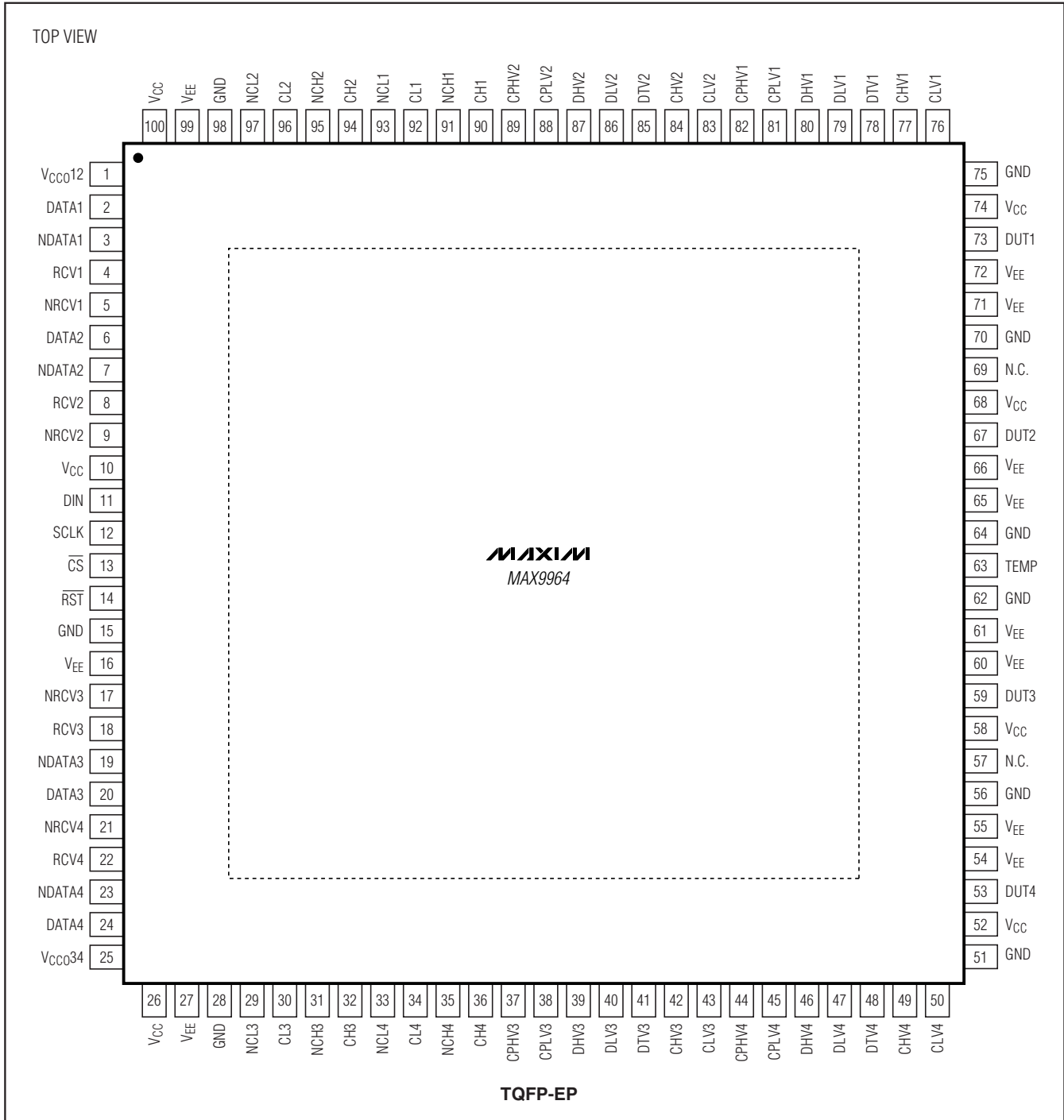
Pin Configurations



Quad, Low-Power, 500Mbps ATE Driver/Comparator

Pin Configurations (continued)

MAX9963/MAX9964



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