CY7C909
CY7C911

CYPRESS SEMICONDUCTOR

CMOS Micro Program Sequencers

Features

- **Fast**
  - **—CY7C909/11 has a 30-ns (min.) clock-to-output cycle time (commercial and military)**
- **Low power**
  - **—I_{CC} (max.) = 55 mA (commercial and military)**
- **V_{CC} margin**
  - **—5V ±10%**
  - **—All parameters guaranteed over commercial and military operating temperature range**
- **Infinitely expandable in 4-bit increments**
- **Capable of withstanding >2001V static discharge voltage**
- **Pin compatible and functionally equivalent to Am2909A/Am2911A**

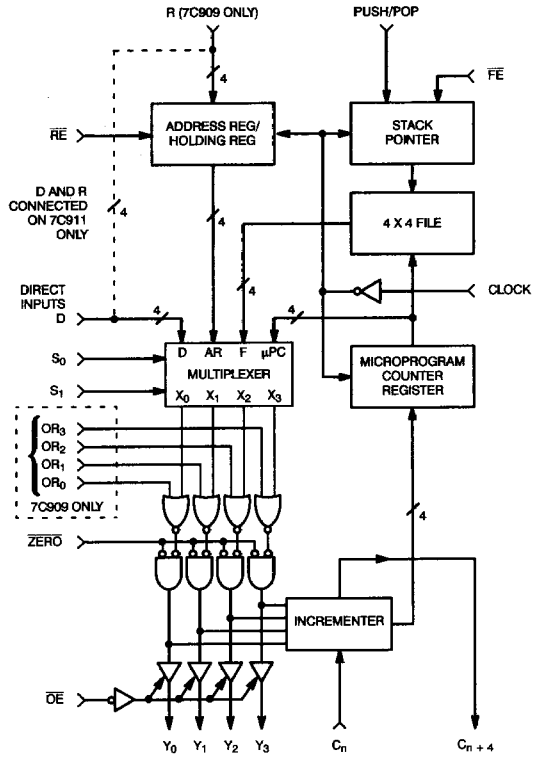
Functional Description

The CY7C909 and CY7C911 are high-speed, four-bit-wide address sequencers intended to control the sequence of execution of micro-instructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4-bit increments. Both devices are implemented in high-performance CMOS for optimum speed and power.

The CY7C909 can select an address from any of four sources. They are: (1) a set of four external direct inputs (D_i); (2) external data stored in an internal register (R_i); (3) a four-word-deep push/pop stack; or (4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. In the CY7C909, each of the four outputs (Y_i) can be ORed with an external input for conditional skip or branch instructions. A $\overline{ZERO}$ input line forces the outputs to all zeros. The outputs are three-state, controlled by the output enable ($\overline{OE}$) input.

The CY7C911 is an identical circuit to the CY7C909, except the four OR inputs are removed and the D and R inputs are tied together. The CY7C911 is available in a 20-pin, 300-mil package.

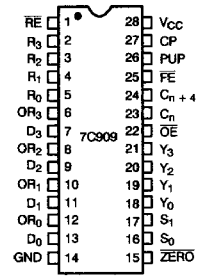
Logic Block Diagram



C909–1

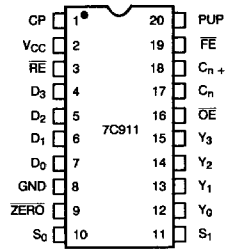
Pin Configurations

DIP
Top View



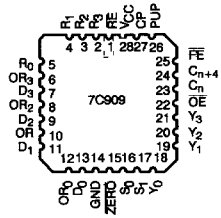
C909–2

DIP
Top View



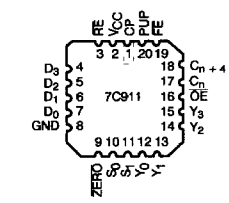
C909–3

PLCC/LCC
Top View



C909–4

PLCC/LCC
Top View



C909–5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current, into Outputs (LOW) ..... 30 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2.6 mA	Commercial	2.4		V
		V_{CC} = Min., I_{OH} = – 1.0 mA	Military	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			– 2.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		– 20	+20	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND or V_{CC}		– 30	– 85	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		55	mA
			Military		55	
I_{CC1}	V_{CC} Operating Supply Current	V_{CC} = Max. V_{IH} ≥ 3.0V, V_{IL} ≤ 0.4V	Commercial		35	mA
			Military		35	

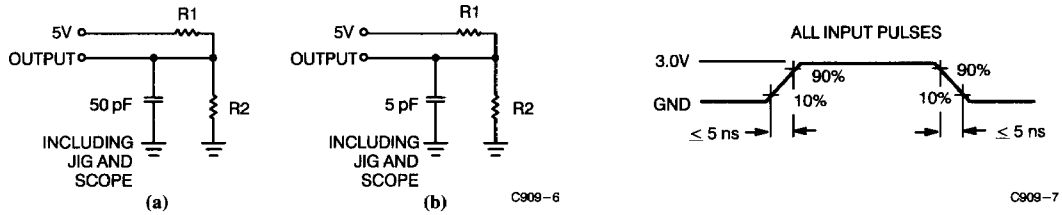
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



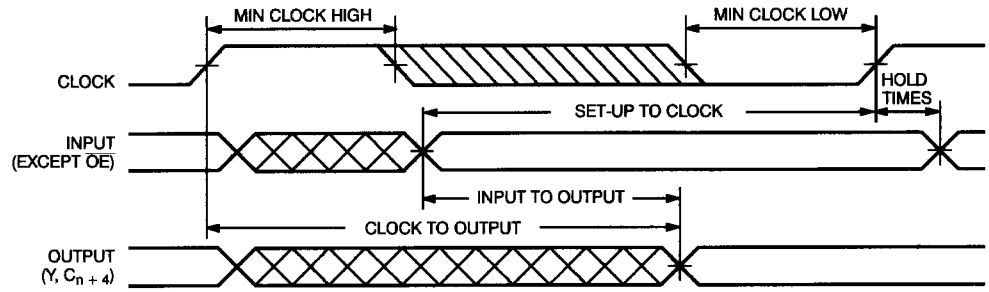
	Commercial	Military
R1	254Ω	258Ω
R2	187Ω	216Ω

Switching Characteristics Over the Operating Range[2, 5]

	CY7C909-30, CY7C911-30				CY7C909-40, CY7C911-40				Units
	Commercial		Military		Commercial		Military		
Minimum Clock LOW Time[6]	15		15		20		20		ns
Minimum Clock HIGH Time[6]	15		15		20		20		ns
MAXIMUM COMBINATORIAL PROPAGATION DELAYS									
From Input To:	Y	C_{n+4}	Y	C_{n+4}	Y	C_{n+4}	Y	C_{n+4}	ns
D_i	17	18	18	19	17	22	20	25	ns
S_0, S_1	18	18	20	20	29	34	29	34	ns
OR_i (CY7C909)	16	16	17	17	17	22	20	25	ns
C_n	—	13	—	15	—	14	—	16	ns
$\overline{ZERO}$	18	18	20	20	29	34	30	35	ns
$\overline{OE}$ LOW to Output	16	—	18	—	25	—	25	—	ns
$\overline{OE}$ HIGH to High Z[5]	16	—	18	—	25	—	25	—	ns
Clock HIGH, S_1, S_0 = LH	20	20	22	22	39	44	45	50	ns
Clock HIGH, S_1, S_0 = LL	20	20	22	22	39	44	45	50	ns
Clock HIGH, $S_1 S_0$, = HL	20	20	22	22	44	49	53	58	ns
MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW-to-HIGH Transition)									
From Input	**Set-Up**	**Hold**	**Set-Up**	**Hold**	**Set-Up**	**Hold**	**Set-Up**	**Hold**	
$\overline{RE}$	11	0	12	0	19	0	19	0	ns
R_i[7]	10	0	11	0	10	0	12	0	ns
Push/Pop	12	0	13	0	25	0	27	0	ns
FE	12	0	13	0	25	0	27	0	ns
C_n	10	0	11	0	18	0	18	0	ns
D_i	14	0	16	0	25	0	25	0	ns
OR_i (CY7C909)	12	0	14	0	25	0	25	0	ns
S_0, S_1	14	0	16	0	25	0	29	0	ns
$\overline{ZERO}$	12	0	13	0	25	0	29	0	ns

Notes:
5. Output loading as in part (b) of AC Test Loads and Waveforms.
6. System clock cycle time (Clock LOW Time and Clock HIGH Time) cannot be less than maximum propagation delay.
7. R_i and D_i are internally connected on the CY7C911. Use R_i set-up and hold times for D_i inputs.

Switching Waveforms



C909-8

Functional Description (continued)

The tables below define the control logic of the 7C909/911. *Table 1* contains the multiplexer control logic, which selects the address source to appear on the outputs.

Table 1. Address Source Selection

Octal	S_1	S_0	Source for Y Outputs
0	L	L	Microprogram Counter (μPC)
1	L	H	Address/Holding Register (AR)
2	H	L	Push-Pop Stack (STK)
3	H	H	Direct inputs (D_i)

Control of the Push/Pop Stack is contained in *Table 2*. File enable ($\overline{FE}$) enables stack operations, while Push/Pop (PUP) controls the stack.

Table 2. Synchronous Stack Control

$\overline{FE}$	PUP	Push-Pop Stack Change
H	X	No change
L	H	Push current PC into stack, increment stack pointer
L	L	Pop stack, decrement stack pointer

Table 3 illustrates the output control logic of the 7C909/911. The $\overline{ZERO}$ control forces the outputs to zero. The OR inputs are ORed with the output of the multiplexer.

Table 3. Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	High Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Table 4 defines the effect of S_0, S_1, $\overline{FE}$, and PUP control signals on the 7C909. It illustrates the address source on the outputs and the contents of the internal registers for every combination of these signals. The internal register contents are illustrated before and after the clock LOW-to-HIGH edge.

6 LOGIC

Table 4. Output Control

Cycle	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	Comment	Principle Use
N	0000	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End Loop
N + 1	—	J + 1	K	Rb	Rc	Rd	Ra	—		
N	0001	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-Up
N + 1	—	J + 1	K	J	Ra	Rb	Rc	—		Loop
N	001X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N + 1	—	J + 1	K	Ra	Rb	Rc	Rd	—		
N	0100	J	K	Ra	Rb	Rc	Rd	K	Use AR for Address;	End Loop
N + 1	—	K + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	
N	0101	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR;	JSR AR
N + 1	—	K + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	011X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N + 1	—	K + 1	K	Ra	Rb	Rc	Rd	—		
N	1000	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	RTS
N + 1	—	Ra + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	
N	1001	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	
N + 1	—	Ra + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	101X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref
N + 1	—	Ra + 1	K	Ra	Rb	Rc	Rd	—		(Loop)
N	1100	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D;	End Loop
N + 1	—	D + 1	K	Rb	Rc	Rd	Ra	—	Pop Stack	
N	1101	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D;	JSR D
N + 1	—	D + 1	K	J	Ra	Rb	Rc	—	Push μPC	
N	111X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N + 1	—	D + 1	K	Ra	Rb	Rc	Rd	—		

J = Contents of microprogram counter; K = Contents of address register; R_a, R_b, R_c, R_d = Contents in stack

Functional Description (continued)

Two examples of subroutine execution appear below. *Table 5* illustrates a single subroutine while *Tables 6* illustrates two nested subroutines. The starting address of the subroutine is applied to the D inputs of the 7C909 at the appropriate time, and the instruction to be performed is applied to the $S_{0,1}$, $\overline{FE}$, and PUP inputs. Typically, these signals are derived from a micro-instruction, register, and the output of the sequencer (Y_i) that is the address in the control ROM of the next micro-instruction to be executed.

Tables 5 shows the sequence of micro-instructions to be executed. At address J + 2, the sequence control portion of the micro-instruction contains the command "Jump to subroutine at A." At the time T_2, the 7C909 inputs are set up to execute the jump and save the return address. The subroutine address A is applied to the D inputs and appears on the Y outputs. On the next clock transition, the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. *Tables 6* has a similar timing chart showing one subroutine linking to a second, with the latter consisting of only one micro-instruction.

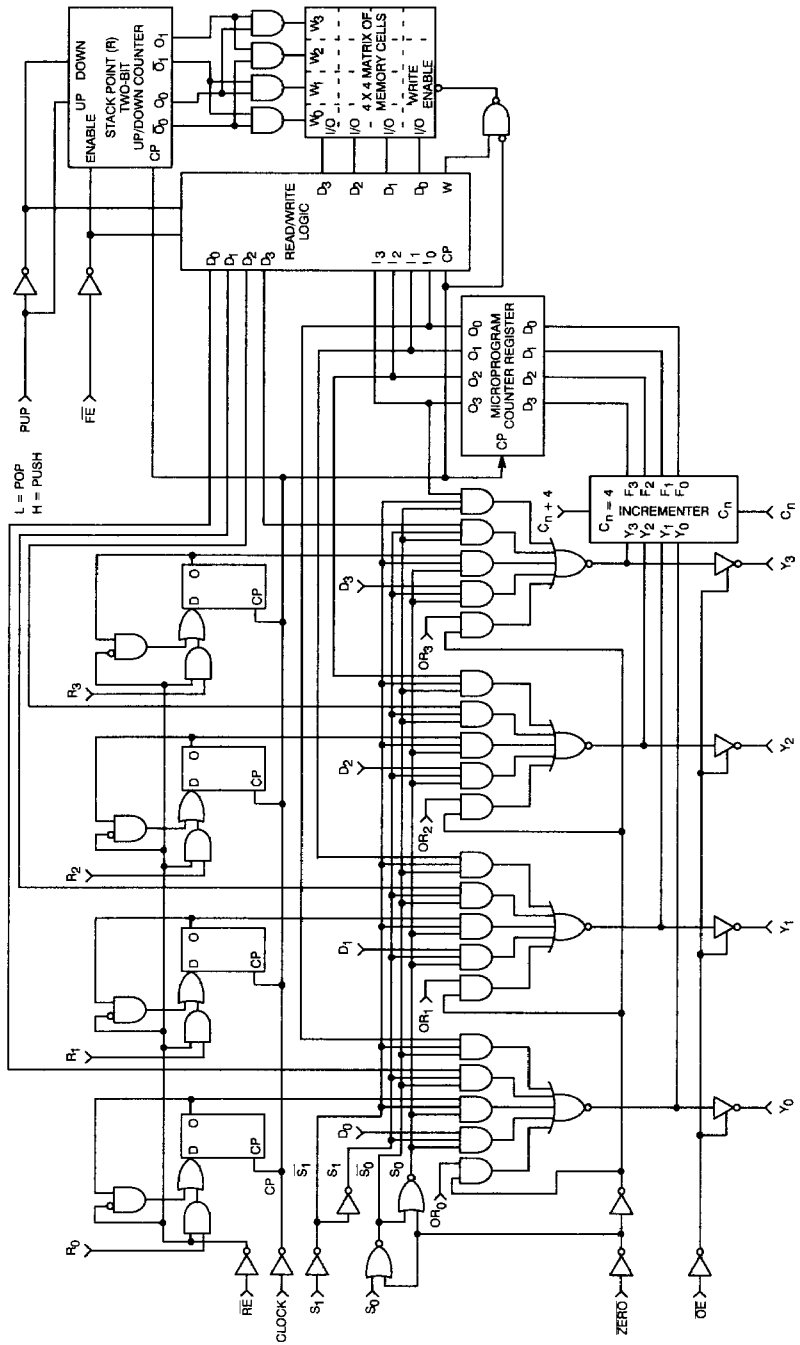
Table 5. Subroutine Execution[8]

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7
Signals	Clock	⎍	⎍	⎍	⎍	⎍	⎍	⎍	⎍
Inputs	S_1, S_0	0	0	3	0	0	2	0	0
	$\overline{FE}$	H	H	L	H	H	L	H	H
	PUP	X	X	H	X	X	L	X	X
	D	X	X	A	X	X	X	X	X
Internal Registers	µPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5
	STK0	–	–	–	J + 3	J + 3	J + 3	–	–
	STK1	–	–	–	–	–	–	–	–
	STK2	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–
Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5
Instruction being executed		Continue	Continue	JSR A	Continue	Continue	RTS	Continue	Continue

Table 6. Two Nested Subroutines, Routine B is Only One Instruction[8]

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Signals	Clock	⎍	⎍	⎍	⎍	⎍	⎍	⎍	⎍	⎍	⎍
Inputs (from µWR)	S_1, S_0	0	3	0	0	3	0	2	0	2	0
	$\overline{FE}$	H	L	H	H	L	H	L	H	L	H
	PUP	X	H	X	X	H	X	L	X	L	X
	D	X	A	X	X	B	X	X	X	X	X
Internal Registers	µPC	J + 2	J + 2	A + 1	A + 2	A + 3	B + 1	B + 1	A + 4	A + 5	J + 3
	STK0	–	–	J + 2	J + 2	J + 2	A + 3	A + 3	J + 2	J + 2	–
	STK1	–	–	–	–	–	J + 2	J + 2	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Output	Y	J + 1	A	A + 1	A + 2	B	B + 1	A + 3	A + 4	J + 3	J + 4
Instruction being executed		Continue	JSR A	Continue	Continue	JSR B	Continue	RTS	Continue	RTS	Continue

Note:
8. C_n = HIGH



Note:
R_i and D_i connected together and OR_i inputs removed on CY7C911.

Figure 1. Microprocessor Sequencer Block Diagram

Functional Description (continued)

Architecture

The CY7C909 and CY7C911 are CMOS microprogram sequencers for use in high-speed processor applications. They are cascadable in 4-bit increments. Two devices can address 256 words of microprogram, three can address up to 4K words, and so on. The architecture of the CY7C909/911 is illustrated in the logic diagram in *Figure 1*. The various blocks are described below.

Multiplexer

The multiplexer is controlled by the S_0 and S_1 inputs to select the address source. It selects either the direct inputs (D_i), the address register (AR), the microprogram counter (μPC), or the stack (SP) as the source of the next micro-instruction address.

Direct Inputs

The direct inputs (D_i) allow addresses from an external source to be output on the Y outputs. On the CY7C911, the direct inputs are also inputs to the address register.

Address Register

The address register (AR) consists of four D-type, edge-triggered, flip-flops that are controlled by the register enable ($\overline{RE}$) input. When register enable is LOW, new data is entered into the register on the LOW-to-HIGH clock transition.

Microprogram Counter

The microprogram counter (μPC) is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has a carry in (C_n) input and a carry out (C_{n+4}) output to facilitate cascading. The carry in input controls the microprogram counter. When carry in is HIGH the incrementer counts sequentially. The counter register is loaded with the current Y output plus one (Y + 1 ⇓ μPC) on the next clock cycle. When carry in is LOW the incrementer does not count. The microprogram counter register is loaded with the same Y output (Y ⇓ μPC) on the next clock cycle.

Stack

The Stack consists of a 4 x 4 memory array and a built-in stack pointer (SP), which always points to the last word written. The stack is used to store return addresses when executing microsubroutines.

The stack pointer is an up/down counter controlled by file enable ($\overline{FE}$) and Push/Pop (PUP) inputs. The file enable input allows stack operations only when it is LOW. The Push/Pop input controls the stack pointer position.

The PUSH operation is initiated at the beginning of a microsubroutine. Push/Pop is set HIGH while file enable is kept LOW. The stack pointer is incremented and the memory array is written with the micro-instruction address following the subroutine jump that initiated the push.

The POP operation is initiated at the end of a microsubroutine to obtain the return address. Both Push/Pop and file enable are set LOW. The return address is already available to the multiplexer. The stack pointer is decremented on the next LOW-to-HIGH clock transition, effectively removing old information from the top of the stack. The stack is configured so that data will roll-over if more than four POPs are performed, thus preventing data from being lost.

The contents of the memory position pointed to by the stack pointer is always available to the multiplexer. Stack reference operations can thus be performed without a push or a pop. Since the stack is four words deep, up to four microsubroutines can be nested.

The $\overline{ZERO}$ input resets the four Y outputs to a binary zero state. The OR inputs (7C909 only) are connected to the Y outputs such that any output can be set to a logical one.

The output enable ($\overline{OE}$) input controls the Y outputs. A HIGH on output enable sets the outputs into a high-impedance state.

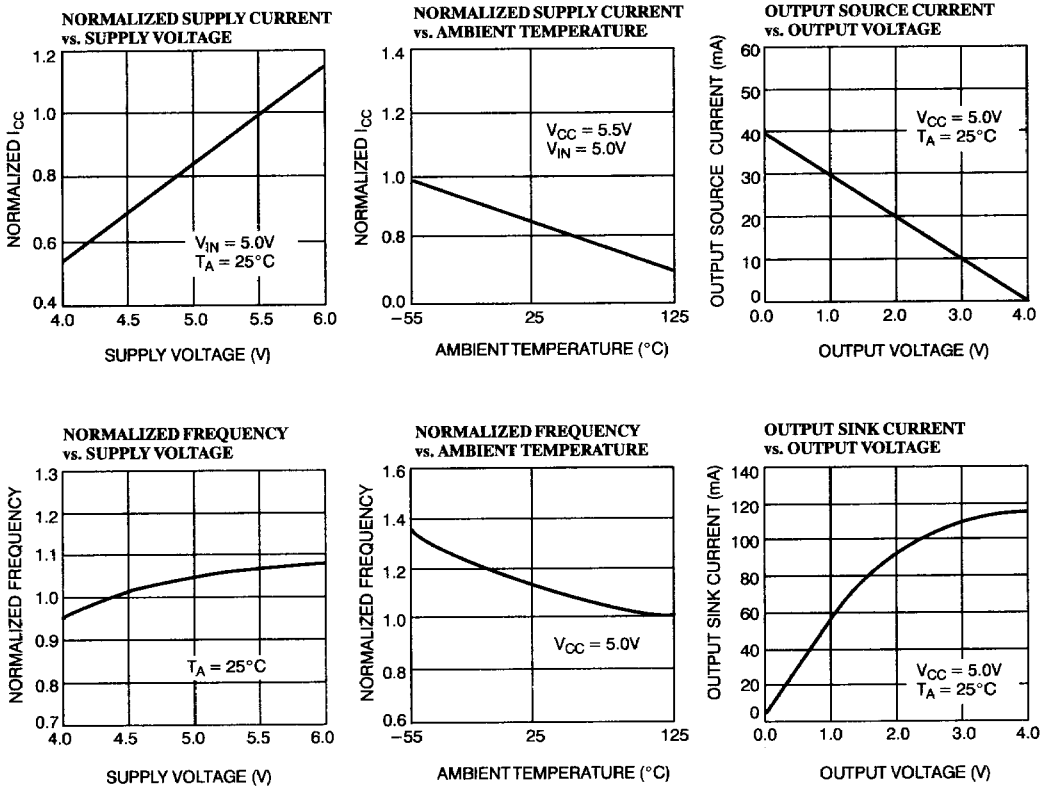
Definition of Terms

Name	Description
INPUTS	
S_1, S_0	Multiplexer Control Lines for Access Source Selection
$\overline{FE}$	File Enable, Enables Stack Operation, Active LOW
PUP	Push/Pop, Selects Stack Operation
$\overline{RE}$	Register Enable, Enables Address Register Active LOW
$\overline{ZERO}$	Forces Output to Logical Zero, Active LOW
$\overline{OE}$	Output Enable, Controls Three-State Outputs Active LOW
OR_i	Logic Or Input to each Address Output Line (7C909 only)
C_n	Carry In, Controls Microprogram Counter
R_i	Inputs to the Internal Address Register (7C909 only)
D_i	Direct Inputs to the Multiplexer
CP	Clock Input
OUTPUTS	
Y_i	Address Outputs
C_{n+4}	Carry Out from Incrementer

Definition of Terms (continued)

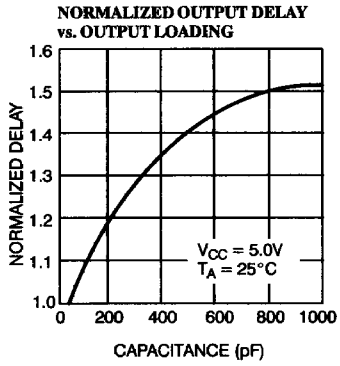
Name	Description
INTERNALSIGNALS	
µPC	Contents of the Microprogram Counter
AR	Contents of the Address Register
STK0 – STK3	Contents of the Push/Pop Stack
SP	Contents of the Stack Pointer
EXTERNALSIGNAL	
A	Address to the Counter Memory

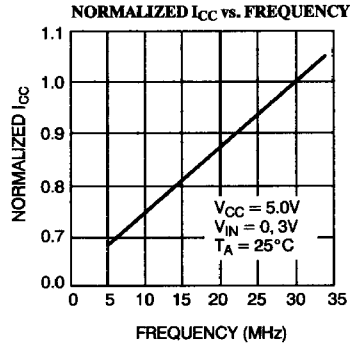
Typical DC and AC Characteristics



C909–10

Typical DC and AC Characteristics (continued)





C909-11

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
30	CY7C909-30DC	D16	Commercial
	CY7C909-30JC	J64	
	CY7C909-30PC	P15	
	CY7C909-30DMB	D16	Military
40	CY7C909-40DC	D16	Commercial
	CY7C909-40JC	J64	
	CY7C909-40LC	L64	
	CY7C909-40PC	P15	
	CY7C909-40DMB	D16	Military
	CY7C909-40LMB	L64	

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
30	CY7C911-30DC	D6	Commercial
	CY7C911-30JC	J61	
	CY7C911-30PC	P5	
	CY7C911-30DMB	D6	Military
40	CY7C911-40DC	D6	Commercial
	CY7C911-40JC	J61	
	CY7C911-40LC	L61	
	CY7C911-40PC	P5	
	CY7C911-40DMB	D6	Military
	CY7C911-40LMB	L61	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{CC1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
Minimum Clock LOW Time	7, 8, 9, 10, 11
Minimum Clock HIGH Time	7, 8, 9, 10, 11
MAXIMUM COMBINATORIAL PROPAGATION DELAYS	
D_i to Y	7, 8, 9, 10, 11
D_i to C_{n+4}	7, 8, 9, 10, 11
S_0, S_1 to Y	7, 8, 9, 10, 11
S_0, S_1 to C_{n+4}	7, 8, 9, 10, 11
OR_i (7C909) to Y	7, 8, 9, 10, 11
OR_i (7C909) to C_{n+4}	7, 8, 9, 10, 11
C_n to C_{n+4}	7, 8, 9, 10, 11
$\overline{ZERO}$ to C_{n+4}	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LH to Y	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LH to C_{n+4}	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LL to Y	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = LL to C_{n+4}	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = HL to Y	7, 8, 9, 10, 11
Clock HIGH, S_0, S_1 = HL to C_{n+4}	7, 8, 9, 10, 11

Parameters	Subgroups
MINIMUM SET-UP AND HOLD TIMES	
$\overline{RE}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{RE}$ Hold Time	7, 8, 9, 10, 11
Push/Pop Set-Up Time	7, 8, 9, 10, 11
Push/Pop Hold Time	7, 8, 9, 10, 11
FE Set-Up Time	7, 8, 9, 10, 11
FE Hold Time	7, 8, 9, 10, 11
C_n Set-Up Time	7, 8, 9, 10, 11
C_n Hold Time	7, 8, 9, 10, 11
D_i Set-Up Time	7, 8, 9, 10, 11
D_i Hold Time	7, 8, 9, 10, 11
OR_i (7C909) Set-Up Time	7, 8, 9, 10, 11
OR_i (7C909) Hold Time	7, 8, 9, 10, 11
S_0, S_1 Set-Up Time	7, 8, 9, 10, 11
S_0, S_1 Hold Time	7, 8, 9, 10, 11
$\overline{ZERO}$ Set-Up Time	7, 8, 9, 10, 11
$\overline{ZERO}$ Hold Time	7, 8, 9, 10, 11

Document #: 38–00015–B