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MOTOROLA

MC145572

ISDN U-Interface Transceiver

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1 INTRODUCTION

1.1 INTRODUCTION

The MC145572 U–interface transceiver is a single chip device for the Integrated Services Digital Network Basic Access Interface that conforms to the American National Standard ANSI T1.601–1992. The device, which can be configured for LT (Line Termination) or NT (Network Termination) applications, performs all necessary Layer 1 functions while utilizing 2B1Q line coding.

The MC145572 is a redesign of the MC145472 and MC14LC5472 U–interface transceivers. The internal signal processing algorithms are the same as for the original MC145472 to maintain its industry–leading performance. The control and time division multiplex interfaces have been significantly enhanced to serve the needs of the growing ISDN (Integrated Services Digital Network) marketplace. The use of the latest process technologies permits the MC145572 to be made available in 44–lead PLCC and TQFP packages.

The MC145572 is designed to be easily retrofit into existing MC145472/MC14LC5472 designs with minimal software and hardware changes. New designs can take advantage of enhanced digital interface features of the MC145572, such as the timeslot assigner and the availability of superframe alignment signals. Software that implements analog loopbacks or Superframer–to–Deframer loopbacks may have to be changed. See **Section 5.6**.

The MC145572 can operate in many different modes. The control of these various modes is provided via special purpose pins and the Serial Control Port (SCP) or the Parallel Control Port (PCP). The SCP conforms to the Motorola Serial Control Peripheral Interface standard, an industry standard serial microprocessor interface. The PCP is a standard microprocessor bus port. The designer may choose between using the General Circuit Interface (GCI) or the Motorola Interchip Digital Link (IDL)–type time division 2B+D data interface. A timeslot assigner is also provided on the MC145572.

The customer data crossing the U–reference point consists of two 64 kbps B channels and one 16 kbps D channel in each direction. Maintenance and framing overhead is also included for a total 160 kbps data (80 Kbaud signalling) rate.

The specifications for the pullable crystal have been relaxed.

1.2 SUPPLEMENTAL DOCUMENTATION

In addition to descriptions of the ISDN network and basic MC145572 device functionality, this document also contains several appendices:

Appendix A, *MC145572EVK ISDN U–Interface Transceiver Evaluation Kit*, provides a brief overview of the extremely versatile MC145572EVK, which is available to assist with design–in of the MC145572. All developers of MC145572–based products are strongly encouraged to make use of this inexpensive, but valuable tool.

Appendix B, *Component Sourcing*, lists specifications and potential sources for key external components such as line interface transformers.

Appendix C, *Printed Circuit Board Layout*, provides recommendations for the printed circuit board (PCB) layout.

Appendix D, *Eye Pattern Generator*, details design information to construct an eye pattern generator.

Appendix E, *Line Interface Circuit Component Value Calculations*, provides a design example on how to calculate component values for the line interface circuit.

Appendix F, *Applications*, provides an example of how to configure two MC145572 U–interface transceivers as a repeater and how to connect MC14LC5540 ADPCM or MC14LC5480 PCM codecs for pair gain applications.

Appendix G, *Performance*, shows graphs of typical line interface circuit performance.

Appendix H, *Test and Debug,* gives test and debug information on high impedance digital output mode, control of transmit signals, and characterization of the pullable crystal.

Appendix I, *Glossary of Terms and Abbreviations,* contains terms found in this and other Motorola publications concerned with Motorola Semiconductor Products for Communications.

Appendix J, *Standards Bodies,* gives a listing of major standards bodies, with contact information.

Every effort has been made to make this a complete and easy to use document; however, contact your local sales office or the factory applications staff if you require any further assistance.

Information regarding the generic 2B1Q U–interface requirement is readily available in standards documents such as ANSI T1.601–1992; and therefore, has not been included in this document. The U–interface equipment designer will find the ANSI document to be a useful reference.

1.3 FEATURES

Key features of the MC145572 U–interface transceiver include:

- Single Chip 2B1Q Echo Cancelling Adaptively Equalized Transceiver
- Conforms to ANSI T1.601–1992, *Integrated Services Digital Network (ISDN)–Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification),* American National Standards Institute
- Compliant to ETSI ETR 080
- Warm Start Capability
- NT Synchronizes To and Operates With 80 kHz ± 32 ppm Received Signal from LT
- Supports Master, Slave, and Slave–Slave Timing Modes
- On–Chip FIFOs for Transmit and Receive Directions
- 2B+D Customer Data Provided by the Industry Standard IDL
- GCI
- Timeslot Assigner
- Control, Status, and Extended Maintenance Functions Provided through the SCP
- Microprocessor Bus Compatible Parallel Port Available as Pin Selectable Option
- On–Chip Conformance with Activation and Deactivation as Specified in ANSI T1.601
- Automatic Handling of Basic Maintenance Functions
- Automatic Internal Compliance with the Embedded Operations Channel (eoc) Protocol as Specified in the American National Standard
- Complete Set of Loopbacks for Both the IDL– and U–Reference Point Directions
- Pin Selectable for LT or NT Applications
- On–Chip 2.5 V Transmit Driver Meeting 1992 Requirement
- 8 kHz Reference Frequency in LT Mode
- High Performance CMOS Process Technology
- 5 V Power Supply

1.4 REVISIONS

This revision (Rev. 3) of the MC145572/D data book uses change bars to indicate significant changes or additions to the book with respect to Rev. 2. All references below pertain to MC145572/D, Rev. 3.

The following is a list of sections, figures, and tables with changes.

Sections:

1.1

1.4

Sections, continued:

3.3.2	MCU/$\overline{\text{GCI}}$:
3.3.2	PAR/$\overline{\text{SER}}$:
3.3.4	TxBCLK:
3.3.4	RxBCLK:
3.3.4	SFAR:
3.3.4	SFAX:
3.3.4	S0:
3.3.6	FREQREF: LT Mode
3.3.6	FREQREF: NT Mode
4.5.6	OR5
5.6.3	Pseudo Code modified
5.6.4	Added new section on Superframe Framer–to–Deframer loopbacks in systems having multiple MC145572s
5.6.5	Was old Section 5.6.4. Modified code. Deleted old Section 5.6.5.
5.6.6	Added new section on external analog loopbacks in systems having multiple MC145572s
5.7	2B1Q Line Interface; moved to Appendix E
5.8	Crystal Oscillator; moved to Section 3.3.7
8.1	
8.3.2.3	
10.4	
10.5	
B.3	
B.3.1	
B.3.2	Deleted section

Figures:

3–1	Added FREQREF reference
4–5	Deleted figure; same as Figure 5–23
5–21	
5–22	
F–4	Added resistor line
F–5	Added FSX reference
F–6	Remote Access Multi–Line Configuration No. 2
F–7	Multi–Line U Line Card

Tables:

3–6	Changed values in PAR/$\overline{\text{SER}}$ column
8–3	Added NOP row
B–3	Deleted Part No. and Mode columns

NOTE

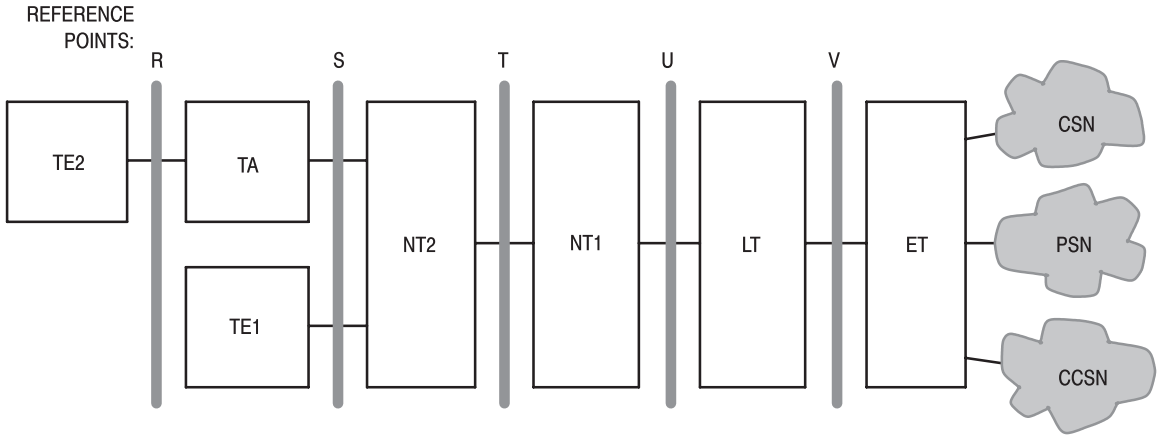
This revision (Rev. 3) was edited for consistency of information. No technical information was changed that was not marked with change bars.

2 ISDN BASIC ACCESS SYSTEM OVERVIEW

2.1 ISDN REFERENCE MODEL

The ISDN reference model is shown in Figure 2–1. This is a general model that can be adapted to many different implementations of the ISDN. The diagram indicates the position of the U–reference point between the LT and the Network Termination 1 (NT1) blocks in the model.

The U–interface is the physical access point to the ISDN at the U–reference point. This interface is a single twisted wire pair supporting full–duplex transmission of digital information at a rate of 160 kbps. The twisted wire pair can extend up to 18,000 feet and may include bridge taps. This interface is often referred to as a Digital Subscriber Line.



Key:

CCSN:	Common Channel Signalling Network	NT2:	Network Termination 2 (OSI Layers 2 and 3)
CSN:	Circuit Switched Network	PSN:	Packet Switched Network
ET:	Exchange Termination (C.O. Switch)	TA:	Terminal Adapter
LT:	Line Termination (Line Card)	TE1:	Terminal Equipment 1 (ISDN Terminal)
NT1:	Network Termination 1 (OSI Layer 1 Only)	TE2:	Terminal Equipment 2 (Non–ISDN Terminal)

Figure 2–1. ISDN Reference Model

2.2 U-INTERFACE TRANSCEIVER ISDN APPLICATIONS

Figure 2–2 shows some typical ISDN applications of the MC145572 U–interface transceiver as well as related ISDN applications for S/T–interface terminal equipment using Motorola semiconductor solutions.

The LT example shows the U–interface transceiver in a line card environment. This line card can be located in an ISDN central office switch or other ISDN compatible switching equipment, including a remote switch or carrier terminal. In this application, the IDL and SCP of the MC145572 are interfaced to the backplane of the switching equipment as required for the particular switch architecture.

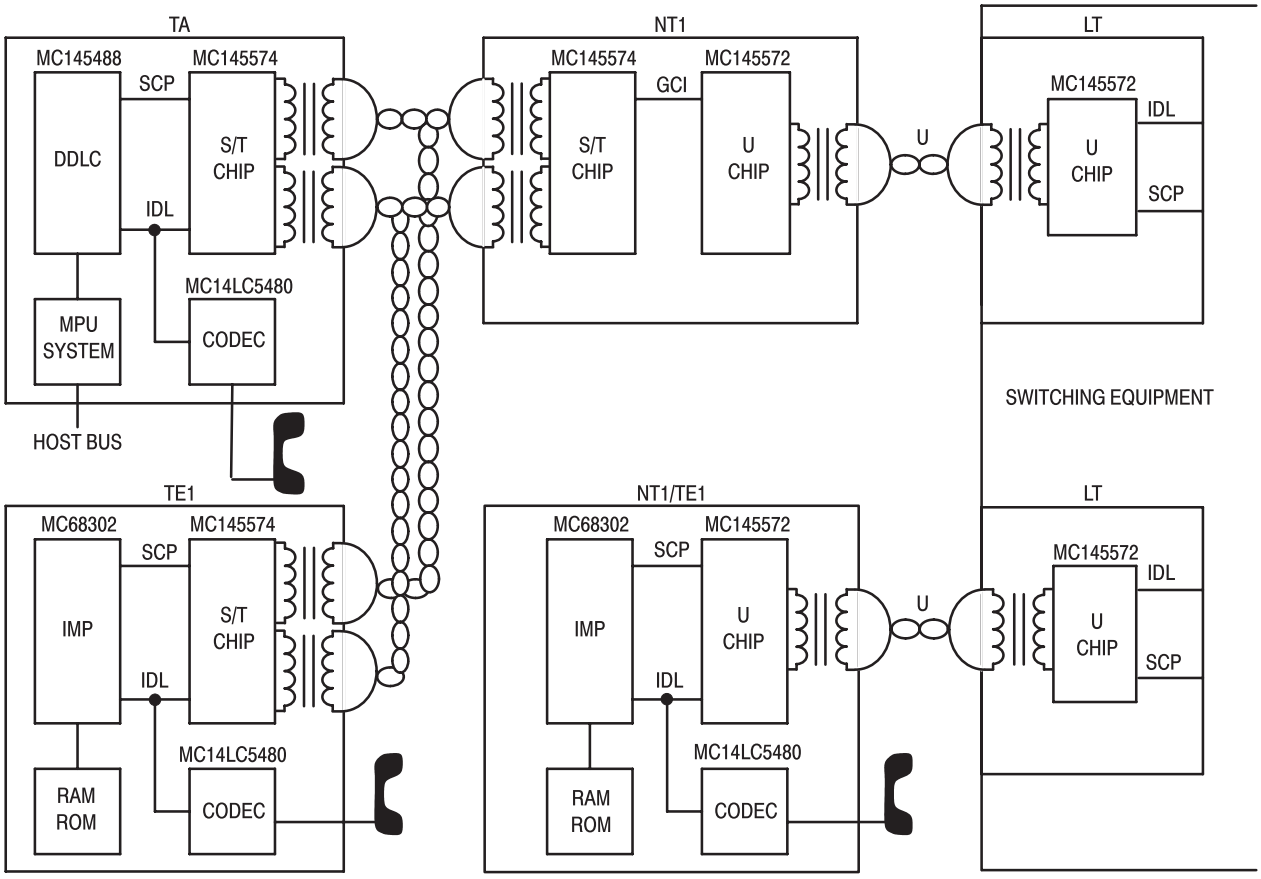


Figure 2–2. MC145572 Typical ISDN Applications

The NT1 converts the 2–wire U–interface to the 4–wire S/T–interface as shown. By combining an MC145572 with a Motorola MC145574 S/T–interface transceiver, an NT1 can be readily implemented.

Also shown is a highly integrated U–interface ISDN terminal, designated NT1/TE1, which implements a complete voice and data terminal with a U–interface for immediate and cost effective access to the ISDN. The MC145572 is shown interfaced to the M68000 core–based MC68302 Integrated Multi-protocol Processor (IMP), which handles layers 2 – 7 of the OSI reference model. Voice is supported with a conventional codec–filter device, such as the MC14LC5480.

The network is completed with a TA and an S/T–interface ISDN terminal (TE1). Two different architectures are shown: the TA is implemented with the MC145488 Dual Data Link controller and a host MCU system, and the TE1 is shown implemented with the MC68302 IMP.

2.3 NON-ISDN U-INTERFACE TRANSCEIVER APPLICATIONS

Typical non–ISDN pair gain application block diagrams are shown in Figures 2–3 and 2–4. Pair gain is a technique to multiplex two or more analog phone lines over a single twisted pair.

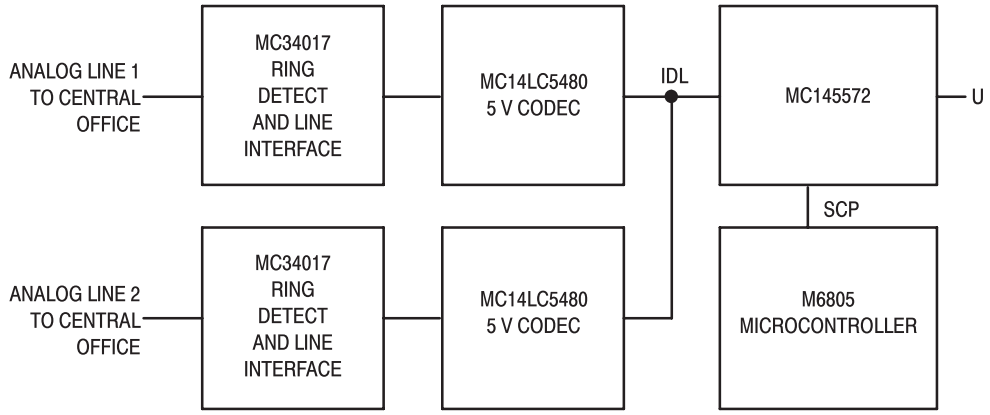


Figure 2–3. Pair Gain Application, Central Office Terminal

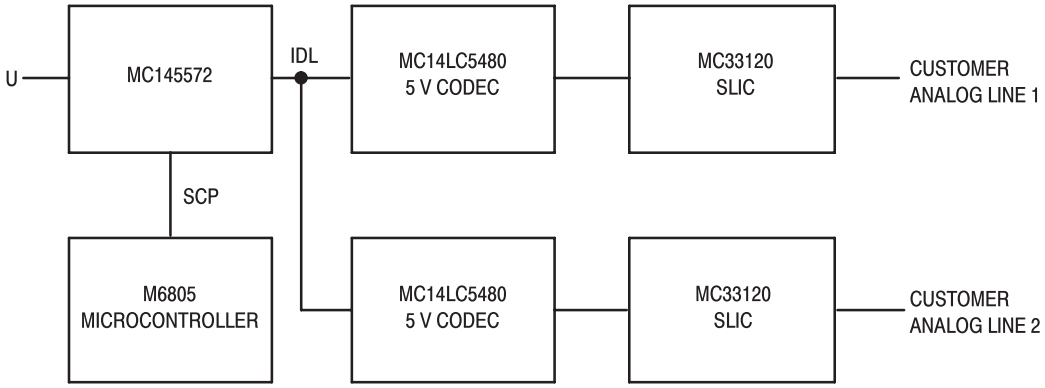


Figure 2–4. Pair Gain Application, Remote Terminal

3
PIN DESCRIPTIONS

3.1 INTRODUCTION

This chapter describes the MC145572 pins and their operation. Additionally, quick reference tables are provided. These tables are organized by the three major modes of operation and by package type.

3.2 PIN DESCRIPTION QUICK REFERENCE

The following tables (Tables 3–1 through 3–5) list the MC145572 pins in functional groups and provide brief pin descriptions. For more detailed information, refer to the section indicated in the table title.

Table 3–1. Power Supply and Mode Selection Pins (See Sections 3.3.1 and 3.3.2)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Power Supply Pins			
V_{DD}	27	44	Positive power supply, nominally + 5 V.
V_{SS}	29, 5	2, 22	Negative power supply, nominally ground.
$V_{DD}Rx$, $V_{DD}Tx$	30, 38	3, 11	Positive power supply for analog circuits, nominally + 5 V.
$V_{SS}Rx$, $V_{SS}Tx$	31, 37	4, 10	Negative power supply for analog circuits, nominally ground.
$V_{DD}I/O$	7, 20	24, 37	Positive power supply for input and output circuits, nominally + 5 V.
$V_{SS}I/O$	6, 19	23, 36	Negative power supply for input and output circuits, nominally ground.
CAP3V	28	1	Connection for internal 3 V regulator decoupling capacitor.
Mode Selection Pins			
$\overline{RESET}$	41	14	Hardware reset when at a logic low, normal operation when at a logic high. This pin has a Schmitt trigger input.
NT/$\overline{LT}$	42	15	Hardware selection of LT (logic low) and NT (logic high) operating mode.
MCU/$\overline{GCI}$	26	43	MCU mode versus GCI mode select input.
PAR/$\overline{SER}$	40	13	Parallel versus serial control port selection. PAR/$\overline{SER}$ = 1 (logic high) for a parallel port. PAR/$\overline{SER}$ = 0 (logic low) for serial control port interfacing.

Table 3–2. Time Division Multiplex Interface Pins (See Section 3.3.3)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Time Division Multiplex Data Interface			
M/$\overline{S}$	43	16	Master/Slave mode select input for the IDL2 or GCI interface. Master mode for M/$\overline{S}$ = 1 (logic high).
FSR/FSC	10	27	The MCU 8 kHz frame sync for data transmitted on the D_{out} pin. In GCI operation, this pin serves as the FSC pin.
FSX	11	28	The MCU 8 kHz frame sync for data input to the D_{in} pin. This pin is not used in GCI mode.
DCL	14	31	MCU bit clock, or GCI 2x bit clock.
D_{out}	13	30	Serial data out of MCU or GCI interface.
D_{in}	12	29	Serial data into MCU or GCI interface.

Table 3–3. Digital Data Interface Pins (See Section 3.3.4)

Pin Name			Pin No.		Pin Description
MCU/ SCP Mode	MCU/PCP Mode	GCI Mode	TQFP	PLCC	
$\overline{\text{SCPEN}}$	$\overline{\text{CS}}$	IN1	4	21	In serial port, MCU mode, $\overline{\text{SCPEN}}$ is the active low SCP enable input. In parallel port, MCU mode, $\overline{\text{CS}}$ is the active low chip select. In full GCI mode, defined when MCU/$\overline{\text{GCI}}$ = 0, this input is IN1.
SCPCLK	R/$\overline{\text{W}}$	IN2	3	20	In serial port, MCU mode, SCPCLK is the serial control port clock input. In parallel port, MCU mode, R/$\overline{\text{W}}$ is the read versus write indication to the parallel port. In full GCI mode, defined when MCU/$\overline{\text{GCI}}$ = 0, this input is IN2.
SCPRx	D0	OUT1	1	18	In serial port, MCU mode, SCPRx is the serial control port data input. In parallel port, MCU mode, D0 is the LSB of the parallel data bus. In full GCI mode, defined by MCU/$\overline{\text{GCI}}$ = 0, OUT1 is an output reflecting the state of bit 5 as set in BR7.
SCPTx	D1	OUT2	2	19	In serial port, MCU mode, SCPTx is the serial control port data output. In parallel port, MCU mode, this is signal D1 of the parallel data bus. In full GCI mode, defined by MCU/$\overline{\text{GCI}}$ = 0, OUT2 is an output reflecting the state of bit 6 as set in BR7
$\overline{\text{IRQ}}$	$\overline{\text{IRQ}}$	—	44	17	Open–drain active low output for microcontroller interrupt.
4.096 CLKOUT	D2	4.096 CLKOUT	17	34	4.096 MHz clock out. In parallel port, MCU mode, this is signal D2 of the parallel data bus.
15.36 CLKOUT	D3	15.36 CLKOUT	18	35	15.36 MHz clock out. Not synchronized to recovered clock in the NT mode. In parallel port, MCU mode, this is signal D3 of the parallel data bus.
BUFXTAL	D4	BUFXTAL	21	38	This is a square wave output from the 20.48 MHz oscillator and it is not synchronized to the recovered clock in the NT mode. In parallel port, MCU mode, this is signal D4 of the parallel data bus.
EYEDATA DCHCLK	D5	S2	22	39	In serial port, MCU mode, this pin may carry either EYEDATA or DCHCLK. In parallel port, MCU mode, this is signal D5 of the parallel data bus. In full GCI mode, this pin is the S2 input.
TxBCLK DCH_{in}	D6	$FREF_{out}$	23	40	In serial port, MCU mode, this pin may carry either TxBCLK or DCH_{in}. TxBCLK is an 80 kHz clock output, aligned and synchronized to the transmitted baud. DCH_{in} is the D channel port serial data input. In parallel port, MCU mode, this is signal D6 of the parallel data bus. In full GCI mode, operating as a GCI slave, this pin provides 2.048 MHz or 512 kHz synchronized clock output.
RxBCLK DCH_{out}	D7	CLKSEL	24	41	In serial port, MCU mode, this pin may carry either RxBCLK or DCH_{out}. RxBCLK is an 80 kHz clock output, aligned and synchronized to the received baud. DCH_{out} is the D channel port serial data output. In parallel port, MCU mode, D7 is the MSB of the parallel data bus. In full GCI mode, operating as a GCI master, CLKSEL selects between 512 kHz and 2.048 MHz for DCL. CLKSEL = 1 selects 2.048 MHz.
SYSCLK 20.48 MHz SFAR $\overline{\text{TSEN}}$	SYSCLK 20.48 MHz SFAR $\overline{\text{TSEN}}$	S1	8	25	In either MCU mode, this pin may carry either SYSCLK, 20.48 MHz, SFAR, or $\overline{\text{TSEN}}$ outputs. SYSCLK is a 10.24 MHz clock for sampling EYEDATA. SFAR is the receive data superframe alignment output in the NT and LT modes. $\overline{\text{TSEN}}$ is an active low open–drain buffer enable output, used for enabling a bus driver to buffer MCU data out from the MC145572, onto a PCM highway. $\overline{\text{TSEN}}$ is active only when D_{out} is active. In full GCI mode, this pin is the S1 input.
TxSFS SFAX	TxSFS SFAX	S0	9	26	In either MCU mode, this pin may carry either TxSFS output, or SFAX input/output. When this pin is unused, connect a 100 kΩ resistor to V_{SS} in LT mode. TxSFS is provided for compatibility to the MC145472, which provides an absolute transmit superframe reference. SFAX is the transmit data superframe alignment input in the LT mode, or superframe alignment output in the NT mode. In LT mode, SFAX can also be an output. In full GCI mode, this pin is the S0 input.

Table 3–4. 2B1Q Interface Pins (See Section 3.3.5)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
TxP, TxN	36, 39	9, 12	Positive and negative outputs of the differential transmit driver.
RxP, RxN	32, 33	5, 6	Positive and negative inputs to the differential receive circuit.
$V_{ref}P$, $V_{ref}N$	35, 34	8, 7	Positive and negative signals for internal voltage reference. Connect a 0.1 μF to 1 μF ceramic capacitor between $V_{ref}P$ and $V_{ref}N$

Table 3–5. Phase Locked Loop and Clock Pins (See Section 3.3.6)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
FREQREF	25	42	LT mode: 8 kHz reference clock input (Schmitt trigger input). NT mode: optional synchronized clock output, selected by control register in the MCU mode (MCU/$\overline{GCI}$ = 1).
$XTAL_{in}$, $XTAL_{out}$	16, 15	33, 32	Input and output signals of the 20.48 MHz crystal oscillator amplifier.

3.3 PIN DESCRIPTIONS

The following descriptions are divided into the same functional groups as the Pin Description Quick Reference Tables in **Section 3.2** and provide more information about the particular subsystem of the device and the associated pins. Refer to Figures 11–1 and 11–2 for pin assignments.

3.3.1 Power Supply Pins

The MC145572 has five pairs of V_{DD} and V_{SS} power supply pins. Each of these pairs provide power to a specific portion of the integrated circuit to minimize interaction between the various high performance subsystems on the device. All of the negative power supply pins should be connected to the same ground reference point and all of the positive power supply pins should be connected to the same + 5 V power supply source.

NOTE

See **Appendix C** for printed circuit board layout recommendations.

V_{DD}: Positive Power Supply

This is one of the five positive power supply pins and should be connected to + 5 V. V_{DD} provides power to the internal digital circuits of the device and should be decoupled with a 0.1 μF ceramic capacitor to V_{SS}.

V_{SS}: Negative Power Supply

Two of the six negative power supply pins are V_{SS}, and they should be connected to ground. These pins provide a ground reference to the internal digital circuits of the device and each should be decoupled with separate 0.1 μF ceramic capacitors to V_{DD}.

V_{DD}Rx, V_{DD}Tx: Positive Analog Power Supply

Two of the five positive power supply pins are V_{DD}Rx and V_{DD}Tx, and they should be connected to + 5 V. These pins provide power to the analog receive and transmit subsystems of the MC145572, and each should be decoupled with separate 0.1 μF ceramic capacitors to V_{SS}Rx and V_{SS}Tx, respectively. These two pins are not tied together internally.

$V_{SS}Rx$, $V_{SS}Tx$: Negative Analog Power Supply

Two of the six negative power supply pins are $V_{SS}Rx$ and $V_{DD}Rx$, and they should be connected to ground. These pins provide a ground reference to the analog receive and transmit subsystems of the device, and each should be decoupled with separate 0.1 µF ceramic capacitors to $V_{DD}Rx$ and $V_{DD}Tx$, respectively.

$V_{DD}I/O$: Positive Power Supply Input/Output

Two of the five positive power supply pins are $V_{SS}I/O$, and they should be connected to + 5 V. These pins provide power to the digital input and output circuits of the device and each should be decoupled with a 0.1 µF ceramic capacitor to $V_{SS}I/O$. These pins can also be connected to 3.3 V to provide I/O compatibility with 3 V interface devices.

$V_{SS}I/O$: Negative Power Supply Input/Output

Two of the six negative power supply pins are $V_{SS}I/O$, and they should be connected to ground. These pins provide a ground reference to the digital input and output circuits of the device, each should be decoupled with a 0.1 µF ceramic capacitor to $V_{DD}I/O$.

CAP3V: Core Logic Positive Power Supply

This pin is tied to the internal core logic power supply. An external 0.1 µF to 1.0 µF decoupling capacitor should be connected between this pin and ground. Applications requiring a 3 V power supply may source current from this pin. See Section 10.3, ***Electrical Specifications***, for more information on the limit of the source current. This output is at 5 V until reset is applied to the MC145572.

3.3.2 Mode Selection Pins

These inputs define the mode of operation for the MC145572. More information on the function of the device in specific modes can be obtained from Chapter 5, ***MCU Mode Device Functionality*** and Chapter 8, ***GCI Mode Functional Description***.

$\overline{\text{RESET}}$: Reset Input

A logic 0 applied to this Schmitt trigger input pin holds the device in a hardware reset condition. A logic 1 puts the device into the normal operating state. Register NR0(b3) provides a similar software reset function, thereby allowing control of this mode from the external microcontroller. This pin must be held low for at least six 20.48 MHz clock periods.

CAUTION

Reset must be asserted until V_{DD} is greater than 4.75 V and the oscillator is stable.

During a hardware reset condition, all SCP registers are reset to their default state, and the signals output from the DCL and FSR pins when in the MCU Master mode are halted. In addition, the Tx driver is put into a low impedance state to terminate the U–interface and the 2B1Q receiver is unable to detect the activation wake–up tone.

NT/$\overline{\text{LT}}$: NT/LT Select Input

A logic 1 applied to this pin puts the device into the NT mode and a logic 0 puts the device into the LT mode. Note that Byte register 8, bit 0, also controls NT versus LT mode selection, thereby allowing software control of this mode.

Table 3–6. Operation Mode as Indicated by Mode Input Pins

Mode	MCU/$\overline{GCI}$	PAR/$\overline{SER}$
GCI	0	0
MCU/PCP	1	1
MCU/SCP	1	0

NOTES: PCP — Parallel Control Port, external MCU uses 8–bit data port to access registers.
SCP — Serial Control Port, external MCU uses four signal serial ports to access registers.

MCU/$\overline{GCI}$: MCU/GCI Select Input

A logic 1 applied to this pin selects the MCU mode. This requires an external MCU to access the internal control/status register of the MC145572. 2B+D data only is transferred over the time division multiplex bus. In MCU mode, four data formats are available on the IDL2 interface. These are short frame, long frame, GCI 2B+D, and timeslot assigner. A logic 0 applied to this pin selects the GCI time division bus mode.

In GCI mode, 2B+D data and control/status information is interfaced to the MC145572 by a single four signal time division multiplexed bus. The SCP interface is not used and those pins are redefined.

In full GCI mode, both MCU/$\overline{GCI}$ and PAR/$\overline{SER}$ must be connected to V_{SS}.

PAR/$\overline{SER}$: Parallel/Serial Select Input

This pin allows parallel versus serial control port selection when the MC145572 is operating in MCU mode. PAR/$\overline{SER}$ = 1 selects parallel port operation. PAR/$\overline{SER}$ = 0 selects serial control port operation. This pin must be connected to V_{SS} when MCU/$\overline{GCI}$ is connected to V_{SS} (i.e., in full GCI mode).

3.3.3 Time Division Multiplex Data Interface Pins

This section describes the Time Division Multiplex (TDM) data interface pins.

M/$\overline{S}$: Master/Slave Select Input

The TDM interface can be configured as a Master or a Slave with the M/$\overline{S}$ pin. A logic 1 input at this pin selects the Master mode and a logic 0 selects the Slave mode. The polarity of this pin can be inverted using BR7(b1).

When the MC145572 is configured for master timing and MCU mode, the FSR/FSC, FSX, and DCL pins are outputs and their signals are generated internally. As a Master, the U–interface transceiver provides a 2.048 MHz, 2.56 MHz, or 512 kHz DCL output as selected in BR7(b2) and OR7(b4).

When the MC145572 is configured for slave timing and MCU mode, the FSR/FSC, FSX, and DCL pins are inputs and their signals are provided externally. As a Slave, the TDM interface block is designed to accept any clock rate from 256 kHz to 4.096 MHz, inclusive.

In GCI Master mode, FSC, D_{out}, and DCL pins are outputs and D_{in} is an input. Either the 512 kHz or 2.048 MHz clock is available on DCL. FSX is not used.

In GCI Slave mode, D_{out} is an output and FSC, DCL, and D_{in} are inputs. FSX is not used. DCL can accept clock rates up to 8.192 MHz.

FSR/FSC

FSR: MCU Mode Frame Synchronization Receive

FSR is the 8 kHz frame sync for the receive data of the TDM interface. In short frame and timeslot assigner mode, the signal at this pin is high for one cycle of the DCL signal

and is rising edge aligned with the rising edge of the DCL signal. This pin is an input when the TDM interface is in Slave mode and an output in the Master mode as established by the M/$\overline{S}$ pin. See Figures 5–17 through 5–20.

When the MC145572 is in NT mode and M/$\overline{S}$ = 1, this output is phase locked to the signal received at the U–interface. As an LT in the Master mode, this output is derived directly from the 20.48 MHz master clock. The frequency of the periodic FSR signal is 8 kHz. As a Slave, the FSR signal must occur at an average rate of 8 kHz (125 μs interval) with a maximum phase deviation from a jitter–free sync of ± 48 μs.

In Master mode, FSR and FSX output the same waveform. In Slave mode, both FSR and FSX inputs must be driven by external circuitry. FSR and FSX inputs can be tied together in Slave mode and a common sync can be used to drive both inputs.

FSC: GCI Mode Frame Synchronization Receive

In full GCI mode and in GCI 2B+D mode, this pin serves as the FSC pin, and the signal is high for two cycles of the DCL signal and the rising edge is aligned with the rising edge of the DCL signal. This pin is an input when the TDM interface is in Slave mode and an output in Master mode as established by the M/$\overline{S}$ pin. FSC indicates a superframe boundary by going high for one DCL clock. This happens once every 12 ms.

When the MC145572 is in NT mode and M/$\overline{S}$ = 1, this output is phase locked to the signal received at the U–interface.

As an LT in the Master mode, this output is derived directly from the 20.48 MHz master clock. The frequency of the periodic FSR signal is 8 kHz.

As a Slave, the FSC signal must occur at an average rate of 8 kHz (125 μs interval) with a maximum phase deviation from a jitter free sync of ± 48 μs.

FSX: MCU Mode Frame Synchronization Transmit

FSX is the 8 kHz frame sync for the transmit data of the MCU interface. This pin is not used in the GCI mode. The formatting of FSX is mode dependent.

This pin is an input when the TDM interface is in the Slave mode and an output in Master mode, as established by the M/$\overline{S}$ pin.

When the MC145572 is in NT mode and M/$\overline{S}$ = 1, this output is phase locked to the signal received at the U–interface. As an LT in the Master mode, this output is derived directly from the 20.48 MHz master clock. The frequency of the periodic FSR signal is 8 kHz. As a Slave, the FSX signal must occur at an average rate of 8 kHz (125 μs interval) with a maximum phase deviation from a jitter free sync of ± 48 μs.

In Master mode, FSR and FSX output the same waveform. In Slave mode, both FSR and FSX inputs must be driven by external circuitry. FSR and FSX inputs can be tied together in the Slave mode and a common sync can be used to drive both inputs.

DCL: Data Clock Input/Output

This pin is an input when the TDM interface is in the Slave mode and an output in the Master mode, as established by the M/$\overline{S}$ pin.

As a timing master in the MCU–NT mode, this pin provides a 2.048 MHz, 512 kHz, or a 2.56 MHz MCU clock output. This choice is programmed in BR7(b2) and OR7(b4). Also see **Section 5.4**.

When configured as a slave in MCU mode, this pin accepts any clock frequency from 256 kHz to 4.096 MHz, inclusive.

In GCI mode, this pin provides clock outputs 2.048 MHz or 512 kHz, as selected by CLKSEL. In GCI Slave mode, this pin accepts clock frequencies of 512 kHz to 8.192 MHz, inclusive.

In NT master timing of operation, recovered timing is conveyed over DCL by adjusting the width of the clock. The adjustment is made by the internal digital PLL and occurs during two consecutive 8 kHz frames, once per U–interface basic frame. The adjustment consists of

adding or subtracting a single 20.48 MHz clock period during the high time of DCL. Since this occurs during two consecutive 8 kHz frames, the total adjustment is ± 97 ns, once every basic frame. See Chapter 10, ***Electrical Specifications,*** for the locations of the timing adjustment.

D_{out}: Data Transmit Output

This pin is the output for the 2B+D data received at the U–interface. The formatting of the data is mode dependent. In GCI mode, D_{out} is an open drain output and must be connected to V_{DD} through a pullup resistor. In IDL–2 mode, D_{out} goes high impedance when the 2B+D transfer is complete. Refer to Chapter 5, ***MCU Mode Device Functionality*** and Chapter 8, ***GCI Mode Functional Description,*** for more information.

D_{in}: Data Receive Input

This pin is the input for the 2B+D data to be transmitted at the U–interface. The formatting of the data is mode dependent. Refer to Chapter 5, ***MCU Mode Device Functionality*** and Chapter 8, ***GCI Mode Functional Description,*** for more information. In GCI mode, D_{in} must be connected to V_{DD} through a 1.5 kΩ pull-up resistor.

3.3.4 Control/Status Interface Pins

These pins provide a digital transfer interface for the MC145572 when configured for MCU mode. In GCI mode, control and status information is provided over the GCI interface.

$\overline{SCPEN}$/$\overline{CS}$/IN1

$\overline{SCPEN}$: Serial Control Port Enable Input

This pin, when held low, selects the SCP for the transfer of control, status, and M channel data information into and out of the U–interface transceiver. $\overline{SCPEN}$ should be held low for 8 or 16 periods of the SCPCLK signal in order for information to be transferred into or out of the MC145572. The SCP interface disregards any SCP operation that is not exactly 8 or 16 SCPCLK clock pulses in length. If the MC145572 is the only SCP device in the system, this pin can be tied low and bursted SCP clock can be used to access the register.

$\overline{CS}$: Parallel Control Port Chip Select

In Parallel Control Port mode, this pin acts as an active low chip select input.

IN1: Input 1

In full GCI mode, defined when MCU/$\overline{GCI}$ = 0, this is an input bit. IN1 may be read via BR7. In NT mode, IN1 is transmitted as PS1 in the M4 maintenance bits.

SCPCLK/R/$\overline{W}$/IN2

SCPCLK: Serial Control Port Clock Input

This is an input to the device used for clocking data into and out of the SCP interface. Data is clocked into the MC145572 from SCPRx on rising edges of SCPCLK. Data is shifted out of the MC145572 SCPTx pin on falling edges of SCPCLK. SCPCLK can be any frequency from 0 up to 4.096 MHz. An SCP transaction takes place when $\overline{SCPEN}$ is brought low. Note that SCPCLK is ignored when $\overline{SCPEN}$ is high (i.e., it may be continuous or it can operate in a burst mode). If the MC145572 is the only SCP device used, the $\overline{SCPEN}$ pin can be tied low and bursted clocks applied to SCPCLK.

R/$\overline{W}$: Parallel Control Port Read/Write

In Parallel Control Port mode, this pin functions as read versus write indication, where write is active low.

IN2: GCI Mode Input 2

IN2 may be read via BR7. In NT mode, IN2 is transmitted as PS2 in the M4 channel maintenance bits.

SCPRx/D0/OUT1

SCPRx: Serial Control Port Receive Input

SCPRx is used to input control, status, and M channel data information to the U–interface transceiver. Data is shifted into the MC145572 on rising edges of SCPCLK. SCPRx is ignored when data is being shifted out of SCPTx or when $\overline{\text{SCPEN}}$ is high.

D0: Data 0

In Parallel Control Port mode, this pin functions as bit 0, LSB, of the data bus.

OUT1: GCI Mode Output 1

In full GCI mode, defined by MCU/$\overline{\text{GCI}}$ = 0, OUT1 is an output reflecting the state of the bit as set in BR7. OUT1 is also set high when the GCI Command/Indicate channel command LTD1 is active.

SCPTx/D1/OUT2

SCPTx: Serial Control Port Transmit Output

SCPTx is used to output control, status, and M channel data information from the MC145572 U–interface transceiver. Data is shifted out of SCPTx on the falling edge of SCPCLK, most significant bit first.

D1: Data 1

In Parallel Control Port mode, this pin functions as bit 1 of the data bus.

OUT2: GCI Mode Output 2

In full GCI mode, defined by MCU/$\overline{\text{GCI}}$ = 0, OUT2 is an output reflecting the state of the bit as set in BR7. OUT2 is also set high when the GCI Command/Indicate channel command LTD2 is active.

$\overline{\text{IRQ}}$: Interrupt Request Output

The $\overline{\text{IRQ}}$ pin is an active low, open drain output, used to signal an external microcontroller that an interrupt condition exists in the MC145572. On clearing the interrupt condition, the pin is returned to the high impedance state. See the description for Nibble Register 3, **Section 4.3.4**, for descriptions of the sources of interrupt conditions.

4.096 CLKOUT/D2

4.096 CLKOUT: 4.096 MHz Buffered Clock Output

This pin provides a buffered 4.096 MHz clock output that can be used for a microcontroller clock. This clock is not locked to the recovered clock timing. This output can be disabled by writing a 1 to OR9(b0).

D2: Data 2

In Parallel Control Port mode, this pin functions as bit 2 of the data bus.

15.36 CLKOUT/D3

15.36 CLKOUT: 15.36 MHz Buffered Clock Output

This pin provides a buffered 15.36 MHz clock output that can be used for the MC145474/75 and MC145574 S/T transceiver clocks. Register BR14(b0) or Register BR15A(b2) must be set to enable this output. This clock is a 20.48 MHz clock with every fourth clock cycle removed. This clock is not locked to the recovered clock timing. This output can be disabled by writing a 1 to OR9(b1). This output can be cleanly transitioned to 10.24 MHz by writing a 1 to OR9(b3).

NOTE

This pin does not provide a 50% duty cycle output. It does provide a clock that the MC145474/75 and MC145574 can use. Figure 10–14 shows the timing of this signal.

D3: Data 3

In Parallel Control Port mode, this pin functions as bit 3 of the data bus.

BUFXTAL/D4

BUFXTAL: Buffered Crystal Output

BUFXTAL is the buffered square wave output from the 20.48 MHz oscillator. After reset, this signal is active. This output can be set to a high impedance state by setting OR9(b2) to a 1. This signal is available in both MCU/SCP and GCI modes of operation.

CAUTION

In NT mode operation, this signal is not phase locked to recovered timing.

D4: Data 4

In Parallel Control Port mode, this pin functions as bit 4 of the data bus.

EYEDATA/DCHCLK/D5/S2

EYEDATA: Eye Pattern Data Output

Eye Pattern Data is a serial data output that provides a digital word once per received 2B1Q baud. This data word represents the recovered 2B1Q received bauds and can be used to reconstruct a conventional eye pattern on an oscilloscope with the use of a digital–to–analog converter. Control bit BR15A(b0) must be set to a 1 to enable this pin. See **Appendix D** for applications information concerning this feature.

DCHCLK: D Channel Clock

DCHCLK is the D channel port clock output. It is enabled by setting D channel port enable in Init Group register OR8 (b0).

D5: Data 5

In Parallel Control Port mode, this pin functions as bit 5 of the data bus.

S2: GCI Mode Slot Selection 2

In full GCI mode, this pin is an input for the timeslot selection, S0 – S2. See Table 3–7 for more information.

Table 3–7. GCI Timeslot Assignment as Set by S0 – S2

GCI Timeslot	S2	S1	S0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

TxBCLK/DCH$_{in}$/D6/FREF$_{out}$

TxBCLK: Transmit Baud Clock Output

This 80 kHz clock indicates the timing of the transmitted 2B1Q bauds. Control bits BR14(b0) or BR15A(b0) must be set to logic 1 to enable this signal.

DCH_{in}: D Channel Data In

DCH_{in} is the D channel port serial input. It is enabled by setting D channel port enable in Init Group register OR8(b0).

D6: Data 6

In Parallel Control Port mode, this pin functions as bit 6 of the data bus.

$FREF_{out}$: GCI Mode Locked Frequency Output

In full GCI mode, operating as a slave, this pin provides 2.048 MHz or 512 kHz synchronized clock output as selected by CLKSEL. When the MC145572 is configured as a GCI timing master, $FREF_{out}$ does not provide a clock since the clock is present on DCL. It is not necessary to set any register bits to enable this output in GCI slave mode.

RxBCLK/DCH_{out}/D7/CLKSEL

RxBCLK: Transmit Baud Clock Output

This 80 kHz clock indicates the timing of the received 2B1Q bauds. Control bits BR14(b0) or BR15A(b0) must be set to logic 1 to enable this signal.

DCH_{out}: D Channel Data Out

DCH_{out} is the D channel port serial output. It is enabled by setting D channel port enable in Init Group register OR8(b0).

D7: Data 7

In Parallel Control Port mode, this pin functions as bit 7 of the data bus.

CLKSEL: Clock Select

When operating as a GCI timing master in full GCI mode, CLKSEL selects between 512 kHz and 2.048 MHz for DCL. CLKSEL = 1 selects 2.048 MHz.

When operating as a GCI timing slave in full GCI–NT mode, CLKSEL selects between phase locked 512 kHz and 2.048 MHz clocks appearing at $FREF_{out}$.

SYSCLK/SFAR/$\overline{TSEN}$/S1

SYSCLK: System Clock Output

System Clock Output is a 10.24 MHz clock that is used to clock Eye Pattern Data. Control bits BR14(b0) or BR15A(b0) must be set to a 1 to enable this signal. See **Appendix D** for applications information concerning this pin.

SFAR: Superframe Alignment Receive

SFAR provides a superframe alignment output signal in the NT and LT modes. This signal is only available when the MC145572 is in MCU mode. Setting OR8 (b1) enables this output. This signal is one MCU clock wide and occurs during the DCL clock following FSR. See **Section 5.4.7**. This pulse indicates the first 2B+D frame received from a U–interface superframe.

$\overline{TSEN}$: Open–Drain Buffer Enable Output

$\overline{TSEN}$ is an open–drain buffer enable output, used for enabling a bus driver to buffer TDM data out from the MC145572 onto a PCM highway. When the MC145572 is configured for MCU mode, $\overline{TSEN}$ is active during the B1, B2, and D channel timeslots, regardless of where they occur. When the MC145572 is configured for GCI 2B+D electrical–only interfacing while in MCU mode, $\overline{TSEN}$ is active during the B1, B2, and D channel timeslots only. $\overline{TSEN}$ is also available when the MC145572 is configured for timeslot assigner operation. When a separate D channel serial port option is enabled, $\overline{TSEN}$ is active only during the B1 and B2 channel timeslots. This pin is enabled when OR7(b5) = 1 or OR8(b3) = 1.

S1: GCI Mode Slot Selection 1

In full GCI mode, this pin is an input for the timeslot selection, S0 – S2.

TxSFS/SFAX/S0

TxSFS: Transmit Superframe Sync Output

This output pulses high, 8 bauds prior to the transmit sync word separating the first and second transmitted basic frames in a superframe. Control bits BR14(b0) and BR15A(b3) must both be set to a 1 to enable this pin. The TxSFS output is coincident with the Tx Baud Clock.

TxSFS is provided for compatibility to the MC145472, which provides an absolute transmit superframe reference.

SFAX: Superframe Alignment Transmit

SFAX is the transmit superframe alignment input in the LT mode, or superframe alignment output in the NT mode. SFAX is enabled by setting SFAX/SFAR Enable in Init Group register OR8 (b1). SFAX may be configured as an output in LT mode by setting OR8 (b5). See **Sections 4.5.9 and 5.4.7.** When GCI 2B+D mode is enabled, MCU/$\overline{GCI}$ = 1, and OR6(b3) = 1, the SFAX function is superceded by modulation of the FSC input. This pulse indicates the first 2B+D IDL frame transmitted onto the U–interface superframe.

WARNING

In MCU mode (MCU/$\overline{GCI}$ pin connected to V_{DD}), this pin function becomes undefined after a hardware or software reset. Most applications do not use any of the features available at this pin. In such cases, a 10 kΩ resistor must be connected between this pin and V_{SS}. In the rare applications that enable any of the functions available at this pin, the 10 kΩ resistor may not be required. This applies to both NT and LT mode operation.

S0: Slot Selection 0

In full GCI mode, this pin is an input for the timeslot selection, S0 – S2.

3.3.5 2B1Q Line Interface Pins

These pins form the 2B1Q interface of the MC145572 U–interface transceiver. Refer to **Appendix E** for information on the line interface. Refer to **Appendix B** for component sourcing.

TxP and TxN: Transmit Positive and Transmit Negative Outputs

These are the differential analog output pins of the transmit line driver.

RxP and RxN: Receive Positive and Receive Negative Inputs

These are the differential analog input pins to the 2B1Q receiver.

$V_{ref}P$ and $V_{ref}N$: Reference Voltage Positive and Reference Voltage

Connect a 0.1 µF ceramic capacitor between these pins.

3.3.6 Crystal Oscillator and Phase Locked Loop (PLL) Pins

In LT mode, the MC145572 derives its 20.48 MHz master clock from a clock reference using an on–chip PLL with an 8 kHz clock reference applied to pin FREQREF.

In NT mode, no reference clock is required, since timing is recovered from the line. External circuitry is the same for both NT and LT modes.

FREQREF: Frequency Reference

LT Mode: This Schmitt trigger digital input pin accepts the 8 kHz reference frequency for the analog phase locked loop in LT mode. Typically, this clock can be the same 8 kHz synchronization input as connected to FSR or FSX. For ISDN central office applications, the frequency applied at this pin should be stable to ± 5 ppm to meet

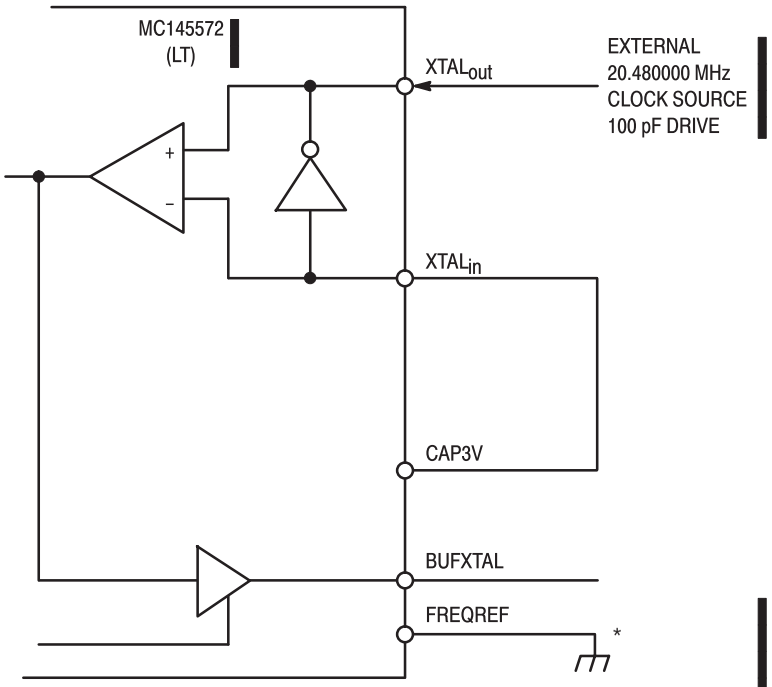
ANSI T1.601–1992 requirements. Some ANSI and ETSI applications require a ± 32 ppm reference.

NT Mode: In MCU/$\overline{GCI}$ = 1 mode, FREQREF can be enabled as an output when the MC145572 is configured for NT mode by setting OR8(b4) to a 1. This signal outputs the internally–generated DCL clock when enabled. Its frequency is programmed by the DCL frequency bits BR7(b2) and OR7(b4).

GCI Mode: In MCU/$\overline{GCI}$ = 0 mode, a separate pin, $FREF_{out}$, provides the synchronized clock and is available for all configurations except for when TxBCLK is enabled. Use the CLKSEL pin to select between 512 kHz and 2.048 MHz in NT mode.

$XTAL_{in}$ and $XTAL_{out}$: Crystal Input and Crystal Output

A 20.48 MHz pullable crystal is connected between $XTAL_{in}$ and $XTAL_{out}$ to form a voltage–controlled crystal oscillator in the LT or NT modes. No other external components are required. See **Section H.3** for information on how to characterize the pullable crystal.



*Required for LT mode only.

Figure 3–1. Method to Drive MC145572 with External Clock

3.3.7 Crystal Oscillator Description

In LT mode, an internal PLL synchronizes a voltage controlled 20.48 MHz crystal oscillator to an 8 kHz reference frequency supplied by the switching equipment. This phase–locked clock assures that the transmitted 2B1Q signal is synchronized to the frequency reference supplied at the FREQREF pin. In addition, the very low frequency response (1 Hz) of the internal PLL loop filter limits jitter present in the frequency reference.

In NT mode, the MC145572 synchronizes its DCL clock output pin to the recovered timing from the U–interface. This clock is available at 512 kHz, 2.048 MHz, and 2.56 MHz. Frequency adjustments are also made to the 20.48 MHz oscillator, but it is not precisely locked to the recovered 2B1Q signal

at all times. This means that the $BUFXTAL_{out}$ pin can not be used as a master clock source in applications that require a synchronized clock. In NT mode, the U–interface transceiver can lock to 80 kbaud ± 32 ppm receive signals.

A single 20.48 MHz pullable crystal must be connected between $XTAL_{in}$ and $XTAL_{out}$ pins of the MC145572. Refer to **Appendix B** for crystal specifications and sourcing information. The crystal specified for the NT mode operation will operate in LT applications. The crystal specified for LT applications *will not* operate in NT applications. The reason is that the NT mode crystal has a tighter overall frequency tolerance than the LT mode crystal.

NOTE

Motorola continues to qualify several third party sources for the 20.48 MHz crystal. Contact your local Motorola representative or Motorola factory applications staff for the latest information regarding component sourcing.

4

MCU MODE REGISTER DESCRIPTION REFERENCE

4.1 INTRODUCTION

This chapter describes all of the MC145572 U–interface transceiver control and status registers available via the Serial and Parallel Control Ports. Tables 4–1 through 4–3 contain Register Maps and **Section 4.2.1** contains a Register Index. See **Section 4.3** for detailed descriptions of each register.

The internal registers of the MC145572 are used when the device is in MCU mode. When in GCI mode, MCU/$\overline{GCI}$ = 0, the MC145572 is controlled via the C/I and Monitor channels and it is not necessary to access the registers in normal applications.

The MC145572 provides a PCP interface mode that provides access to all control registers. See **Section 5.3.2** for more information on the use of the PCP interface.

The register map for the MC145572 is nearly identical to that for the MC145472 after a hardware or software reset. Reserved bits in the MC145472 register map have been redefined to permit access to new registers in the MC145572. Most software developed for the MC145472 will work for the MC145572 without modifications.

The MC145572 SCP interface is pin–for–pin identical to that of MC145474/75 and MC145574 S/T–interface transceivers. Using the same interface as the MC145474/75 provides a common interface for applications utilizing both the MC145572 and the MC145474/75 and for applications that can use either device, such as line cards or terminal equipment.

In addition to being pin–for–pin compatible, the architecture of the register map and the SCP interface is nearly identical to that of the MC145474/75. This simplifies the code development effort and minimizes device driver code size for the microcontroller.

For complete information on the operation of Control interfaces, see **Section 5.3**.

Table 4–1. Nibble Registers and R6 Map (NR0 – NR5; R6) — See Section 4.3

	b3	b2	b1	b0
NR0	Software Reset	Power–Down Enable	Absolute Power–Down	Return to Normal
NR1	Linkup	Error Indication	Superframe Sync	Transparent Activation in Progress
NR2	Activation Request	Deactivation Request	Superframe Update Disable	Customer Enable
NR3	$\overline{IRQ3}$	$\overline{IRQ2}$	$\overline{IRQ1}$	$\overline{IRQ0}$
NR4	Enable $\overline{IRQ3}$	Enable $\overline{IRQ2}$	Enable $\overline{IRQ1}$	Enable $\overline{IRQ0}$
NR5	Reserved	Block B1	Block B2	Swap B1/B2

	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1	eoc a2	eoc a3	eoc dm	eoc i1	eoc i2	eoc i3	eoc i4	eoc i5	eoc i6	eoc i7	eoc i8

Table 4–2. Byte Register Map (BR0 – BR15A)

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40	M41	M42	M43	M44	M45	M46	M47
BR1	M40	M41	M42	M43	M44	M45	M46	M47
BR2	M50	M60	M51	febe Input	Reserved	Reserved	Reserved	Reserved
BR3	M50	M60	M51	Received febe	Computed nebe	Verified act	Verified dea	Superframe Detect
BR4	febe Counter 7	febe Counter 6	febe Counter 5	febe Counter 4	febe Counter 3	febe Counter 2	febe Counter 1	febe Counter 0
BR5	nebe Counter 7	nebe Counter 6	nebe Counter 5	nebe Counter 4	nebe Counter 3	nebe Counter 2	nebe Counter 1	nebe Counter 0
BR6	U–Loop B1	U–Loop B2	U–Loop 2B+D	U–Loop Transparent	IDL2–Loop B1	IDL2–Loop B2	IDL2–Loop 2B+D	IDL2–Loop Transparent
BR7	BR15A Select	**OUT2**	**OUT1**	IDL2 Invert	IDL2 Free Run	IDL2 Speed	IDL2 M/$\overline{S}$ Invert	IDL2 8/10
		GCI IN2	**GCI IN1**					
BR8	Frame Steering	Frame Control 2	Frame Control 1	Frame Control 0	crc Corrupt	Match Scrambler	Receive Window Disable	NT/$\overline{LT}$ Invert
	Frame State 3	Frame State 2	Frame State 1	Frame State 0	Reserved	Reserved	Reserved	NT/$\overline{LT}$ Mode
BR9	eoc Control 1	eoc Control 0	M4 Control 1	M4 Control 0	M5/M6 Control 1	M5/M6 Control 0	febe/nebe Control	Reserved
BR10	Reserved	Reserved	Reserved	Reserved	Reserved	Select Dump Access	Select DCH Access	Select Overlay
BR11	Activation Control 6	Activation Control 5	Activation Control 4	Activation Control 3	Activation Control 2	Activation Control 1	Activation Control 0	Activation Timer Disable
	Activation State 6	Activation State 5	Activation State 4	Activation State 3	Activation State 2	Activation State 1	Activation State 0	Activation Timer Expire
BR12	Activation Control Register	Interpolate Enable	Load Activation State	Step Activation State	Hold Activation State	Jump Select	Reserved	Force Linkup
	EPI 18	EPI 17	EPI 16	EPI 15	EPI 14	EPI 13	EPI 12	EPI 11
BR13	Enable MEC Updates	Accumulate EC Output	Enable EC Updates	Fast EC Beta	Accumulate DFE Output	Enable DFE Updates	Fast DFE/ARC Beta	Clear All Coefficients
	EPI 10	EPI 9	EPI 8	EPI 7	EPI 6	EPI 5	EPI 4	EPI 3
BR14	Reserved	ro/wo to r/w	Reserved	Framer–to–Deframer Loop	± 1 Tones	Reserved	Reserved	Enable CLKs
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Mask 7	**Mask 6**	**Mask 5**	Mask 4	Mask 3	Mask 2	Mask 1	Mask 0
BR15A	FREQ ADAPT	Jump Disable	Reserved	Reserved	Enable TxSFS	Reserved	Reserved	Enable Eye Data and Baud Clock
				Reserved	Reserved	Reserved	Reserved	Reserved

NOTE: Bits in bold type were reserved bits in the MC145472/MC14LC5472 register map.

Table 4–3. Overlay Register Map (OR0 – OR13)

INIT GROUP REGISTER OVERLAY REGISTERS OR0 – OR9, OR11, AND OR12								
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
OR0	D_{out} B1 Channel Timeslot Bits (7:0)							
OR1	D_{out} B2 Channel Timeslot Bits (7:0)							
OR2	D_{out} D Channel Timeslot Bits (7:0)							
OR3	D_{in} B1 Channel Timeslot Bits (7:0)							
OR4	D_{in} B2 Channel Timeslot Bits (7:0)							
OR5	D_{in} D Channel Timeslot Bits (7:0)							
						GCI Slot (2:0)		
OR6	TSA B1 Enable	TSA B2 Enable	TSA D Enable	GCI Select M4–OR0	GCI Mode Enable	Reserved	Reserved	Reserved
OR7	Internal Analog Loopback	Line Connect	$\overline{\text{TSEN}}$ D Channel Enable	IDL2 Rate 2	IDL2 Long Frame Mode	crc Corrupt Mode	febe/nebe Rollover	M4 Trinal Mode
OR8	D/R Mode 1	D/R Mode 0	SFAX Output Enable	FREQREF Output Enable	$\overline{\text{TSEN}}$ Enable B1, B2	Reserved	SFAX SFAR Enable	D Channel Port Enable
OR9	Reserved	Open Feedback Switches	Analog Loopback	CLKOUT 2048	4096 Hirate	2048 Disable	1536 Disable	4096 Disable
BR10	Reserved	Reserved	Reserved	Reserved	Reserved	**Select Dump Access**	**Select DCH Access**	**Select INIT Group**
D Channel Access Select Overlay								
OR12	D Channel Transmit Bits (7:0)							
	D Channel Receive Bits (7:0)							
Dump/Restore Access Select Overlay								
OR13	Dump Register Write Access (7:0)							
	Dump Register Read Access (7:0)							

4.2 REGISTER MAP

The register map consists of six 4–bit nibble registers (NR0 – NR5), one 12–bit nibble register (R6), seventeen byte registers (BR0 – BR15A), and twelve overlay registers (OR0 – OR9, OR11, and OR12).

4.2.1 Register Index

The following guide lists the registers alphabetically by functional groups and indicates which register number; NR0 – NR5, R6, or BR0 – BR15A, and bit or bits, (b7:b0); to refer to for detailed information.

Activation

Control — BR11(b7:b1)
Control Steer — BR12(b7)
Customer Enable — NR2(b0)
Deactivation Request — NR2(b2)
Error Indication — NR1(b2)
Error Power Indicator — BR12, BR13
Force Linkup — BR12(b0)
Hold Activation State — BR12(b3)
In Progress — NR1(b0)
Jump Select — BR12(b2)
Linkup — NR1(b3)
Load Activation State — BR12(b5)
Request — NR2(b3)
State — BR11(b7:b1)

Diagnostics

± 1 Tones — BR14(b3)
Accumulate DFE Output — BR13(b3)
Accumulate EC Output — BR13(b6)
Clear All Coefficients — BR13(b0)
Enable Clocks — BR14(b0)
Enable DFE Updates — BR13(b2)
Enable EC Updates — BR13(b5)
Enable Eye Data and Baud Clock — BR15A(b0)
Enable MEC Updates — BR13(b7)
Enable TxSFS — BR15A(b3)
Enable 15.36 MHz — BR15A(b2)
Enable 20.48 MHz — BR15A(b1)
Error Power Indicator — BR12, BR13
Fast DFE/ARC Beta — BR13(b1)

Activation (continued)
Step Activation State — BR12(b4)
Superframe Sync — NR1(b1)
Superframe Update Disable — NR2(b1)
Timer Disable — BR11(b0)
Timer Expire — BR11(b0)
Transparent — NR1(b0)
Verified act — BR3(b2), BR9(b5:b4)
Verified dea — BR3(b1), BR9(b5:b4)
Deactivation
Request — NR2(b2)
GCI
IN/OUT — BR7(b6:b5)
GCI Mode Enable — OR6 (b3)
IDL2
Timeslot Assigner
D_{out} B1 Timeslot — OR0
D_{out} B2 Timeslot — OR1
D_{out} D Timeslot — OR2
D_{in} B1 Timeslot — OR3
D_{in} B2 Timeslot — OR4
D_{in} D Timeslot — OR5
TSA Enable — OR6 (b7:b5)
8–Bit/10–Bit Mode — BR7(b0)
Block B1 — NR5(b2)
Block B2 — NR5(b1)
Customer Enable — NR2(b0)
Free Run — BR7(b3)
Invert — BR7(b4)
Loopbacks — See Loopbacks
Master/Slave Invert — BR7(b1)
Speed — BR7(b2)
Swap B1/B2 — NR5(b0)
B1 IDL2 Timeslot Enable — OR6(b7)
B2 IDL2 Timeslot Enable — OR6(b6)
D IDL2 Timeslot Enable — OR6(b5)
IDL2 Long Frame Mode — OR7(b3)
IDL2 Rate — OR7(b4)
Interrupt
Enable — NR5
Status — NR3
Loopbacks
Framer–to–Deframer Loop — BR14(b4)
IDL2–Loop 2B+D — BR6(b1)
IDL2–Loop B1 — BR6(b3)
IDL2–Loop B2 — BR6(b2)
IDL2–Loop Transparent — BR6(b1)
Match Scrambler — BR8(b2)
Receive Window Disable — BR8(b1)
U–Loop 2B+D — BR6(b5)
U–Loop B1 — BR6(b7)
U–Loop B2 — BR6(b6)
U–Loop Transparent — BR6(b4)
Open Feedback Switch — OR9(b6)
Analog Loopback — OR9(b5)
nebe
Computed — BR3(b3)
Control — BR9(b1)
Counter — BR5
febe/nebe Rollover — OR7(b2)
Diagnostics (continued)
Fast EC Beta — BR 13(b4)
Force Linkup — BR12(b0)
Freq Adapt — BR15A(b7)
Jump Disable — BR15A(b6)
Mask — BR15(b4:b0)
ro/wo to r/w — BR14(b6)
Superframe Detect — BR3(b0)
Select Dump Access — BR10(b2)
Select DCH Access — BR10(b1)
D Channel Access Overlay — OR12
Dump/Restore Access Overlay — OR13
eoc
Control — BR9(b7:b6)
act — BR3(b2)
Message — R6
febe
Control — BR9(b1)
Counter — BR4
Input — BR2(b4), BR9(b1)
Received — BR3(b4)
febe/nebe Rollover — OR7(b2)
Maintenance
act — BR3(b2)
crc Corrupt — BR8(b3)
dea — BR3(b1)
eoc — See eoc
febe — See febe
M4 Trinal Mode — OR7(b0)
M4 Control — BR9(b5:b4)
M4 Send — BR0
M4 Received — BR1
M5/M6 Control — BR9(b3:b2)
M50 Received — BR3(b7)
M50 Send — BR2(b7)
M51 Received — BR3(b5)
M51 Send — BR2(b5)
M60 Received — BR3(b6)
M60 Send — BR2(b6)
nebe — See nebe
Return to Normal — NR0(b0)
Superframe Update Disable — NR2(b1)
Verified act — BR3(b2)
Verified dea — BR3(b1)
Mode
Absolute Power–Down — NR0(b1)
NT/LT Invert Mode — BR8(b0)
NT/LT Mode — BR8(b0)
Power–Down Enable — NR0(b2)
Software Reset — NR0(b3)
GCI 2B+D Mode — OR6(b3)
Superframe Framer
Frame Control — BR8(b6:b4)
Frame State — BR8(b7:b4)
Frame Steering — BR8(b7)

4.2.2 Bit Description Legend

Each bit described in the following sections has a read/write indicator associated with it. This indicator, shown in the lower right corner of each bit, shows what type of bit resides there. The options are described in Table 4–4.

Table 4–4. Bit Read/Write Indicator

Indicator	Type	Description
rw	Read/Write	A Read/Write bit may be written to by the external microcontroller. The information that is read back will be the data that was written.
ro	Read–Only	A Read–Only bit may be read by the external microcontroller. Writing to it has no effect unless otherwise specified in the text. When the text says that an “ro” bit is set or cleared, this operation is performed internally.
ro/wo	Read–Only/Write–Only	A Read–Only/Write–Only bit may be written to by the external microcontroller. However, the value that is read back by the external microcontroller is not necessarily the value that was written. An “ro” bit is set and cleared by some internal operation in the U–interface transceiver.

NOTE

Byte register 14 includes a bit (BR14(b6)) that converts all of the write–only (wo) registers to read/write registers for diagnostic purposes. If not specified, a register is not affected by BR14(b6) and operates as discussed for all modes.

4.3 NIBBLE REGISTERS

4.3.1 NR0: Reset and Power-Down Register

This register contains read/write control bits. All bits are cleared on Hardware Reset ($\overline{\text{RESET}}$), but are unaffected by Software Reset (NR0(b3)). This register is write–only when the U–interface transceiver is in Absolute Power–Down mode (NR0(b1)).

CAUTION

NR0 should not be modified while device is in GCI mode.

	b3	b2	b1	b0
NR0	SOFTWARE RESET rw	POWER–DOWN ENABLE rw	ABSOLUTE POWER–DOWN rw	RETURN TO NORMAL rw

Software Reset

This bit forces the U–interface transceiver into a reset state. Setting this bit to 1 causes a software reset. To allow the transceiver to resume operation, this bit must be cleared by either writing a 0 to it or asserting hardware reset. Reset must be asserted for at least six 20.48 MHz clock periods. There must be a 20.48 MHz clock at $XTAL_{in}$ for the MC145572 to reset correctly. This bit has no effect on the contents of NR0 and BR10.

Power–Down Enable

When this bit is set to 1 and the U–interface transceiver is searching for a wake–up tone from the far–end tranceiver, the MC145572 enters the Power–Down mode. In Power–Down mode, the MC145572 transmit drivers and the time division multiplex interface circuitry for both IDL2 and GCI operation are turned off. This bit must be cleared to 0 before enabling the MC145572 to perform any non–activation related functions other than waiting for a wakeup tone. The MC145572 automatically exits from Power–Down mode on one of three conditions:

1. A wakeup tone is detected on the U–interface.

2. The external microcontroller sets the Activation Request bit, (NR2(b3)).
3. This bit is reset to 0.

When this bit is 0, the U–interface transceiver is not permitted to enter power–down mode. The U–interface transceiver has warm start capability regardless of the state of this bit.

Absolute Power–Down

When this bit is 1, the U–interface transceiver enters its Absolute Power–Down mode, the equivalent of a software reset. All clocks except the Phase Locked Loop (PLL) subsystem used in the LT mode are shut off when this bit is set to 1. In NT mode, the oscillator is turned off. All internal bias currents are turned off and the transmit drivers are high impedance. After setting this bit back to 0, the internal circuits resume full power. After this bit is cleared, the Software Reset bit must be set to 1 for approximately 1 ms while the internal clocks stabilize. Absolute Power–Down may also be aborted by a Hardware Reset ($\overline{\text{RESET}}$). During Absolute Power–Down, NR0 is the only register that may be written to. Setting this bit clears all coefficients and forces the transceiver to activate in cold start mode during the next activation procedure.

Return to Normal

This bit is used to return maintenance functions to their normal operating state. When set to 1, the `crc` Corrupt bit (BR8(b3)) and all of the loopback control bits in BR6 are cleared.

4.3.2 NR1: Activation Status Register

This register contains device activation status. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset ($\overline{\text{RESET}}$). If any bit in this register changes from 0 to 1, or if Linkup, Superframe Sync, or Transparent/Activation in Progress change from 1 to 0, an $\overline{\text{IRQ3}}$ (NR3(b3)) is generated. The $\overline{\text{IRQ3}}$ interrupt is cleared by reading NR1.

	b3	b2	b1	b0
NR1	LINKUP r0	ERROR INDICATION ro	SUPERFRAME SYNC ro	TRANSPARENT ACTIVATION IN PROGRESS ro

NOTE

When access to the D channel via register OR12 is enabled, NR1 indicates a D channel interrupt by setting all four status bits to 1s. Reading OR12 clears the special code (1111) from NR1 but does not affect any updates in activation status. So, if there has been a change in activation status, an interrupt is still queued up even though the D channel interrupt has been cleared.

Linkup

This bit is set when the U–interface transceiver has completed an activation up to the point where full–duplex operation of the U–interface has been established. For the ANSI T1.601–1992 defined activation to be completed, the `act` bit in the M4 maintenance bits must still be exchanged. However, from purely a transmit/receive point of view, the U–interface is operational when Linkup is 1. Linkup will remain set until one of four things happens:

1. Receive framing is lost or severely in error, and remains so, for 480 ms.
2. While operating in the NT mode, receive framing is lost after Deactivate Request is set in NR2(b2), or Verified `dea` (BR3(b1)) becomes a 1 during M4 Control mode 0,0 (BR9(b5:b4)).
3. While operating in the LT mode, the Deactivate Request bit (NR2(b2)) is set.
4. A hardware or software reset occurs.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

Error Indication

This bit is set to 1 when a timer expires. Time–out sources are:

1. 15–second Activation Timer (BR11(b0)).
2. 480–ms loss of frame/signal.
3. Failure to get NT1 response to the TL signal (10 ms following the cessation of TL). (TL is 3 ms in duration.)

Error Indication is always automatically reset prior to the next $\overline{\text{IRQ3}}$. This is the result of either setting the Activate Request bit in NR2(b3) or receiving a wakeup tone. Error Indication is not cleared by reading NR1.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

Superframe Sync

This bit is a 1 when the received superframe is being reliably detected. It transitions from 0 to 1 coincident with Linkup being set. Subsequently, if the superframe is lost, Superframe Sync returns to 0, and if Superframe Sync remains 0 for 480 ms, the U–interface transceiver will deactivate. While Superframe Sync is 0, the received maintenance bits are unknown. $\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ0}}$ are not generated while Superframe Sync is 0. The 2B+D data is blocked (forced to all 1s) when Superframe Sync is 0.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

Transparent/Activation in Progress

This bit has a dual purpose. When the transceiver is deactivated, this bit is 0. Whenever an activation begins, this bit is internally set to a 1 and an $\overline{\text{IRQ3}}$ is generated. When the activation process is completed, Linkup is set to 1 indicating success, and this bit remains set to 1, indicating that the receiver and Superframe Deframer are ready to pass data transparently from the U–interface to the IDL2 interface. If the activation process fails, this bit is cleared and Error Indication is set to 1. Whenever Linkup is 1, this bit may be cleared, indicating that the receiver has detected a high error on the U–interface. Under this condition, the receiver blocks received data (forcing the 2B+D data to all 1s) until the error returns to normal.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

NOTE

The received data is not transmitted on the IDL2 interface until Linkup is 1, Superframe Sync is 1, Transparent/Activation in Progress is 1, and either Customer Enable (see NR2(b0)) or Verified `act` (see BR3(b2)) is 1.

D Channel Interrupt

When access to the D channel register OR12 has been enabled by setting BR10(b1), the operation of the NR1 status bits is modified. A D channel available status is indicated by NR1(b3:b0) all being set to 1s. Software must first do a check for NR1 = $F, then perform a check for status of the individual bits. The D channel interrupt is cleared by reading OR12.

4.3.3 NR2: Activation Control Register

Register NR2 contains activation/deactivation control bits. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset ($\overline{\text{RESET}}$).

CAUTION

NR2 normally is not written to in GCI mode; if necessary, NR2 can be written to, but bits b3 and b2 should always be written as 0 while the device is in GCI mode.

	b3	b2	b1	b0
NR2	Activation Request rw	Deactivation Request rw	Superframe Update Disable rw	Customer Enable rw

Activation Request

When this bit is set to 1 and the U–interface transceiver is in ANSI T1.601–1992 defined “Full Reset”, the transceiver will begin an activation. The external microcontroller never needs to set this bit to 0. The bit is internally set to 0 whenever Transparent/Activation in Progress (NR1(b0)) is set to a 1, whenever TL is transmitted in the LT mode, or on hardware or software reset. If the activation fails for any reason, the Activation Request bit must be set to 1 once again to initiate another activation attempt. The transceiver self–activates if an incoming tone is detected when in LT or NT mode. Once activation starts, the MC145572 automatically clears this bit. Do not continuously reassert this bit. It only needs to be set once per activation attempt.

Deactivation Request

When this bit is set to 1 in the LT mode; upon reaching Linkup = 1, the U–interface transceiver will halt transmission and proceed to ANSI T1.601 defined “Tear Down” state H10 or J10, following three complete superframes. The deactivation sequence can be aborted if the Deactivate Request bit is set back to 0 prior to completion of three transmitted superframes. In NT mode, the Deactivate Request bit is set to a 1 by the external microcontroller in response to a received `dea` bit on the M4 channel, which indicates to the U–interface transceiver that this is a normal deactivation attempt. In this case, the MC145572 will reactivate in the warm start mode. In NT mode, the MC145572 automatically clears this bit upon deactivation. In LT mode, this bit is not cleared prior to starting the next activation and must be cleared when the MC145572 is deactivated.

Superframe Update Disable

This bit tells the Superframe Framer whether or not to update the maintenance bits M40 – M47, M50, M51, and M60, which are being transmitted with the new bits that have been loaded in the control registers. In normal operation, this bit is always set to 0, allowing the transmitted bits to be updated at the transmit superframe boundary with the maintenance channel data in registers BR0 and BR2(b7:b4). The exception to this is during a deactivation in the LT mode. The transceiver can be forced to send exactly three superframes of updated M4 channel data before it deactivates. In that sequence of operations, the Superframe Update Disable bit is first set to 1. The M4 maintenance bits are then written by the external microcontroller to the proper setting for deactivation. The Superframe Update Disable bit is set to a 0 and the Deactivate Request bit in NR2(b2) is set to a 1 by the external microcontroller. This guarantees that the U–interface transceiver will send exactly three superframes of updated M4 data before the activation state controller shuts everything down. Note that Superframe Update Disable does not affect the transmitted eoc, `febe`, or `crc` maintenance bits.

Customer Enable

When this bit is set to 1, it permits the U–interface transceiver to pass 2B+D data transparently. During the activation procedure, the Customer Enable bit normally is set to 0. Only after the U–interface transceiver has reached full–duplex operation and the `act` bits of the M4 maintenance channel have been properly exchanged, should the Customer Enable bit be set to a 1. See BR9(b5:b4), M4 Control Bits, for another way to achieve 2B+D data transparency.

4.3.4 NR3: Interrupt Status Register

This is the interrupt status register, and it is read–only. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset ($\overline{\text{RESET}}$). Each interrupt status bit in the register operates the same. If it is 1 and its corresponding interrupt enable is 1 in Register NR4, the $\overline{\text{IRQ}}$ pin on the chip will become active. $\overline{\text{IRQ3}}$ has the highest priority and $\overline{\text{IRQ0}}$ has the lowest.

	b3	b2	b1	b0
NR3	$\overline{\text{IRQ3}}$ ro	$\overline{\text{IRQ2}}$ ro	$\overline{\text{IRQ1}}$ ro	$\overline{\text{IRQ0}}$ ro

$\overline{\text{IRQ3}}$

This interrupt is set whenever there is a state change in NR1 and is cleared by reading NR1. If this bit is set by the D channel register interrupt, it is cleared once OR12 has been read, unless there has been a change in activation status.

$\overline{\text{IRQ2}}$

This interrupt is dedicated to the eoc. Whenever the eoc buffer, Register R6, is updated by the Superframe Deframer, this bit is set. The loading of the eoc buffer is dependent on its mode of operation. See Register BR9(b7:b6) for details of when the buffer is loaded. To clear the interrupt, it is necessary to read Register R6, the eoc buffer register. $\overline{\text{IRQ2}}$ is asserted at the end of the fourth and eighth basic frame of a superframe.

$\overline{\text{IRQ1}}$

This interrupt is dedicated to the received M4 maintenance bits. This bit is set whenever the M4 buffer, Register BR1, is updated. The updating of the M4 buffer is dependent on its mode of operation. See Register BR9(b5:b4) for details of when the buffer is updated. To clear the interrupt, it is necessary to read Register BR1, which is the M4 receive buffer. $\overline{\text{IRQ1}}$ is asserted at the end of every superframe.

$\overline{\text{IRQ0}}$

This interrupt is dedicated to the received M50, M51, and M60 bits from basic frames 1 and 2 that are buffered in Register BR3. Whenever these bits in Register BR3 are updated, this interrupt bit is set. The updating of BR3 is dependent on its mode of operation. See Register BR9(b3:b2) for details of when the buffer is updated. To clear the interrupt, it is necessary to read Register BR3. $\overline{\text{IRQ0}}$ is asserted at the end of the fourth received basic frame of a superframe.

4.3.5 NR4: Interrupt Mask Register

This is the interrupt mask register. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset ($\overline{\text{RESET}}$). Each bit operates in the the same manner. For example, if Enable $\overline{\text{IRQ1}}$ is set to 1 by the external microcontroller and the $\overline{\text{IRQ1}}$ interrupt bit is set to 1 in NR3, the $\overline{\text{IRQ}}$ pin becomes active when there is a change in activation status, or there is a D channel interrupt when D channel register OR12 is updated.

	b3	b2	b1	b0
NR4	Enable $\overline{\text{IRQ3}}$ rw	Enable $\overline{\text{IRQ2}}$ rw	Enable $\overline{\text{IRQ1}}$ rw	Enable $\overline{\text{IRQ0}}$ rw

4.3.6 NR5: IDL2 Data Control Register

This register contains controls for the IDL2 interface. More IDL2 controls are in Registers BR6, BR7, and OR0 – OR9. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset ($\overline{\text{RESET}}$). See Figures 4–4 and NO TAG in Register BR6 description for clarification regarding the precedence of the swap and blocking functions listed in this register.

CAUTION

Reserved bit b3 should be set to 0 at all times to maintain future compatibility.

	b3	b2	b1	b0
NR5	Reserved rw	Block B1 rw	Block B2 rw	Swap B1/B2 rw

Block B1

When this bit is 1 and the IDL2 Invert (BR7(b4)) is 0, the B1 channel is forced to transmit 1s on the IDL2 interface. When IDL2 Invert (BR7(b4)) is 1, 0s are transmitted in the B1 timeslot. Data received on the B1 channel from the IDL2 interface is still transmitted normally through the U–interface. The B1 designator on this bit always refers to the IDL2 interface. Therefore, even if bit Swap B1/B2 (NR5(b0)) is 1, data in the first B channel timeslot on the IDL2 interface is the data that is blocked.

Block B2

When this bit is 1 and the IDL2 Invert (BR7(b4)) is 0, the B1 channel is forced to transmit 1s on the IDL2 interface. When IDL2 Invert (BR7(b4)) is 1, 0s are transmitted in the B2 timeslot. Data received on the B2 channel from the IDL2 interface is still transmitted normally out of the U–interface. The B2 designator on this bit always refers to the IDL2 interface. Therefore, even if bit Swap B1/B2 (NR5(b0)) is 1, data in the second B channel timeslot on the IDL2 interface is the data that is blocked.

Swap B1/B2

When this bit is 1, the IDL2 interface performs a swap of the B channels from the U–interface to the IDL2 interface and from the IDL2 interface to the U–interface.

4.3.7 R6: eoc Data Register

This register is 12 bits long to match the length of the eoc message. Refer to Tables 4–5 and 4–6 to see how the eoc bits in this register map to the superframe. Operation of Register R6 depends on the setting of the eoc control bits in BR9(b7:b6) and BR14(b6). This register is double buffered for read and write operations.

In the default mode (BR14(b6)) is 0, R6 performs as a read–only/write–only register. Data that is read from R6 by the external microcontroller is the eoc message that the Superframe Deframer stores according to the eoc Control register (BR9(b7:b6)). Data that is written to R6 is stored in a latch contained in the Superframe Framer and is subsequently transmitted beginning on the next transmit eoc frame boundary. The Superframe Framer latches are set to 1s on hardware or software resets. The Superframe Update Disable register, NR2(b1), has no effect on this register.

	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1 ro/wo	eoc a2 ro/wo	eoc a3 ro/wo	eoc dm ro/wo	eoc i1 ro/wo	eoc i2 ro/wo	eoc i3 ro/wo	eoc i4 ro/wo	eoc i5 ro/wo	eoc i6 ro/wo	eoc i7 ro/wo	eoc i8 ro/wo

When BR14(b6) is set to 1, the Superframe Framer register that contains the transmit eoc message bits becomes a read/write register. Therefore, the data that is written to the Superframe Framer may be read back through R6. In this mode, the received eoc message is not available.

Table 4–5. Register Bit Locations Within the Superframe LT → NT

	Framing	2B+D	Overhead Bits (M1 – M6)					
QUAT Positions	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Basic Frame #	Sync Word	2B+D	M1	M2	M3	M4	M5	M6
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	dea	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	sco	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	1	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	uoa	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	aib	crc11	crc12

act = start up bit, set = 0 during start up
aib = alarm indication bit (set = 0 to indicate interruption)
crc = cyclic redundancy check: covers 2B + D + M4
dea = turn off bit (set = 0 to indicate turn off)
1 = reserved bit for future standard (set = 1)
sco = 0 start on command only
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
febe = far–end block error
uoa = U–only–activation

Table 4–6. Register Bit Locations Within the Superframe NT → LT

	Framing	2B+D	Overhead Bits (M1 – M6)					
QUAT Positions	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Basic Frame #	Sync Word	2B+D	M1	M2	M3	M4	M5	M6
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	ps1	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	ps2	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	ntm	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	cso	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	sai	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	nib	crc11	crc12

act = start up bit, set = 1 during start up
crc = cyclic redundancy check: covers 2B + D + M4
cso = cold start only (set = 1 for cold start only)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
febe = far–end block error
ntm = NT in test mode bit (set = 0 to indicate test mode)
ps1, ps2 = power status bits, (set = 0 to indicate power problems)
sai = S–activation indicator bit (optional, set = 1 for S/T activity)
nib = network indicator bit

4.4 BYTE REGISTERS

4.4.1 BR0: M4 Transmit Data Register

This register contains the M4 bits that are framed and sent by the Superframe Framer. The bits written to this register are sent out on the next transmit superframe boundary, if Superframe Update Disable (NR2(b1)) is set to 0. This register is double buffered. All bits are set to 1s following a Hardware Reset ($\overline{\text{RESET}}$) or Software Reset (NR0(b3)). This register is replaced by Register OR0 when BR10(b0) = 1.

CAUTION

BR0 should not be modified while device is in GCI mode. See OR6(b4).

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40 rw	M41 rw	M42 rw	M43 rw	M44 rw	M45 rw	M46 rw	M47 rw

Table 4–7 shows the definitions of the M4 bits as defined by ANSI T1.601–1992 for the Network to NT channel and the NT to Network channel.

Table 4–7. M4 Bit Definitions

M4 Bits	Network to NT	NT to Network
M40	act	act
M41	dea	ps1
M42	sco*	ps2
M43	1**	ntm
M44	1**	cso
M45	1**	1**
M46	[uoa]	[sai]
M47	[aib]	nib*

* These bits are defined in Bellcore document TR–NWT000397, Issue 3. When set to 0, the LT indicates to the NT that the network will deactivate the loop between calls.

** These bits are presently reserved by ANSI T1.601–1988 and should be set to 1s.

[ ] These are bit definitions for the revised ANSI T1.601–1992. In ANSI T1.601–1988 they were set to 1s.

4.4.2 BR1: M4 Receive Data Register

By reading this register, the external microcontroller obtains a buffered copy of the M4 bits that are parsed from the received superframe by the Superframe Deframer. The values in the register are valid when Superframe Sync (NR1(b1)) is 1. See Register BR9(b5:b4) for a description of when the "read" information is updated and when to write to this register. This register is double buffered. The receive M4 channel byte can be read at any time during the superframe prior to the next update. It is recommended that the MPU read this register as soon as possible after an interrupt. Note that BR14(b6) has no effect on the operation of this register. Bit 0 in Overlay register OR7 selects trinal checking on M4 act, dea, uoa, sai bits when set to 1. If trinal checking is desired for all bits, then it must be done in software. This register is replaced by Register OR1 when BR10(b0) = 1. When OR7(b0) is set, the M4 act, dea, uoa, sai bits must be the same for three superframes before they are updated in this register.

	b7	b6	b5	b4	b3	b2	b1	b0
BR1	M40 ro/wo	M41 ro/wo	M42 ro/wo	M43 ro/wo	M44 ro/wo	M45 ro/wo	M46 ro/wo	M47 ro/wo

4.4.3 BR2: M5/M6 Transmit Data Register

This register contains the reserved M5 and M6 bits that are sent by the Superframe Framer. The bits written to the register are sent out on the next transmit superframe boundary, if Superframe Update Disable (NR2(b1)) is set to 0. All bits are set to 1s following a Hardware Reset ($\overline{\text{RESET}}$) or Software Reset (NR0(b3)). See BR9(b1) for details concerning use of the far–end block error (`febe`) Input, b4. Bits b7, b6, and b5 are double buffered. When BR10(b0) = 1, this register is replaced by Register OR2.

CAUTION

Reserved bits b0, b1, b2, and b3 should be set to 0 at all times to maintain future compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR2	M50 rw	M60 rw	M51 rw	`febe` Input rw	Reserved rw	Reserved rw	Reserved rw	Reserved rw

ANSI T1.601–1992 presently reserves bits M50, M60, and M51. Therefore, these bits should be set to 1s for ISDN applications.

`febe` Input

The value in this bit is enabled to be transmitted as `febe` when BR9(b1) is set to 1.

4.4.4 BR3: M5/M6 Receive Data Register

This register contains the ANSI T1.601–1992 reserved M5 and M6 bits that are received by the Superframe Deframer, occurring in basic frames 1 and 2 of the superframe, and four other Superframe Deframer status bits. The M5 and M6 values in the register are valid when the Superframe Sync bit, NR1(b1), is 1. M50, M51, and M60 are updated, based on the mode set in Register BR9(b3:b2). Bits b7, b6, and b5 are double buffered. They can be read at any time during the superframe prior to the next update. It is recommended that this register be read as soon as possible after an M5/M6 channel interrupt. Refer to the description of BR9(b3:b2) for details concerning the operation of these three bits. When BR10(b0) = 1, this register is replaced by Register OR3.

	b7	b6	b5	b4	b3	b2	b1	b0
BR3	M50 ro/wo	M60 ro/wo	M51 ro/wo	Received `febe` ro	Computed `febe` ro	Verified `act` ro	Verified `dea` ro	Super-frame Detect ro

Received `febe`

This is the state of the received `febe` bit in the last complete received superframe. It is updated at the end of each received superframe when Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s.

Computed nebe

This is the state of the cyclic redundancy check (`crc`) check from the last complete received superframe. It is updated at the end of each received superframe. This bit is 0 when a `crc` error is detected. Also, when either Superframe Sync (NR1(b1)) or Linkup (NR1(b3)) is 0, this computed near–end block error (`nebe`) bit is forced to 0.

Verified `act`

This is the dual–consecutively checked setting of the `act` bit in the received superframe. Dual–consecutive checking requires that the received bit be in the same state for two consecutive superframes. Whenever the U–interface transceiver detects a transition from 0 to 1 on Superframe Sync, NR1(b1), Verified `act` is set to 0. It remains in its current state until both Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are 1s. Then, if the received `act` bit is 1 for two consecutive superframes, Verified `act` becomes a 1. After Verified `act` becomes a 1, it changes to 0 if the received `act` bit is received as

a 0 for two consecutive superframes. This bit is updated at the end of the first frame of each superframe and is provided in this register for status only. See BR9(b5:b4) for more information regarding this bit. When OR7(b0) is set, the M4 act and dea bits must be valid for three superframes before Verified act or Verified dea are updated.

Verified dea

This is the dual–consecutively checked, inverted setting of the dea bit, in the received superframe. Since the dea bit can only be received by an NT, this bit can only be 1 in the LT mode. Dual–consecutive checking requires that the received bit is in the same state for two consecutive superframes. Whenever the U–interface transceiver detects a transition from 0 to 1 on Superframe Sync in NR1(b1), Verified dea is set to 0. It remains in its current state until both Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are 1s. Then, if the received dea bit is 0 for two consecutive superframes, Verified dea will become 1. After Verified dea becomes 1, if the received dea bit is ever 1 for two consecutive superframes, then Verified dea will become a 0. This bit is updated at the end of the second basic frame of each superframe and is provided in this register for status only. See BR9(b5:b4) for more information regarding this bit. When OR7(b0) is set, the M4 dea bit must be valid for three superframes before Verified dea is updated.

Superframe Detect

This is the unmodified output of the Superframe Deframer's superframe detection circuit. It is primarily intended for diagnostic purposes.

4.4.5 BR4: febe Counter

This register contains the current febe count. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the febe bit is active in a superframe, the counter will increment at the end of the received superframe. The counter will not increment unless Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s. If OR7(b1) is set, then the febe counter will roll over from $FF to $00. The user software must take into account that if OR7(b1) is set, the counter value read from BR4 might be less than the previous value, which means that the counter has rolled over. The default setting for OR7(b1), after any hardware or software reset, produces the same operation as the MC145472/MC14LC5472. This register is replaced by Register OR4 when BR10(b0) = 1. When OR7(b1) is cleared, BR4 counts to $FF and does not roll over. This is the default configuration after any reset to maintain MC145472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR4	febe Counter 7 rw	febe Counter 6 rw	febe Counter 5 rw	febe Counter 4 rw	febe Counter 3 rw	febe Counter 2 rw	febe Counter 1 rw	febe Counter 0 rw

4.4.6 BR5: nebe Counter

This register contains the current nebe count. A nebe occurs whenever the received crc message does not match the computed crc or when Linkup (NR1(b3)) is 1 and Superframe Sync (NR1(b1)) is 0. The Superframe Framer maintains the superframe timing to increment the nebe counter when Superframe Sync is 0. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it.

When the Superframe Deframer detects a crc error in the received superframe, the counter is incremented at the end of that superframe. When OR7(b1) is set, then the febe counter rolls over from $FF to $00. The user software must take into account that if OR7(b1) is set, the counter value read from BR5 might be less than the previous value, which means that the counter has rolled over. The default setting for OR7(b1), after any hardware or software reset, produces the same operation as the MC145472/MC14LC5472. When BR10(b0) = 1, this register is replaced by Register OR5. When

OR7(b1) is cleared, BR5 counts to $FF and does not roll over. This is the default configuration after any reset to maintain MC145472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR5	nebe Counter 7 rw	nebe Counter 6 rw	nebe Counter 5 rw	nebe Counter 4 rw	nebe Counter 3 rw	nebe Counter 2 rw	nebe Counter 1 rw	nebe Counter 0 rw

4.4.7 BR6: Loopback Control Register

This register contains the loopback controls. For normal (no loopback) operation, bits b7:b5 and b3:b1 of BR6 should be 0. BR6 is cleared by a Software Reset (NR0(b3)), Hardware Reset ($\overline{\text{RESET}}$), or when the Return to Normal bit (NR0(b0)) is set. When a bit is set to 1, the appropriate loopback is enabled. This register is replaced by Register OR6 when BR10(b0) = 1.

Bits b7 through b4, inclusive, are not set when the MC145572 is operating in the automatic eoc mode.

	b7	b6	b5	b4	b3	b2	b1	b0
BR6	U–Loop B1 rw	U–Loop B2 rw	U–Loop 2B + D rw	U–Loop Trans–parent rw	IDL–Loop B1 rw	IDL–Loop B2 rw	IDL–Loop 2B + D rw	IDL–Loop Trans–parent rw

U–Loop B1

This bit selects a loopback on the B1 channel toward the U–interface.

U–Loop B2

This bit selects a loopback on the B2 channel toward the U–interface.

U–Loop 2B+D

This bit selects a loopback on the B1, B2, and D channels toward the U–interface.

U–Loop Transparent

This bit selects whether the loopback toward the U–interface should be handled transparently or not. This transparency selection applies to all channels that are selected for loopback to the U–interface.

IDL2–Loop B1

This bit selects a loopback on the B1 channel toward the IDL2 interface. This bit operates in all IDL2 and GCI modes.

IDL2–Loop B2

This bit selects a loopback on the B2 channel toward the IDL2 interface. This bit operates in all IDL2 and GCI modes.

IDL2–Loop 2B+D

This bit selects a loopback on the B1, B2, and D channels toward the IDL2 interface. When this bit is set to 1, the IDL2–loop B1 and IDL2–loop B2 bits are ignored. This bit operates in all IDL2 and GCI modes.

IDL2–Loop Transparent

This bit selects whether the loopback toward the IDL2 interface should be handled transparently or not. This transparency selection applies to all channels that are selected for loopback to the IDL2 interface.

Figures 4–1 and 4–2 may be used to determine the combined effect of setting more than one loopback control in BR6, as well as the bits in NR5 and BR7. Only details for the B1 channel are shown, but a similar set of logic applies to both the B2 and D channels. D_{out} and D_{in} refer to the two external pins on the device. There are two control signals shown in Figure 4–2 that do not come from MC145572 registers. Link Active is an internal signal that is asserted when the ANSI T1.601–1992 defined activation sequence reaches SN3/SL3 and Customer Enable (NR2(b0)) is set, or Verified `act` (BR3(b2)) is set. Link Good is asserted whenever the ANSI T1.601–1992 defined activation sequence is completed successfully and the internally monitored receive error rate is adequate for passing data.

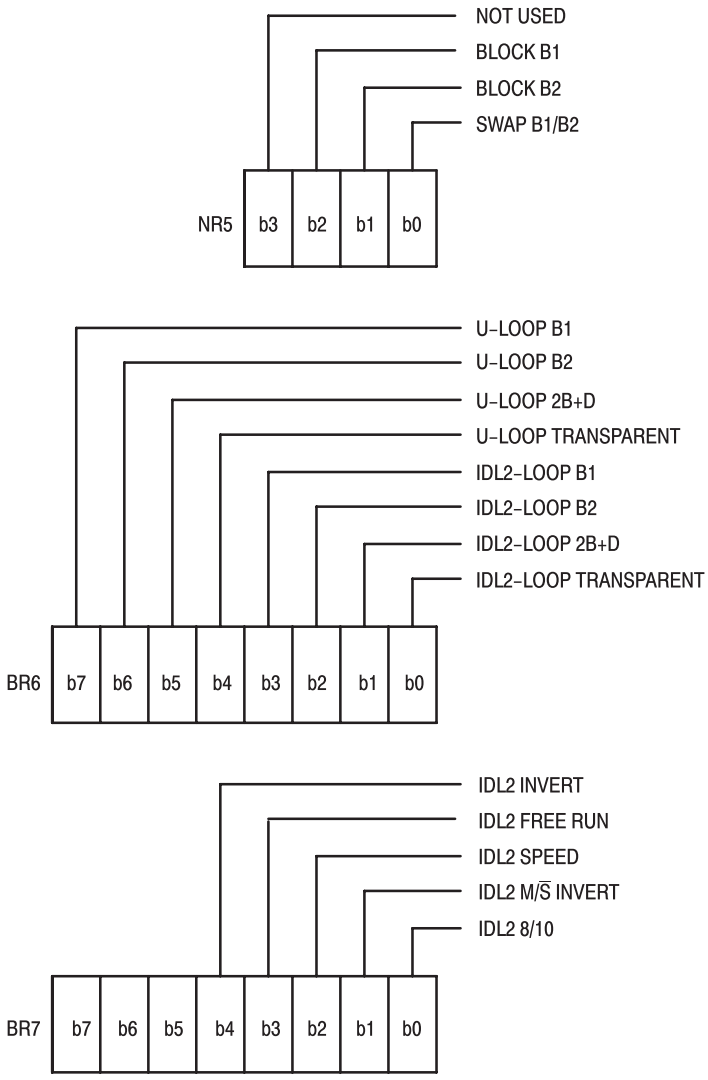


Figure 4–1. IDL2 Interface Loopback Control Bits

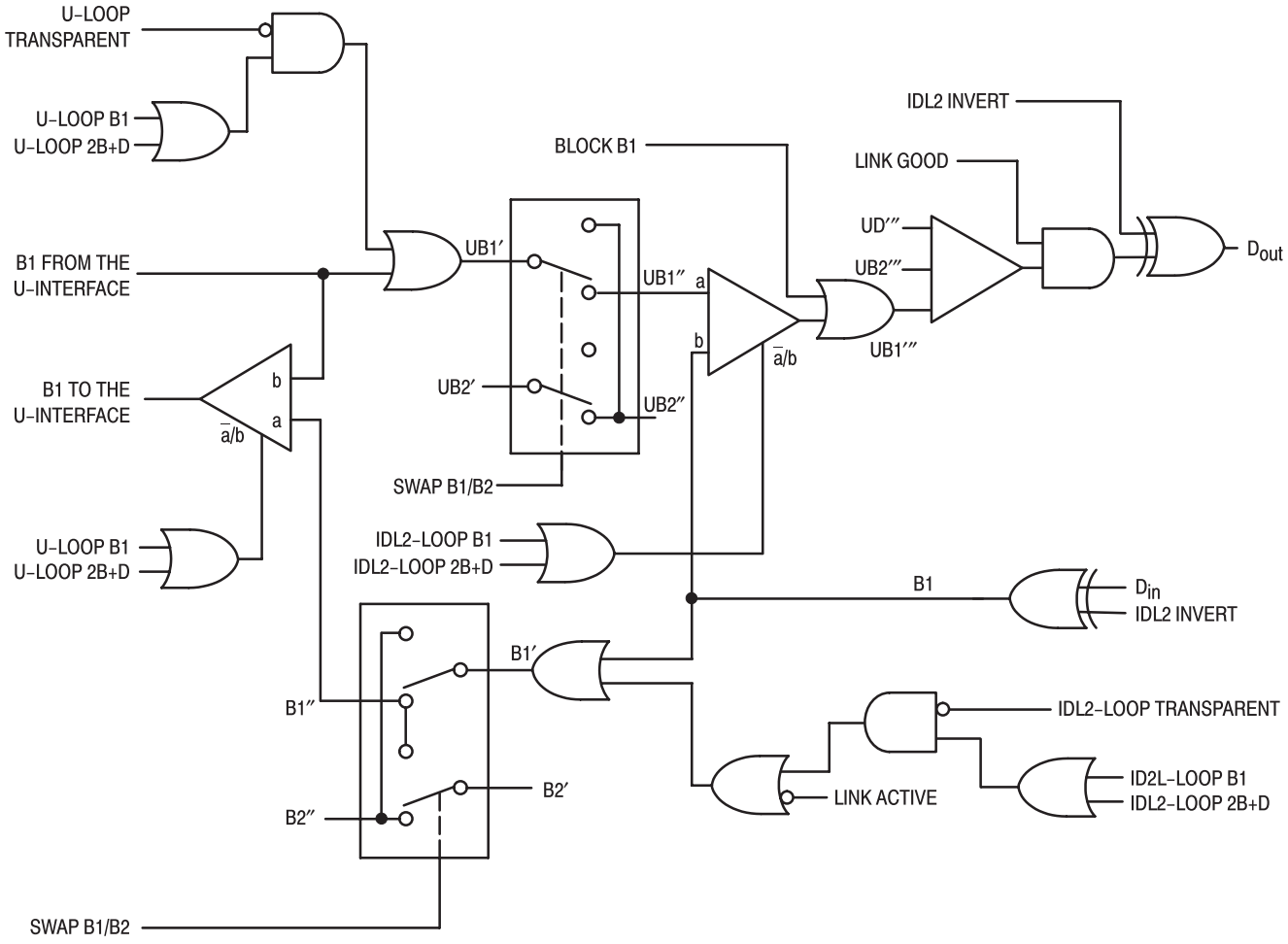


Figure 4–2. IDL2 Interface Loopback Logic Diagram

4.4.8 BR7: IDL2 Configuration Register

This register contains IDL2 interface mode information. BR7 is cleared on Hardware Reset ($\overline{\text{RESET}}$) or Software Reset (NR0(b3)). All bits in this register are read/write. This register is replaced by Register OR7 when BR10(b0) = 1.

	b7	b6	b5	b4	b3	b2	b1	b0
BR7	BR15A Select rw	OUT2 wo GCI IN2 ro	OUT1 wo GCI IN1 ro	IDL2 Invert rw	IDL2 Free Run rw	IDL2 Speed rw	IDL2 M/$\overline{\text{S}}$ Invert rw	IDL2 8/10 rw

BR15A Select

When set to 1, this bit causes Register BR15A to be substituted for Register BR15 in the SCP register map. After any reset, this bit is cleared to 0.

GCI IN2/OUT2

This is a read–only/write–only bit. The write–only portion, OUT2, is cleared by hardware and software resets. In full GCI mode, entered by holding the pin MCU/$\overline{\text{GCI}}$ low, the state of OUT2 is driven onto a GCI mode dedicated output pin. However, if the GCI C/I channel decodes the input command DISS to the MC145572, this same pin is forced high. When read (again, provided the MC145572 is in full GCI mode), bit IN2 reflects the state of a GCI mode dedicated input pin. These pins may be used for any purpose in a GCI application. See Chapter 3, ***Device Description***, for more information. GCI command LTD2 when active in LT mode or NTD2 when active in NT mode, sets OUT2 high.

GCI IN1/OUT1

This is a read–only/write–only bit. The write only portion, OUT1, is cleared by hardware and software resets. In full GCI mode, entered by holding the pin MCU/$\overline{GCI}$ low, the state of OUT1 is driven onto a GCI mode dedicated output pin. When read (again, provided the MC145572 is in full GCI mode), bit IN1 reflects the state of a GCI mode dedicated input pin. These pins may be used for any purpose in a GCI application. See Chapter 3, ***Device Description***, for more information. GCI command LTD1 when active in LT mode or NTD1 when active in NT mode, sets OUT1 high.

IDL2 Invert

When set to 1, this bit forces the IDL2 interface to invert every bit just before it is transmitted on the D_{out} pin and invert every bit that is received on D_{in}.

IDL2 Free Run

When set to 0, this bit forces the DCL and FSR/FSX outputs to run continuously when in the IDL2 Master mode. When this bit is 1, the DCL and FSR/FSX stop when the U–interface transceiver is deactivated. DCL and FSR/FSX will start operating when Superframe Sync in NR1(b1) becomes 1 and halts when the U–interface transceiver enters the ANSI T1.601 defined “Tear Down” state.

IDL2 Speed

This bit selects the DCL clock speed in the IDL2 Master mode. When this bit is 0, the clock rate is 2.56 MHz. A 1 selects a rate of 2.048 MHz. This bit also sets the output clock rate for FREQREF or $FREF_{out}$ when in NT Slave mode. Also, see the description for OR7(b4).

IDL2 M/S Invert

When this bit is 1, it inverts the polarity of the IDL2 Master/Slave pin. When this bit is 0 and IDL2 Master is set high, the U–interface transceiver operates in the IDL2 Master mode.

IDL2 8/10

This bit reorders the sequence of 2B+D data presented in the IDL2 data transfer. The two possible transfer sequences are shown in Figures 4–3 and 4–4. A 1 selects the 8–bit mode and a 0 selects the 10–bit mode. In the 8–bit mode, the two B channels are provided sequentially, followed by the two D channel bits. In the 10–bit mode, one D channel bit follows each B channel byte. The ability to swap the B channels, (NR5(b0)), applies to both of these modes. For further information about the IDL2 interface, see **Section 5.4**.

NOTE

If timeslot assignment mode is enabled via OR6 b(7), b(6), or b(5), then the IDL2 8/10 control bit is ignored and B channel and D channel data is placed according to OR0 – OR5.

If GCI electrical mode is selected by setting OR6(b3) to a 1, the IDL2 interface transfers only 2B+D data in the GCI timeslot locations as programmed in OR5(b2:b0).

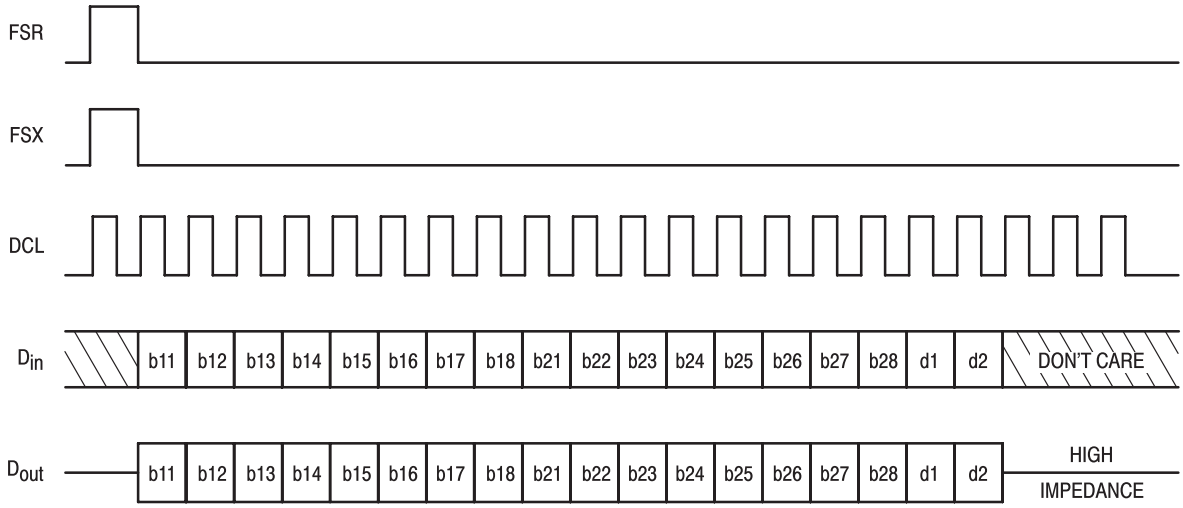


Figure 4–3. IDL2 Interface Timing in 8–Bit Master Mode

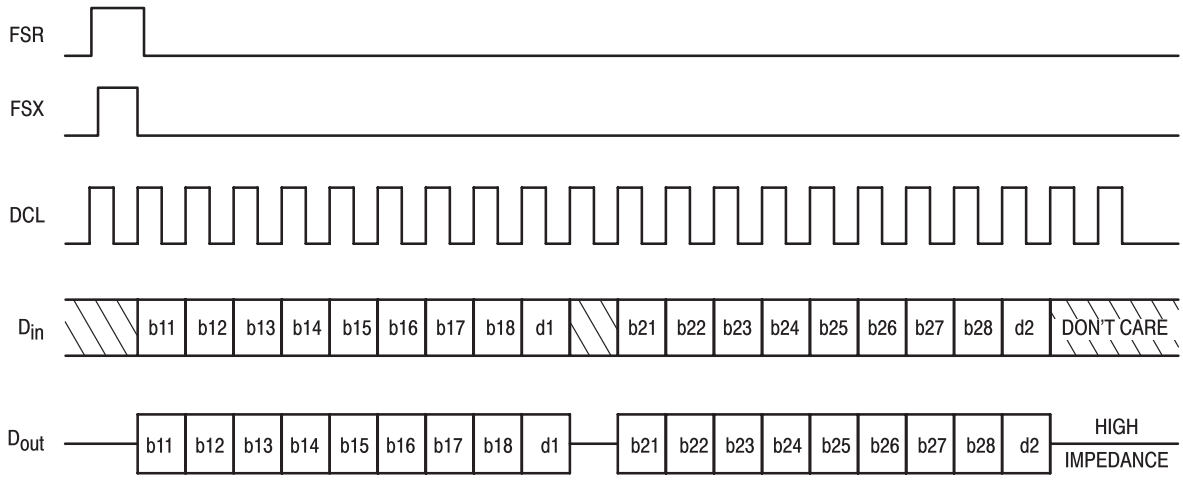


Figure 4–4. IDL2 Interface Timing in 10–Bit Master Mode

4.4.9 BR8: Transmit Framer and Mode Control Register

This register contains controls used for test operations such as external loopbacks, Superframe Framer Control and State information, and NT/$\overline{\text{LT}}$ mode control. All write capable bits are cleared on a Software Reset (NR0(b3)) or Hardware Reset ($\overline{\text{RESET}}$). Bits b7 – b4 and b0, are read–only/write–only. To read the write–only bits, it is necessary to set BR14(b6) to 1. When BR10(b0) = 1, this register is replaced by Register OR8.

	b7	b6	b5	b4	b3	b2	b1	b0
BR8	Frame Steering wo	Frame Control 2 wo	Frame Control 1 wo	Frame Control 0 wo	crc Corrupt rw	Match Scrambler rw	Receive Window Disable rw	NT/$\overline{\text{LT}}$ Invert wo
	Frame State 3 ro	Frame State 2 ro	Frame State 1 ro	Frame State 0 ro	Reserved	Reserved	Reserved	NT/$\overline{\text{LT}}$ Mode ro

Frame Steering
When this bit is a 1, the Frame Control 2:0 bits take over control of the Superframe Framer's mode of operation.

Frame Control 2:0
These bits set the mode of operation for the Superframe Framer when the Frame Steering bit is 1. Table 4–8 shows the mode the Superframe Framer will go into, based on the three Frame Control bits and the Frame Steering bit.

Table 4–8. Frame Control Modes

Frame Steering	Frame Control 2:0			Superframe Framer Mode of Operation	
b7	b6	b5	b4	NT	LT
1	0	0	0	SN0	SL0
1	0	0	1	Six frames of 10 kHz tone followed by SN1	SL1
1	0	1	0	SN2	SL2
1	0	1	1	SN3	SL3
1	1	0	0	10 kHz tone	
1	1	0	1	40 kHz tone	
1	1	1	0	Generates a single quat every basic frame which alternates over all four of the 2B1Q symbols.	
1	1	1	1	Superframe Framer free runs the scrambler with no synchronization words.	
0	Don't Care			The Superframe Framer output is determined by the state of the Automatic Activation Controller.	

Frame State 3:0
These bits provide the external microcontroller with the current state of the U–interface transceiver's Superframe Framer, regardless of whether the Superframe Framer is being controlled by the external microcontroller or internally by the Automatic Activation Controller. The meaning of Frame State 2:0 maps directly onto the meaning of Frame Control 2:0. Frame State 3 is 0 at all times, except during TN of an NT activation sequence. State transitions are always made on frame or superframe boundaries.

crc Corrupt
When set to 1, this bit forces the transmitted crc to be inverted. It is used for eoc maintenance procedures and to force an outgoing corrupt crc in digital loop carrier systems. As the transmit framer

transmits the crc and this bit is set, the transmitted crc is inverted. This bit can be cleared or set at any time during transmission of a superframe. This bit functions the same as in the MC145472/ MC14LC5472 after a Hardware Reset ($\overline{\text{RESET}}$). When OR7(b2) is set to 1, the operation of this bit is modified so that the outgoing crc is only corrupted on the current superframe.

Match Scrambler
When set to 1, this bit forces the descrambler and scrambler polynomials to match. This is used for external analog loopback and framer–to–deframer loopback.

Receive Window Disable
When set to 1, this bit disables the search window placed around the received synchronization word in the LT mode. When the receive window is disabled, the LT will synchronize to an incoming synchronization word that is located at any arbitrary point with respect to its transmitted synchronization word. This allows the U–interface transceiver to use its own transmitted synchronization word for frame detection when operated in external analog loopback mode and framer–to–deframer loopback.

NT/$\overline{\text{LT}}$ Invert
This bit allows override control of the setting of the NT or LT operation of the U–interface transceiver's external NT/$\overline{\text{LT}}$ mode pin. If this bit is 0 and the NT/$\overline{\text{LT}}$ pin is high, the device is in NT mode. When this bit is then set to 1, the device will then be in the LT mode.

NT/$\overline{\text{LT}}$ Mode
This read–only bit reflects the current mode of the device. If 1, the U–interface transceiver is operating in the NT mode.

4.4.10 BR9: Maintenance Channel Configuration Register

This register contains mode control over the deframer's updating of the received maintenance bits. The register is cleared on Software Reset (NR0(b3)) or Hardware Reset ($\overline{\text{RESET}}$). When BR10(b0) = 1 this register is replaced by Register OR9.

CAUTION

See **Appendix C** for printed circuit board layout recommendations.

	b7	b6	b5	b4	b3	b2	b1	b0
BR9	eoc Control 1 rw	eoc Control 0 rw	M4 Control 1 rw	M4 Control 0 rw	M5/M6 Control 1 rw	M5/M6 Control 0 rw	febe/ nebe Control rw	Reserved

eoc Control 1:0
These bits control the eoc handling capability of the U–interface transceiver. Table 4–9 gives a brief description of each mode selected by the eoc Control bits. The eoc Trinal–Check mode (b7,b6 = 1,0) and the Automatic eoc Processor mode (b7,b6 = 0, "Don't Care") are described in the paragraphs following Table 4–9. The default mode setting is 0,0; thereby selecting the Automatic eoc Processor. Regardless of the operating mode, every time R6 is loaded by the deframer, $\overline{\text{IRQ2}}$ (NR3(b2)) is set to 1. Use the update on every frame mode (b7,b6 = 1,1) for digital loop carrier or proprietary applications.

Table 4–9. eoc Control Modes

eoc Control 1:0		eoc Function Description
b7	b6	
1	1	Update eoc register (R6) on every eoc frame (twice during each superframe). Recommended for Digital Loop Carrier applications.
1	0	Update eoc register (R6) after passing a trinal–check.
0	Don't Care	Update eoc register (R6) after passing a trinal–check and also invoke Automatic eoc Processor to operate when in NT mode.

eoc Trinal–Check Mode (b7, b6 = 1,0)

The eoc Trinal–Check operation checks for three identical consecutive eoc messages being received before loading the eoc message into R6. Register R6 is always updated with the received message when the third identical consecutive message is received.

In Trinal–Check mode when operating as an LT, the trinal–check is automatically restarted whenever a new message is written to the Superframe Framer's R6 register for transmission. The eoc Trinal–Check is reset whenever the Linkup (NR1(b3)) or Superframe Sync (NR1(b1)) bits are 0.

When operating as an NT in Trinal–Check mode, received eoc messages are automatically transmitted back by the Superframe Framer if the address is either the NT1 or broadcast address. This continues until three valid consecutive identical messages have been received. If the eoc address in the received eoc message is not 0 or 7, the Hold message is substituted and automatically transmitted back to the LT. Once three valid consecutive identical messages have been received, the deframer updates Register R6. Once R6 has been updated with the received message, the Superframe Framer's Register R6 (written to by a SCP interface operation) is transmitted. It is up to the microcontroller firmware to handle the eoc message and place a response into R6 before the U–chip sends the next eoc frame out to the LT (see Figure 4–2). Register R6 will be repeated throughout all subsequent eoc frames until it is altered by another CPI interface write to it, or the received eoc message changes.

Automatic eoc Processor Mode (b7 = 0, b6 = Don't Care)

An Automatic eoc Processor is provided in the NT mode. This processor operates the eoc in accordance with ANSI T1.601–1992. The processor recognizes eoc messages addressed to either the NT1 or the broadcast address. The processor decodes the messages in Table 4–10 and then takes the action indicated. If a properly addressed message is received that is not listed in the table, the "Unable to Comply" message is transmitted in response. If an improperly addressed message is received, the "Hold State" message is transmitted with the NT1 address. Whenever operating in this mode, the eoc Trinal–Check operation continues to function and R6 will be loaded with the eoc message that the Automatic eoc Processor decodes. Note that because the Automatic eoc Processor is an NT mode only function, selecting mode 0,0 in the LT mode is equivalent to mode 1,0.

Regardless of eoc mode, Register R6 will not be altered while Superframe Detect (BR3(b0)) is a 0. When the automatic eoc mode is enabled, bits in BR6 are not set when loopback messages are received.

Table 4–10. Automatic eoc Processor Functions

eoc Message	Automatic eoc Processor Response
Operate 2B + D Loopback	Invokes a loopback to the U–interface at the IDL interface of the B1, B2, and D channels. Transparency will be determined by the setting of BR6(b4), U–loop transparent.
Operate B1 Channel Loopback	Invokes a loopback to the U–interface at the IDL interface of the B1 channel. The loopback is transparent.
Operate B2 Channel Loopback	Invokes a loopback to the U–interface at the IDL interface of the B2 channel. The loopback is transparent.
Request Corrupted `crc`	Equivalent to setting BR8(b3) to a 1.
Notify of Corrupted `crc`	None.
Return to Normal	Resets all of the previously invoked eoc functions.
Hold State	Maintains previously invoked eoc functions.

M4 Control 1:0

These bits control the M4 handling capability of the U–interface transceiver. The default mode setting is b5, b4 = 0,0. In all of the modes, BR1 will not be loaded and an $\overline{\text{IRQ1}}$ (NR3(b1)) will not be issued unless both Linkup (NR1(b3)) and Superframe Sync (NR1(b1)) are 1s. When OR7(b0) is set to 1; `uoa`, `act`, `sai`, and `dea` bits in the M4 channel are trinal–checked. See Table 4–11.

Table 4–11. M4 Control Modes

OR7	BR9 M4 Control 1:0		M4 Function Description
	b5	b4	
0	0	0	M4 Dual Consecutive mode. In addition, the Verified act (BR3(b2)) and Verified dea (BR3(b1)) operations are enabled in this mode only.
0	0	1	M4 Dual Consecutive mode.
0	1	0	Delta mode.
0	1	1	Every mode.
1	X	X	M4 channel bits M40 (act), M41 (dea), and M46 (uoa, sai) are trinal–checked. Remaining bits operate per BR9(b5,b4) settings. Verified act and Verified dea available on trinal–checked act, dea bits when b5:b4 = 0,0.

M4 Dual Consecutive Modes (b5, b4 = 0,0 or 0,1)

The M4 Dual Consecutive modes perform a simple algorithm on the received M4 bits, and only interrupt the external microcontroller when an M4 bit has changed state and has remained in the new state for two consecutive superframes. The M4 bit values read from BR1 in this mode are only the most recent values that have been the same for two consecutive superframes. Referring to Table 4–12, suppose, for example, that for several superframes the M4 bits have been all 0s, as shown in the column labeled “Received M4 Byte”. If the external microcontroller read BR1, it would read all 0s as shown in the column labeled “BR1 Contents”. Now, notice in the subsequent superframes 2 and 3 that the received M4 bits that do not hold their state for at least two consecutive superframes, do not cause an interrupt and do not show up in BR1.

Table 4–12. M4 Dual Consecutive Modes Example

Superframe	Received M4 Byte	BR1 Contents	Action
1	0000 0000	0000 0000	—
2	1000 0001	0000 0000	—
3	0001 0001	0000 0001	$\overline{\text{IRQ1}}$ is set

At start–up, there is no history of what has been received in the M4 bits. Therefore, the technique for the initial setting for BR1 is as follows: a hardware or software reset sets BR1 to all 0s. However, at the user’s discretion, while either Linkup (NR1(b3)) or Superframe Sync (NR1(b1)) is 0, the user may write to BR1 and set the initial value. In this way, the external microcontroller may assume a current state for the M4 bits, and then wait for an $\overline{\text{IRQ1}}$ to inform it of a change in state. Also, any time that Superframe Sync is lost and then regained, the initial programmed value is reloaded into BR1.

The default M4 Dual Consecutive mode (b5, b4 = 0,0) has the additional feature of performing automatic detection of the act and dea bits. Verified act (BR3(b2)) and Verified dea ((BR3(b1)) are dual consecutive checked values of M40 and M41. Verified act is valid for both NT and LT modes. Verified dea operates in the NT mode only. Whenever there is a 0 to 1 transition on Superframe Sync (NR1(b1)), Verified act and Verified dea are reset. If M40 is received as 1 for two consecutive superframes, Verified act is set to 1. Similarly, if M40 is received as 0 for two consecutive superframes, Verified act is set to 0. When this mode is selected, the logical OR of Verified act and the Customer Enable bit in NR2(b0) permits customer data transparency without any action taken by the external microcontroller. In NT mode, if M41 is received for two consecutive superframes as 0, Verified dea is set to 1. Similarly, if M41 is received as 1 for two consecutive superframes, Verified dea will return to 0. When this mode is selected, the logical OR of Verified dea and the Deactivate Request bit in NR2(b2) allows the U–interface transceiver to respond to the far–end transceiver’s intention to deactivate without requiring any interaction by the external microcontroller. Note that the state of Verified act and Verified dea may be monitored by the external microcontroller through BR3(b2:b1).

M4 Delta Mode (b5, b4 = 1,0)

The Delta mode compares the M4 data from the previous superframe against the current received superframe M4 data. If there is a difference in at least one bit, BR1 is updated and an $\overline{\text{IRQ1}}$ interrupt is issued. Note that in this mode, BR1 always contains a copy of the latest received M4 byte from the previous superframe.

M4 Every Mode (b5, b4 = 1,1)

The Every mode stores each received superframe of M4 data in BR1 and issues an interrupt at the end of every received superframe.

Note that regardless of the mode of operation, BR1 will not be altered while Superframe Sync (NR1(b1)) is 0.

M4 Trinal–Check Mode

The M4 `act`, `dea`, `sai`, and `uoa` bits can be configured for trinal–check operation by setting OR7(b0) to a 1. See **Section 4.5.8** for more detail.

M5/M6 Control 1:0

These bits control the M5/M6 handling capability of the U–interface transceiver. The default mode setting is b3, b2 = 0,0, which selects the Dual Consecutive mode. These controls are identical in operation to the M4 mode control functions, except that they apply to M50, M51, and M60. Refer to the M4 Control mode paragraphs above for a description of the M5/M6 Control modes. The M5/M6 interrupt, $\overline{\text{IRQ0}}$ (NR3(b0)), occurs in the middle of the superframe when basic frame 4 has been completely received.

Table 4–13. M5/M6 Control Modes

M5/M6 Control 1:0		M5/M6 Function Description
b3	b2	
0	Don't Care	M5/M6 Dual Consecutive mode.
1	0	Delta mode.
1	1	Every mode.

`febe`/`nebe` Control

This bit controls how the transmitted `febe` is computed. If this bit is 0, the transmitted `febe` is set active if either the Computed `nebe` (BR3(b3)) is active or the `febe` input (BR2(b4)) is set active. If this control bit is set to 1, the transmitted `febe` is set to whatever is set in the `febe` input (BR2(b4)).

NOTE

Regarding `febe` and `nebe`, "active" means they are set to 0.

4.4.11 BR10: Overlay Select Register

This register is used to enable access to the overlay register set of the MC145572. To maintain future compatibility, the reserved bits must be written as 0s.

	b7	b6	b5	b4	b3	b2	b1	b0
BR10	Reserved	Reserved	Reserved	Reserved	Reserved	Select Dump Access rw	Select DCH Access rw	Select Overlay rw

Select Dump Access

This bit hides the normal byte register BR13, and the register becomes a byte–wide access port, OR13, to the dump/restore mechanism of the U–chip. Two more bits in the overlay registers control the operating mode of the dump/restore mechanism. See Overlay register OR8. This bit is reset by hardware reset only.

Select DCH Access

This bit hides the normal byte register, BR12, and the register becomes an 8–bit read–only/write–only register, OR12, and provides access to the D channel. When this bit is asserted, D channel input data present on the pin interfaces of the MC145572 is ignored and D_{out} is high impedance. Instead, the D channel is sourced strictly from this register. D channel data received from the U–interface maintains correct byte alignment relative to the U–interface basic frame boundary on the pin interfaces, and is readable through the overlay register, OR12, eight bits at a time. $\overline{IRQ3}$ is used to indicate when every new eight bits of data are received, in addition to indicating a change in receive status.

A special code (1111) is loaded in Nibble register NR1, to indicate that the source of the interrupt is the D channel access register. Both transmit and receive of the D channel data is aligned respective to the transmit and receive superframes. When selected, the D channel access register has the highest priority over other possible routes (e.g., the IDL2 interface and the D channel port), for the D channel data. This bit is reset by hardware reset only. Software should read and write this register at the time the D channel interrupt occurs.

Enabling OR12 access, enables the D channel interrupt onto $\overline{IRQ3}$. The interrupt must still be enabled via $\overline{IRQ3}$ Enable in NR4 for the $\overline{IRQ}$ pin to become active. Upon receipt of the interrupt, the external controller must read the interrupt status in NR3 to determine that it is an $\overline{IRQ3}$. The controller must then read NR1, where it would find the code 1111, indicating the actual source is a D channel interrupt.

NOTE

If DCH Access mode is used in conjunction with timeslot assignment, the D channel timeslot must not be timeslot 0 in order to maintain synchronization with the transmit superframe. This is especially true in LT mode when SFAX is used as an input.

Select Overlay

This bit hides the normal byte registers BR0 – BR9, and the registers become the overlay registers OR0 – OR9. In general, the overlay registers contain device information that needs to be set only once following reset, such as the timeslot information or during some test mode. This bit is reset by hardware reset only.

4.4.12 BR11: Activation State Register

This register contains activation state and control data. All the bits are cleared on Hardware Reset ($\overline{RESET}$) and Software Reset (NR0(b3)). The register is a read–only/write–only register. Setting BR14(b6) to 1 permits the external microcontroller to read back the write portion of the register.

	b7	b6	b5	b4	b3	b2	b1	b0
BR11	Activation Control 6 wo	Activation Control 5 wo	Activation Control 4 wo	Activation Control 3 wo	Activation Control 2 wo	Activation Control 1 wo	Activation Control 0 wo	Activation Timer Disable wo
	Activation State 6 ro	Activation State 5 ro	Activation State 4 ro	Activation State 3 ro	Activation State 2 ro	Activation State 1 ro	Activation State 0 ro	Activation Timer Expire ro

Activation Control 6:0

These write–only bits allow the external microcontroller to set a new activation state for the U–interface transceiver to execute. The transition to this state is controlled by BR12. Use of this register is not required for normal operation.

Activation Timer Disable

When this write–only bit is 0, the activation timer operates normally. During activation the timer will time for approximately 15 seconds, and then the Activation Timer Expire bit will become 1, and the activation state machine will react to the time–out. When this bit is set to 1, the activation timer is disabled and the Activation Timer Expire will always read back as 0.

Activation State 6:0

These read–only bits contain the current state of the internal activation controller. Activation State 6, BR11(b7) indicates cold start mode when it is 0 and indicates warm start mode when it is 1.

Activation Timer Expire

This bit shows the status of the activation timer. A 1 indicates that the activation timer has expired.

4.4.13 BR12: Activation State Test Register

This register is read–only/write–only. The write only portion controls the U–interface transceiver's internal CPU and activation controller. The read portion contains the eight most significant bits of the Error Power Indicator (EPI) register in the CPU. By setting BR14(b6) to 1, the external microcontroller can read back the setting of the control bits. These bits are cleared on a Hardware Reset ($\overline{\text{RESET}}$) or Software Reset (NR0(b3)). This register is replaced by OR12 when BR10(b1) = 1.

CAUTION

Reserved bit b1 should be set to 0 at all times to maintain future compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR12	Activation Control Register wo	Interpolate Enable wo	Load Activation State wo	Step Activation State wo	Hold Activation State wo	Big Jump Select wo	Reserved wo	Force Linkup wo
	EPI 18 ro	EPI 17 ro	EPI 16 ro	EPI 15 ro	EPI 14 ro	EPI 13 ro	EPI 12 ro	EPI 11 ro

Activation Control Steer

When this bit is 0, the internal CPU of the MC145572 has total control of its peripherals, and has them perform a normal activation procedure. However, when this bit is set to 1, the internal CPU and its peripherals are directed to use the control information provided in the Interpolate Enable bit in this register (b6), BR13, BR15A(b7), and BR15A(b6).

Interpolate Enable

This bit is active only when the Activation Control Steer bit (b7) is set to 1. The timing interpolator is enabled when this bit is 1 and the transceiver is operating in LT mode. The timing interpolator is disabled when this bit is 0 and the transceiver is operating in LT mode.

Load Activation State

When this bit is set to 1, Activation Control 6:0 is loaded into the activation controller as the new state. The load is performed at a time that does not adversely affect the operation of the CPU, and will take place within 1 baud of setting this bit to 1. To load an activation state, this bit must initially be 0. The desired state should then be loaded into BR11 and this bit should be set to 1. Loading overrides the setting of the Hold Activation State bit (b3).

Step Activation State

When this bit is set to 1, the activation controller advances to its next state based on its current inputs. The step is performed at a time that does not adversely affect the operation of the CPU. This bit must be returned to 0 following the step, to prepare for subsequent steps. Stepping overrides the Hold Activation State bit (b3). Note that the step will not occur unless the CPU has determined that a condition for continuing to the next activation state has been satisfied.

Hold Activation State
When this bit is set to 1, the activation controller is held in the current state until either a Load Activation State (b5) or a Step Activation State (b4) is performed.

Big Jump Select
When this bit is 1, timing phase jumps will be made in four–unit increments. When this bit is 0, timing phase jumps will be made in one–unit increments.

Force Linkup
When this bit is set to 1, the internal status is forced to be that of full–duplex operation. Note that the CPU is still operating according to the activation state as read in BR11. However, loopbacks and maintenance operations may be performed at the Superframe Framer/Deframer level with full data transparency.

EPI 18:11
These are the most significant bits of the EPI register within the CPU. The EPI register in the CPU takes on different meanings, depending on the current activation state. This EPI register is updated once per frame. The EPI 10:3 bits are in Register BR13. EPI 2:0 are not available to the external microcontroller.

4.4.14 BR13: Echo Canceller Test Register

This register contains several items that control the internal operation of the U–interface transceiver echo canceller. These bits are cleared on a Hardware Reset ($\overline{\text{RESET}}$) or Software Reset (NR0(b3)). Note that none of the control bits in this register affect the operation of the chip unless the Activation Control Steer bit in BR12(b7) is set to 1. This register is replaced by OR13, when BR10(b2) = 1.

	b7	b6	b5	b4	b3	b2	b1	b0
BR13	Enable MEC Updates wo	Accumu-late EC Output wo	Enable EC Updates wo	Fast EC Beta wo	Accumu-late DFE Output wo	Enable DFE Updates wo	Fast DFE/ARC Beta wo	Clear All Coeffi-cients wo
	EPI 10 ro	EPI 9 ro	EPI 8 ro	EPI 7 ro	EPI 6 ro	EPI 5 ro	EPI 4 ro	EPI 3 ro

Enable MEC Updates
When set to 0, this bit freezes the current coefficients of the Memory Echo Canceller (MEC).

Accumulate EC Output
When this bit is set to 1, the results of all three echo cancellers (MEC, Transversal Echo Canceller (TEC), and Infinite Impulse Response Echo Canceller (IIREC)) are included in the process of recovering the received symbol.

Enable EC Updates
When set to 0, this bit freezes the current coefficients of the TEC and IIREC echo cancellers.

Fast EC Beta
This bit controls the echo canceller beta constant. A 1 instructs the echo canceller to adapt at its fastest rate.

Accumulate DFE Output
When 0, this bit forces the output from the Decision Feedback Equalizer (DFE) convolution to 0 and the symbol storage elements of the DFE will set to alternating ± 1. When this bit is 1, the DFE convolution is included in the process of recovering the received symbol.

Enable DFE Updates
When set to 0, this bit freezes the DFE coefficients and the Adaptive Reference Control (ARC) tap.

Fast DFE/ARC Beta

This bit controls the betas for the DFE and ARC. When set to 1, the DFE and ARC adapt at their highest rate.

Clear All Coefficients

When set to 1, the coefficients in the DFE, ARC, TEC, and MEC are cleared and the elastic buffer is reset. The timing offset between the receive and transmit clocks is not altered by setting this bit.

EPI 10:3

These are the least significant bits of the EPI register within the CPU. The EPI register in the CPU takes on different meanings, depending on the current activation state. This EPI register is updated once per frame. The EPI 18:11 bits are in Register BR12. EPI 2:0 are not available to the external microcontroller.

4.4.15 BR14: Test Register

This register is used for setting various diagnostic modes. This register is cleared on a Hardware Reset ($\overline{\text{RESET}}$) or Software Reset (NR0(b3)). When all of these bits are 0, the register map is in the default mode.

CAUTION

Reserved bits b7, b5, b2, and b1 must be set to 0 at all times.

	b7	b6	b5	b4	b3	b2	b1	b0
BR14	Reserved rw	ro/wo to r/w rw	Reserved rw	Framer–to–Deframer Loop rw	± 1 Tones rw	Reserved rw	Reserved rw	Enable CLKs rw

ro/wo to r/w

When this bit is set to 1, all of the write–only registers, except BR15A, become read/write registers for diagnostic purposes. A bit that is normally read–only will not be available when this bit is set to 1. Setting this bit to 1 has no effect on BR15A(b4:b0); they remain write–only bits at all times.

Framer–to–Deframer Loopback

This bit enables the Superframe Framer to Superframe Deframer Loopback mode when it is 1. The transmit drivers are off in this mode.

±1 Tones

When this bit is set to 1, the Superframe Framer generates its tones (10 kHz and 40 kHz) using ± 1 quats instead of the default of ± 3 quats.

Enable CLKs

When set to 1, this bit enables the SYSCLK, EYEDATA, RxBCLK, TxBCLK, and TxSFS pins. Note that BR15A(b3) must also be set to 1 for the TxSFS output to be enabled.

NOTE

SYSCLK, EYEDATA, RxBCLK, TxBCLK, and TxSFS pin functionality can be modified by the setting of bits in OR8 and OR9.

4.4.16 BR15: Revision Number Register

This read–only register contains the revision number of the particular U–interface transceiver device. BR15 is accessed by a SCP or PCP transfer when BR7(b7) is 0 and the byte address is 15.

	b7	b6	b5	b4	b3	b2	b1	b0
BR15	Mask 7 ro	Mask 6 ro	Mask 5 ro	Mask 4 ro	Mask 3 ro	Mask 2 ro	Mask 1 ro	Mask 0 ro

Mask 7:0

These bits allow for an electronic determination of the revision number of the MC145572 U–interface transceiver manufacturing mask set.

4.4.17 BR15A: Baud Clock and Timing Test Register

This register is used to enable clock and test data outputs. All writable bits in this register are cleared to 0 after a reset. BR15A is accessed by a CPI transfer when BR7(b7) is 1 and the byte address in the SCP transfer is 15. The write–only bits in this register remain write–only bits when BR14(b6) is set to 1.

CAUTION

Reserved bits b5 and b4 must be set to 0 at all times.

	b7	b6	b5	b4	b3	b2	b1	b0
BR15A	FREQ ADAPT rw	Jump Disable rw	Reserved rw	Reserved wo	Enable TxSFS wo	Reserved wo	Reserved wo	Enable Eye Data and Baud Clock wo
				Reserved ro	Reserved ro	Reserved ro	Reserved ro	Reserved ro

FREQ ADAPT

This bit is a read/write bit. There is no effect on the operation of the U–interface transceiver unless Control Steer (BR12 (b7)) is set to 1. When Control Steer is 1 and FREQ ADAPT is set to 1, the NT frequency adaptation circuits are enabled to adjust the external crystal frequency. Setting this bit to 0 freezes the frequency adaptation circuits in their current state.

Jump Disable

This bit is a read/write bit. Setting this bit to 1 disables the digital PLL when Activation Control Steer (BR12(b7)) is set to 1 (this bit is used for Motorola test purposes only).

Enable TxSFS

When set to 1 with BR14(b0) set to 1, this bit enables the transmit Superframe Sync to be output.

Enable Eye Data and Baud Clock

When set to 1, this bit enables the EYEDATA, SYSCLK, Rx BAUD CLK, and Tx BAUD CLK output pins.

NOTE

When the MC145572 is configured for IDL2 and SCP operation the 15.36 CLKOUT, 4.096 CLKOUT, and BUFXTAL pins default to “on.” Software written for MC145472/MC14LC5472 that set BR15A (b1 or b2) is not affected when an existing MC145472 or MC14LC5472 product is upgraded to MC145572.

4.5 OVERLAY REGISTERS

Table 4–3 shows the registers on MC145572 that overlay the standard byte registers. The SCP address for the overlay registers is the same as the address for the standard byte register set. The overlay registers are substituted for the standard registers, when at least one of BR7(b7) or BR10(b2, b1, b0) is set to 1. BR15A was implemented in MC145472, but the other registers are new to MC145572.

BR15A was modified on MC145572 from MC145472, to change the 15.36 MHz and 20.48 MHz clock outputs to default to enabled. In order to maintain code–compatibility with MC145472, the bits were moved from BR15A to the overlay registers. To disable these clocks, OR9(b2, b1, b0) can be set to 1s.

Overlay registers OR0 – OR5 are used for defining the timeslot assignment when the IDL2 interface is put into Timeslot Assigner mode by setting one or more of the bits TSA B1 Enable, TSA B2 Enable, or TSA D Enable, found in Overlay register OR6. Timeslots are two DCL clocks in width and are numbered starting from 0.

Overlay register OR5 also is used to define the GCI timeslot when the bit GCI Mode Enable is asserted in Overlay register OR6. The remainder of the bits in Overlay registers OR6 – OR9 are explained following Table 4–3.

All bits in the overlay registers are reset to 0 on hardware and software resets. The overlay registers are hidden after a hardware or software reset. They can be accessed when BR10(b0) is set to 1.

4.5.1 OR0: D_{out} B1 Timeslot Register

This register controls when the B1 timeslot appears on the D_{out} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR0	D_{out} B1 Channel Timeslot Bits (7:0) rw							

4.5.2 OR1: D_{out} B2 Timeslot Register

Programmed the same way as OR0. This register controls when the B2 timeslot appears on the D_{out} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR1	D_{out} B2 Channel Timeslot Bits (7:0) rw							

4.5.3 OR2: D_{out} D Timeslot Register

Programmed the same way as OR0. This register controls when the D timeslot appears on the D_{out} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR2	D_{out} D Channel Timeslot Bits (7:0) rw							

4.5.4 OR3: D_{in} B1 Timeslot Register

Programmed the same way as OR0. This register controls when the B1 timeslot is input from the D_{in} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR3	D_{in} B1 Channel Timeslot Bits (7:0)							
	rw							

4.5.5 OR4: D_{in} B2 Timeslot Register

Programmed the same way as OR0. This register controls when the B2 timeslot is input from the D_{in} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR4	D_{in} B2 Channel Timeslot Bits (7:0)							
	rw							

4.5.6 OR5: D_{in} D and GCI Timeslot Register

Programmed similar to OR2. This register controls when the D timeslot is input from the D_{in} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR5	D_{in} D Channel Timeslot Bits (7:0)							
						GCI Slot		
						S2 Bit	S1 Bit	S0 Bit
	rw					rw		

GCI Slot (2:0)

In IDL2 mode, if OR6 b(3) is set to indicate GCI 2B+D operation, b(2:0) is used to program the GCI timeslot. These bits are treated like the S2, S1, and S0 pins in Full GCI mode. See Table 3–7 for timeslot assignment.

4.5.7 OR6: Timeslot and GCI Control Register

This register is used to enable the timeslot assigner and select GCI 2B+D data format when in IDL2 mode. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR6	TSA B1 Enable	TSA B2 Enable	TSA D Enable	GCI Select M4 – BR0	GCI Mode Enable	Reserved	Reserved	Reserved
	rw	rw	rw	rw	rw	rw	rw	rw

NOTE

Setting b7, b6, or b5 will put the MC145572 in Timeslot Assigner mode. In Timeslot Assigner mode, the IDL2 8/10 mode bit in BR7(b0) is ignored and data is placed according to values programmed in OR0 – OR5.

TSA B1 Enable

This bit is used to enable the B1 channel in IDL2 Timeslot mode. The B1 timeslot is defined through Overlay registers OR0 and OR3. Whenever any channel (B1, B2, or D) is enabled for Timeslot mode, all channels enter Timeslot mode. If in Timeslot mode and TSA B1 Enable is 0, then the B1 channel is not present on the pin D_{out}, and the B1 channel transmit on the U–interface is actively driven to V_{OH}.

TSA B2 Enable

This bit is used to enable the B2 channel in IDL2 Timeslot mode. The B2 timeslot is defined through Overlay registers OR1 and OR4. Whenever any channel (B1, B2, or D) is enabled for Timeslot mode, all channels enter Timeslot mode. If in Timeslot mode and TSA B2 Enable is 0, then the B2 channel is not present on the pin D_{out}, and the B1 channel transmit on the U–interface is actively driven to V_{OH}.

TSA D Enable

This bit is used to enable the D channel in IDL2 Timeslot mode. The D timeslot is defined through Overlay registers OR2 and OR5. Whenever any channel (B1, B2, or D) is enabled for Timeslot mode, all channels enter Timeslot mode. If in Timeslot mode and TSA D Enable is a 0, then the D channel is not present on the pin D_{out}, and the D channel transmit on the U–interface is actively driven to V_{OH}.

If both TSA D Enable and D channel port Enable are set to 1, then the D channel data is presented on both D_{out} and DCH_{out}, and the data transmit onto the U–interface is taken from DCH_{in}. If the D channel port is enabled and TSA D Enable is set to 0 (see Overlay register OR8(b0)), then the D channel continues to operate on the D channel port and D_{out} is high impedance during the D channel bit time.

The clock on DCHCLK (assuming the D channel port is enabled), operates relative to FSR, based on the timeslot programmed in the timeslot registers for the D channel.

GCI Select M4 – BR0

This bit is useful only in conjunction with full GCI mode when the pin MCU/$\overline{GCI}$ = 0. In that mode, when this bit is set to 0, the GCI C/I channel control automatically sets and resets M4 channel control bits pertaining to the activation state. The bits controlled by the C/I channel are: {`act`, `dea`, `uoa`} in the LT mode and {`act`, `sai`} in the NT mode. Additionally, the {ps1, ps2} bits in the NT mode are transmitted according to the state of IN1 and IN2 pin inputs. When this bit is set to 1, all M4 bits are transmitted according to the data present in Register BR0. When operating in full GCI mode, the bit can be set/cleared by using the monitor channel byte register read/write commands. After a hardware or software reset this bit is 0. Normally, GCI operation does not require this bit to be set to a 1.

GCI Mode Enable

This bit makes it possible to transfer 2B+D data over the IDL2 interface as if it were in GCI mode. This operation is established by setting the pin MCU/$\overline{GCI}$ and this bit to 1. The 2B+D data is transferred at the timeslot indicated in OR5(2:0). The monitor and C/I channels of the GCI interface are ignored as inputs and are not driven as outputs. Additionally, the operation of FSC, regarding its control of the transmit superframe in Slave mode, takes precedence over the input on SFAX. See OR5 b(2:0) for GCI slot assignment in this mode.

4.5.8 OR7: Configuration Register 1

This register is used to enable or control various modes of the MC145572. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR7	Internal Analog Loopback rw	Line Connect rw	$\overline{TSEN}$ DCH Enable rw	IDL2 Rate 2 rw	IDL2 Long Frame Mode rw	`crc` Corrupt Mode rw	`febe`/ `nebe` Rollover rw	M4 Trinal Mode rw

Internal Analog Loopback

When this bit is set to 1, the analog loopback path is inside the MC145572. Default after any reset is 0 or external analog loopback path.

Line Connect

When this bit is 1, the U–interface line can remain connected during analog loopbacks. When this bit is 0, the line must be disconnected. Default after any reset is 0.

$\overline{\text{TSEN}}$ DCH Enable

This bit enables $\overline{\text{TSEN}}$ when D channel data is present on the D_{out} or DCH_{out} pins. When the timeslot assigner is enabled, the $\overline{\text{TSEN}}$ signal is active during the timeslot which D channel data is transferred.

IDL2 Rate 2

In the IDL2 mode, when IDL2 rate 2 is set to 1, the IDL2 clock (DCL) rate is 512 kHz. IDL2 clock speed (see Register BR7) is ignored when this bit is set to 1. In full GCI mode, as a master in the NT mode, the DCL clock rate is selected using the pin input (see CLKSEL description in **Section 3.3.4**). This bit also sets the clock frequency on FREQREF or $FREF_{out}$ when in NT Slave mode.

IDL2 Long Frame Mode

While operating as an IDL2 master, this bit controls whether the FSR and FSX operate in Long Frame or Short Frame mode. If this bit is 1, both FSR and FSX operate in Long Frame mode. As an IDL2 slave, the MC145572 determines the mode based on the length of FSR. See **Section 5.4.2.**

`crc` Corrupt Mode

This bit changes the operating mode of the input control bit `crc` Corrupt in register BR8. When `crc` Corrupt mode is set to 1, the `crc` Corrupt input is used to only corrupt one outgoing superframe `crc`. When `crc` Corrupt mode is set to 0, the `crc` Corrupt behaves as it did in the MC145472, unaligned to the transmit superframe, and continues to affect the `crc` data until explicitly reset.

`febe`/`nebe` Rollover

This bit changes the operating mode of the `febe` and `nebe` counter registers BR4 and BR5. When `febe`/`nebe` rollover is set to 1, the `febe` and `nebe` counter registers do not saturate at all 1s, but instead, rollover from $FF to $00. When `febe`/`nebe` rollover is set to 0, the `febe` and `nebe` counter registers behave just as they do in the MC145472.

M4 Trinal Mode

This bit changes the operating mode of the persistence checking performed on the `act`, `dea`, `sai`, and `uoa` bits in the deframer. When M4 Trinal mode is set to 1, the checked M4 bits must be valid for three consecutive superframes before asserting Verified `act`, or Verified `dea`, etc. When M4 Trinal mode is set to 0, the checked M4 bits behave as they did in the MC145472, only checking them as configured in BR9(b5,b4). When operating in full GCI mode, the MC145572 performs trinal checks on the received M4 channel `act`, `dea`, `sai`, and `uoa` bits (see Table 4–11).

4.5.9 OR8: Configuration Register 2

This register is used to control the dump/restore operation, SFAX and SFAR outputs, and three–state enable for off–chip bus drivers. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR8	D/R Mode 1 rw	D/R Mode 0 rw	SFAX Output Enable rw	FREQREF Output Enable rw	$\overline{\text{TSEN}}$ BCH Enable rw	Reserved rw	SFAX/ SFAR Enable rw	D Channel Port Enable rw

CAUTION

Reserved bit b2 must be set to 0 at all times.

D/R Mode (1:0)
These bits control the operating mode of Dump/Restore Access Overlay register OR12. {0,0} sets the mode for normal dumping and restoring of the internal coefficients via the EYE_{out} interface. {1,0} permits read access to the arctap. {0,1} permits write access to the arctap. {1,1} should be selected to perform dump/restore via the IDL2 or GCI interface depending on the state of the MCU/$\overline{GCI}$ pin.

SFAX Output Enable
When this bit is set to 1 in LT mode, it forces the SFAX pin to be an output. Normally, in LT mode, SFAX is an input to control the start of the transmit superframe.

FREQREF Output Enable
When this bit is set to 1 in NT mode, it forces the pin FREQREF to become an output and source a locked clock. The locked clock is the same as DCL clock.

$\overline{TSEN}$ BCH Enable
When this bit is set to 1, it enables the pin $\overline{TSEN}$ to operate an off–chip bus driver during the B1 and B2 timeslots. When the timeslot assigner is enabled, the TSEN signal is active during the timeslot in which B1 and B2 channel data is transferred.

SFAX/SFAR Enable
When this bit is set to 1, it enables two pins on the MC145572 to be used to control and/or indicate the location of the transmit and receive superframes relative to the IDL2 interface.

D Channel Port Enable
When this bit is set to 1 and pin MCU/$\overline{GCI}$ = 1, three pins are enabled on the MC145572 to be used as a D channel port. When the D channel port is enabled, D channel information transmitted on the U–interface is taken from DCH_{in2}, and D channel information from the U–interface is transmitted on both DCH_{out} and D_{out2}. (Note that D_{out} does not output the D channel data when the IDL2 interface is in timeslot mode, and the TSA D Enable is not set to 1.)

4.5.10 OR9: Configuration Register 3

This register is used to control the analog loopback and clocks that are available at MC145572 pins. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

CAUTION

Reserved bit b7 must be set to 0 at all times.

	b7	b6	b5	b4	b3	b2	b1	b0
OR9	Reserved rw	Open Feedback Switches rw	Analog Loopback rw	CLKOUT 2048 rw	4096 Hirate rw	2048 Disable rw	1536 Disable rw	4096 Disable rw

Open Feedback Switches
When this bit is set to 1, it opens the internal feedback path between the transmit (TxP/TxN) and the receive (RxP/RxN) sections. This feature may be used in conjunction with analog loopback.

Analog Loopback
When this bit is set to 1, it invokes a receive analog loopback on the MC145572.

CLKOUT 2048
When this bit is set to 1, it enables a 20.48 MHz buffered clock output on pin 25 of the MC145572FN and on pin 8 of the MC145572PB.

4096 Hirate
When this bit is set to 1, it causes the 4.096 MHz clock output to cleanly transition to a 10.24 MHz rate. When set back to 0, the clock cleanly transitions to 4.096 MHz.

2048 Disable

When this bit is set to 1, it causes the 20.48 MHz clock output at BUFXTAL to go to high impedance.

1536 Disable

When this bit is set to 1, it causes the 15.36 CLKOUT pin to go high impedance.

4096 Disable

When this bit is set to 1, it causes the 4.096 CLKOUT pin to go high impedance. This bit may only be written to once, following a hardware or software reset. Once the 4.096 CLKOUT pin has been turned off by setting this bit, it can only be re–enabled by asserting a hardware or software reset to the MC145572. This bit is reset by hardware reset, NR0(b3) = 1 or NR0(b1) = 1.

4.6 D CHANNEL AND DEBUG REGISTERS

4.6.1 OR12: D Channel Data Register

When BR10(b1) is set to 1, this double buffered register takes the place of Normal Byte register BR12, and the register becomes an 8–bit read–only/write–only register providing access to the D channel. In this mode, D channel input data present on the pin interfaces of MC145572 is ignored. Instead, D channel is sourced strictly from this register. D channel data received from U–interface is byte aligned to Superframe Sync, and is readable through OR12, eight bits at a time. This register is updated with the received D channel data, when SFS, NR1(b3) is a 1. Data is transferred from OR12 to the U–interface, when SFS, NR1(b3), is a 1.

$\overline{\text{IRQ3}}$ is used to indicate when each new eight bits of data are received. A special code (1111) is loaded in Nibble register NR1, to indicate that the source of the interrupt is the D channel access register. Reading OR12 clears the special code (1111) from NR1, but does not affect any updates in activation status. So, if there has been a change in activation status, an interrupt is still queued up even though the D channel interrupt has been cleared. Both transmit and receive D channel data are aligned to the transmit and receive superframes. The MC145572 does not perform any HDLC framing/deframing.

D channel data is transmitted to and received from the U–interface most significant bit first.

OR12	D Channel Transmit Bits (7:0)	wo
	D Channel Transmit Bits (7:0)	ro

NOTE

If this register is used when the timeslot assignment is enabled, D channel timeslot must not be 0, so as to maintain synchronization with the transmit superframe. This is especially important in LT mode, when SFAX is used as an input.

4.6.2 OR13: Dump/Restore Test Register

This register takes the place of Byte register BR13 when BR10 B(2) is set, and the register becomes a byte–wide access port to the dump/restore mechanism of the U–chip. Two more bits in the overlay registers control the operating mode of the dump/restore mechanism. See Overlay register OR8. This bit is reset by both hardware and software resets. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

OR13	Dump Register Write Access	wo
	Dump Register Read Access	ro

5

MCU MODE DEVICE FUNCTIONALITY

5.1 FUNCTIONAL OVERVIEW

This chapter describes the operation of MC145572 when operated in the MCU mode.

A functional block diagram of the MC145572 U–interface transceiver is shown in Figure 5–1. This device utilizes mixed analog and digital signal processing circuit technology to implement an adaptively equalized echo cancelling full–duplex transmitter/receiver or transceiver.

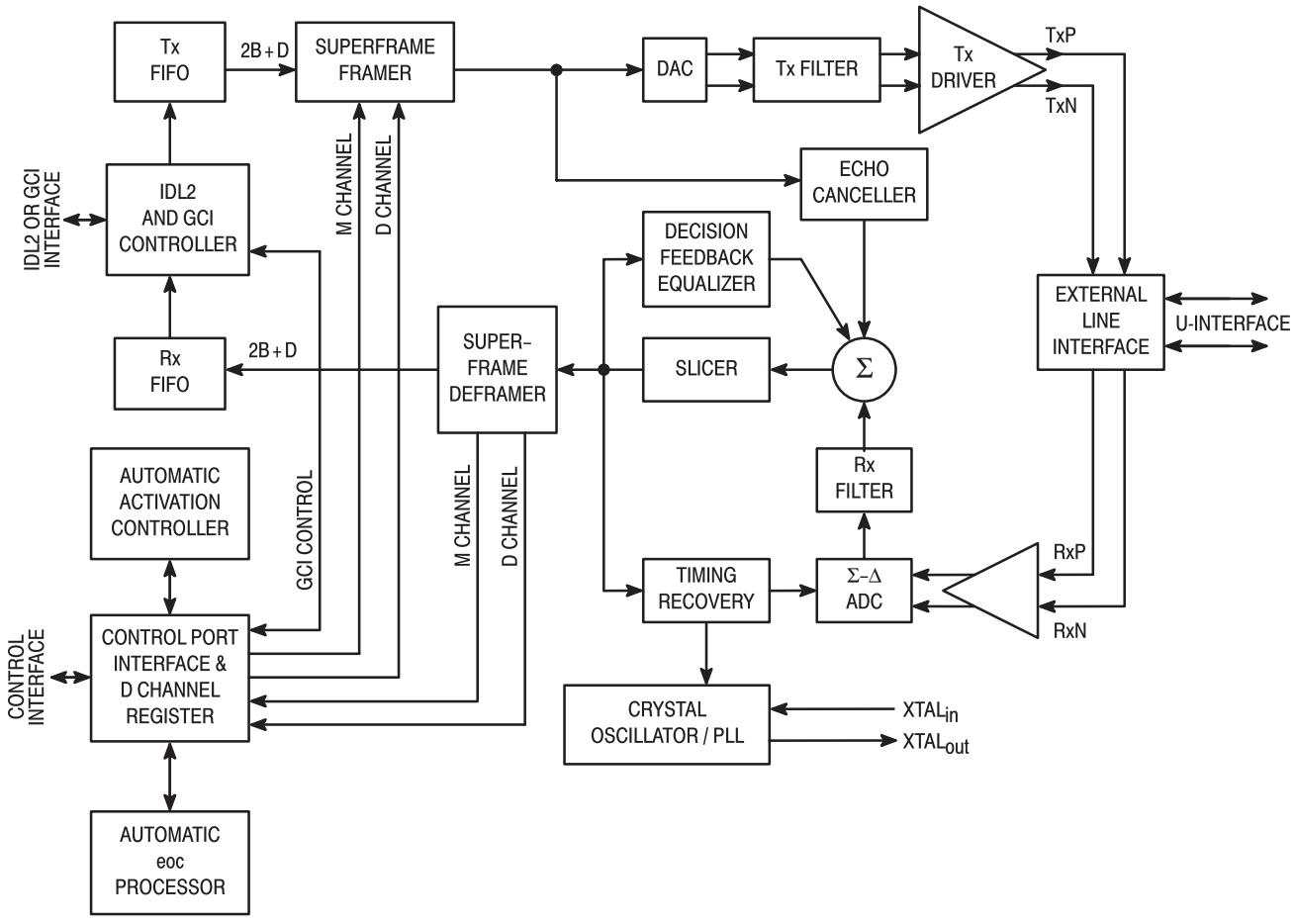


Figure 5–1. MC145572 Functional Block Diagram

The 2B+D data is input to the device at the D_{in} pin of the time division multiplexed data interface. This data is passed through a three–frame deep FIFO prior to being formatted and scrambled in the Superframe Framer. The resulting 160 kbps binary data stream is converted to an 80 kbaud dibit stream, which is subsequently converted to four analog amplitudes by the DAC (digital–to–analog converter). The resulting pulse amplitude modulated signal is band limited by the Tx filter prior to entering the Tx driver, which differentially drives the line coupling circuit to the twisted wire pair.

From the twisted wire pair, information from the far–end U–interface transceiver is coupled through the external line interface circuit to the differential receiver inputs RxP and RxN. (In this two–wire environment, the transmitted signal is also coupled into the receiver inputs.) This combined analog signal

is converted to a digital word in the Σ–Δ (sigma–delta) ADC (analog–to–digital converter). After filtering, an adaptively generated replica of the transmitted signal, calculated by the echo canceller, is subtracted from the combined signal leaving only the far–end signal. In addition, phase distortion present in the far–end signal is corrected by the DFE. The resulting four–level signal is decoded by the slicer to produce a 160 kbps data stream. Timing information is also recovered from the far–end signal. The Superframe Deframer descrambles and disassembles the received superframes and passes the received 2B+D data through a three IDL frame deep FIFO to the IDL interface, where it is available at the D_{out} pin of the time division multiplexed data interface.

The MC145572 permits the designer to select one of three options for control of the device and access to its register set. When operating in MCU mode, the MC145572 can be configured for either SCP or PCP mode of operation. In SCP mode, control and status of the device is handled via the SCP, a standard four–wire serial microcontroller interface. In PCP mode, the MC145572 is configured to provide an eight–bit wide data port with a chip select and read/write pin. In either case, the internal register set of the MC145572 gives an external microcontroller access to the 4 kbps Maintenance channel provided across the U–interface.

When the MC145572 is configured for GCI mode, the C/I channel of the GCI interface is used for control and status messages. The GCI Monitor channel is used to send and receive Maintenance channel messages. The Monitor channel also permits the internal registers of the MC145572 to be read from or written to, if it is desired to bypass the normal operation of the GCI interface.

The eoc portion of the M channel can be handled automatically with the internal Automatic eoc Processor. In addition, activation and deactivation of the MC145572 is handled by an Automatic Activation Controller.

The MC145572 requires a single 20.48000 MHz pullable crystal connected between the $XTAL_{in}$ and $XTAL_{out}$ pins. No other external components are required for the crystal oscillator. Internal crystal pulling circuitry adjusts the crystal frequency in both LT and NT modes of operation.

Detailed descriptions of the various interfaces and user accessible sections are provided in this chapter.

5.2 MC145472/MC14LC5472 COMPATIBILITY

After either a hardware or software reset, the MC145572 maintains basic pin function and register compatibility with the MC14LC5472 U–interface transceiver when configured for MCU mode and using the SCP interface. There are differences between MC14LC5472 and MC145572 in exact signal requirements and outputs for these pins.

Most software written for MC14LC5472 will operate MC145572 without requiring any modifications. The MC145572 has an extended register set which provides access to the on–chip timeslot assigner, I/O pin configuration bits, D channel, and internal parameters of the device. The extended registers are accessed by setting bits in Register BR10 that were reserved bits for MC14LC5472. The new registers then overlay the original registers and are referred to in this document as Overlay registers OR0 through OR9, OR12, and OR13. Register BR10 is common to both register sets, permitting software to switch between the basic register set and the overlay register set, as required. Tables 4–1, 4–2, and 4–3 detail the register set of MC145527. See Chapter 4, ***Register Description,*** for details on the register set.

Tables 5–1 and 5–2 contain the MC145572 pin function charts. The MC145572 requires a line interface transformer having a turns ratio of 1:1.25 where the 1.25 is on the tip and ring side of the transformer. The MC14LC5472 used a line interface transformer having a 1:2 turns ratio.

When operated in MCU mode with the SCP, MC145572 has clock outputs enabled on 15.36 CLKOUT and BUFXTAL pins after a hardware or software reset. On MC14LC5472, these clocks were disabled after a hardware or software reset. Due to this change, the function of bits BR15A(b2, b1) have changed in MC145572. In MC14LC5472, these two bits enabled 15.36 CLKOUT and BUFXTAL outputs, respectively; when set to 1. In MC145572, these bits are reserved and writing a 1 to either of these bits to enable a clock, leaves the clock(s) enabled. To disable one or both of these clocks, software must set either bit b2 or bit b1 in Overlay register OR9.

Table 5–1. Mode Pin Breakout Summary and Comparison

Function	PLCC Pin No.	TQFP Pin No.	MC145572	MC14LC5472
V_{DD}	44	27	+ 5 V	+ 5 V
V_{SS}	2, 22	29, 5	Connect to Ground	Connect to Ground
$V_{DD}I/O$	24, 37	7, 20	+ 5 V or + 3 V	+ 5 V
$V_{SS}I/O$	23, 36	6, 19	Connect to Ground	Connect to Ground
$V_{DD}Rx$	3	30	+ 5 V	+ 5 V
$V_{SS}Rx$	4	31	Connect to Ground	Connect to Ground
$V_{DD}Tx$	11	38	+ 5 V	+ 5 V
$V_{SS}Tx$	10	37	Connect to Ground	Connect to Ground
TxP/TxN	9, 12	36, 39	Transmit Output	Transmit Output
RxP/RxN	5, 6	32, 33	Receive Input	Receive Input
$V_{ref}N/V_{ref}P$	7, 8	34, 35	Voltage Reference	Voltage Reference
$XTAL_{in}/XTAL_{out}$	33, 32	16, 15	Pullable Crystal Only	Pullable Crystal and Other Components
FREQREF	42	25	8 kHz Reference Input	Accepts One of Eight Reference Frequencies
$\overline{RESET}$	14	41	Reset When Low	Reset When Low
MCU/$\overline{GCI}$	43	26	MCU When = 1 GCI When = 0	Not Applicable
NT/$\overline{LT}$	15	42	NT Mode When = 1 LT Mode When = 0	NT Mode When = 1 LT Mode When = 0
M/$\overline{S}$	16	43	Master Mode When = 1 Slave Mode When = 0	Master Mode When = 1 Slave Mode When = 0
PAR/$\overline{SER}$	13	40	Select MCU Parallel Control Port When = 1 Select MCU Serial Control Port When = 0	Not Applicable

Table 5–2. Pin Function per Mode and MC14LC5472 Comparison

MC145572 Function						MC14LC5472
PLCC Pin No.	TQFP Pin No.	MCU/SCP Mode	MCU/PCP Mode	GCI Master Mode	GCI Slave Mode	Function
17	44	$\overline{IRQ}$	$\overline{IRQ}$	Not Used	Not Used	$\overline{IRQ}$
21	4	$\overline{SCPEN}$	$\overline{CS}$	IN1 (Note 1)	IN1	$\overline{SCPEN}$
20	3	SCPCLK	R/$\overline{W}$	IN2 (Note 1)	IN2	SCPCLK
18	1	SCPRx	D0	OUT1 (Note 2)	OUT1 (Note 2)	SCP Rx
19	2	SCPTx	D1	OUT2	OUT2	SCP Tx
27	10	FSR (Note 3)	FSR (Note 3)	FSC	FSC	IDL SYNC
28	11	FSX (Note 4)	FSX (Note 4)	Not Used	Not Used	Not Applicable
31	14	DCL	DCL	DCL	DCL	IDL CLK
29	12	D_{in}	D_{in}	D_{in}	D_{in}	IDL Rx
30	13	D_{out}	D_{out}	D_{out}	D_{out}	IDL Tx
34	17	4.096 CLKOUT	D2	4.096 CLKOUT	4.096 CLKOUT	4.096 CLK OUT
35	18	15.36 CLKOUT	D3	15.36 CLKOUT	15.36 CLKOUT	15.36 CLK OUT
38	21	BUFXTAL	D4	BUFXTAL	BUFXTAL	BUF XTAL
26	9	TxSFS (Note 5)	TxSFS (Note 5)	S0	S0	Tx SFS
25	8	SYSCLK (Note 6)	SYSCLK (Note 6)	S1	S1	SYSCLK
39	22	EYEDATA (Note 7)	D5	S2	S2	EYE DATA
40	23	TxBCLK (Note 8)	D6	Not Used	$FREF_{out}$	Tx BAUD CLK
41	24	RxBCLK (Note 9)	D7	CLKSEL	Not Used	Rx BAUD CLK

NOTES:
1. In NT mode, IN1 and IN2 carry PS1 and PS2 data.
2. DISS is OR'd into this output.
3. When IDL2 interface is operating in GCI electrical mode, this pin is named FSC.
4. When IDL2 interface is operating in GCI electrical mode, this pin is unused.
5. SFAX is muxed onto this pin.
6. 20.48 MHz, SFAR, and $\overline{TSEN}$ are muxed onto this pin.
7. DCHCLK and TxOFF are muxed onto this pin.
8. DCH_{in} and TxMAG are muxed onto this pin.
9. DCH_{out} and TxSIGN are muxed onto this pin.

5.3 CONTROL INTERFACES

When operated in MCU mode, MC145572 has two configurations that provide MCU access to its internal register set. The SPC mode is a four–wire serial interface that clocks data into or out of MC145572 at data rates up to 4 Mbps. This interface is compatible with National's MICROWIRE™ interface. The PCP mode configures MC145572 to have an eight–bit parallel data port that can be located anywhere in processor memory. The PCP mode is enabled when the MCU/$\overline{GCI}$ pin is tied to a 1 and the PAR/$\overline{SER}$ pin is tied to a 1. The SCP mode is enabled when the MCU/$\overline{GCI}$ pin is tied to a 1 and the PAR/$\overline{SER}$ pin is tied to a 0.

NOTE

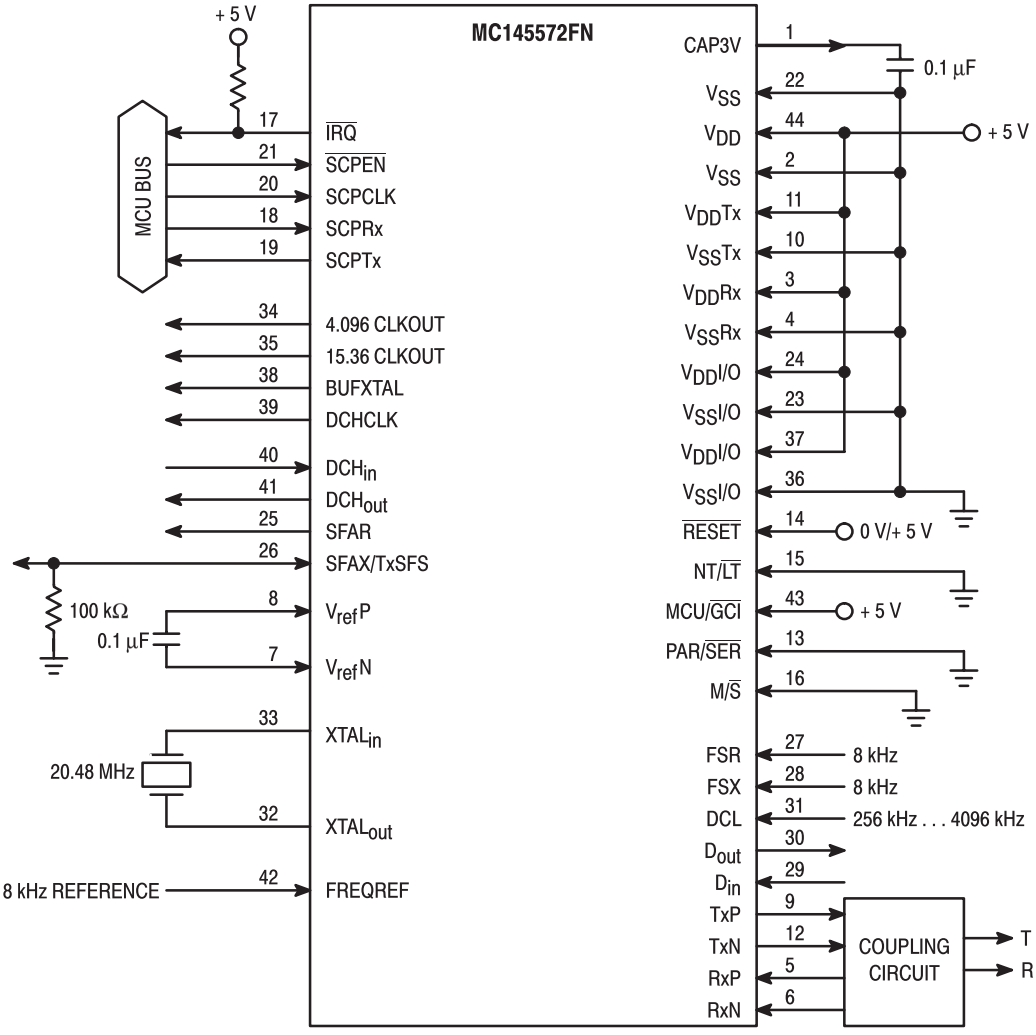
When MC145572 is configured for MCU operation, it is possible to put the IDL2 interface pins into GCI Electrical mode, which accepts GCI timing for transfer of 2B+D data only. This is done by setting bit OR6(b3) GCI Mode Enable. Access to the MC145572 register set is via the SCP or PCP. In GCI Electrical mode, the pin names and functions for IDL2 interface pins correspond to the GCI names and function.

5.3.1 SCP Mode

The MC145572 is equipped with an industry standard SCP interface. The SCP is used by an external controller, such as an M68HC05 family microcontroller, MC145488 Dual Data Link Controller, or MC68302 Integrated Multiprotocol Processor, to communicate with the U–interface transceiver.

The SCP is a full–duplex four–wire interface with control and status information passed to and from the U–interface transceiver. The SCP interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCPTx, SCPRx, SCPCLK, and $\overline{\text{SCPEN}}$, respectively. The SCP Clock determines the rate of exchange of data in both the transmit and receive directions, and the SCP Enable signal governs when this exchange is to take place. The four–wire SCP interface is supplemented with an interrupt request line, $\overline{\text{IRQ}}$, for external microcontroller notification of an event requiring service.

The operation and configuration of the U–interface transceiver is controlled by setting the state of the control registers within the U–interface transceiver and monitoring the status registers. The control, status, and M channel data registers reside in six 4–bit wide nibble registers, one 12–bit wide nibble register, and twenty–nine 8–bit wide byte registers. A complete register map and detailed register descriptions can be found in **Chapter 4.** Figure 5–2 shows pin configurations to operate MC145572 in IDL2 mode using the SCP for access to the register set. See **Chapter 10** for the SCP timing diagrams.



NOTE: In LT mode, the 100 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 5–2. MCU Mode with SCP Configuration

5.3.1.1 NIBBLE REGISTER OPERATION

The 4–bit nibble registers are accessed via an 8–bit SCP interface operation, as shown in Figure 5–3 for a write operation and Figure 5–4 for a read operation. The first bit of the transfer on SCPRx is a read/write (R/$\overline{W}$) bit, indicating the purpose of the operation. This is followed by a 3–bit address field (A2:A0), which specifies nibble address 0 through nibble address 5. (Nibble addresses 6 and 7 have other purposes, which are described later.) For a write operation, the 4–bit data word (D3:D0) follows. For a read operation, the 4–bit data word (D3:D0) follows on the SCPTx pin.

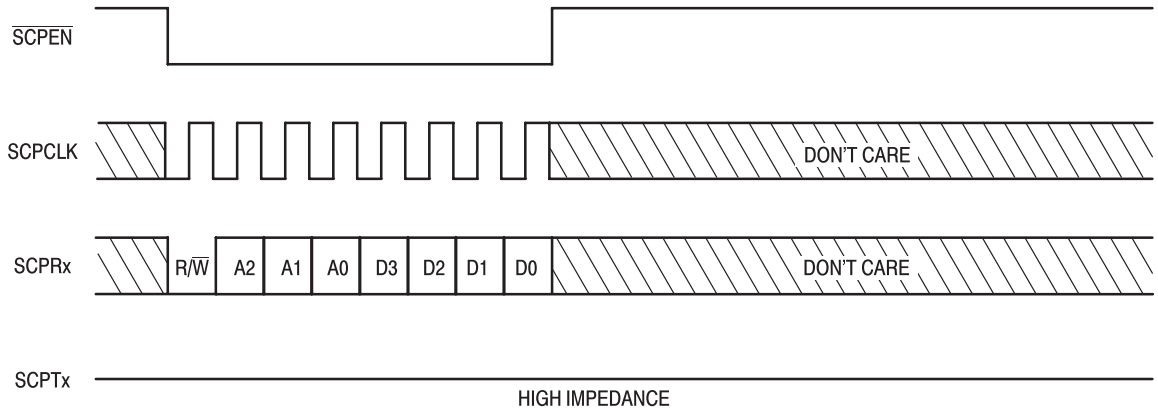


Figure 5–3. SCP Nibble Registers 0 – 5, Write Operation

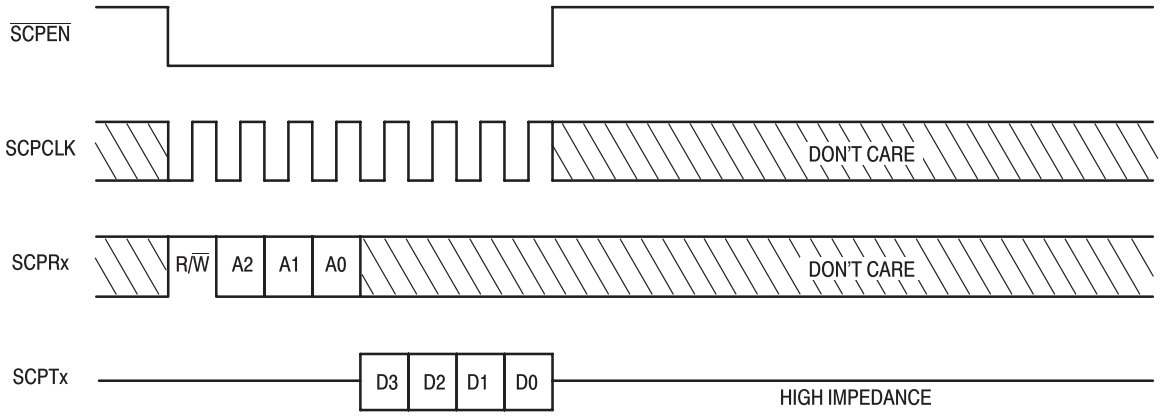


Figure 5–4. SCP Nibble Registers 0 – 5, Read Operation

5.3.1.2 REGISTER R6 OPERATION

The 12–bit Nibble register 6 is located at nibble register address 6 and can be accessed with two sequential 8–bit SCP interface operations, as shown in Figures 5–5 and 5–6. In this case, the second 8–bit operation accesses the last 8 data bits (D7:D0) as shown. Alternatively, this register can be accessed with a single 16–bit operation, as shown in Figures 5–7 and 5–8. See Register R6 description in **Section 4.3.7** for correspondence between the ANSI defined eoc bits and the data bits transferred over the SCP interface.

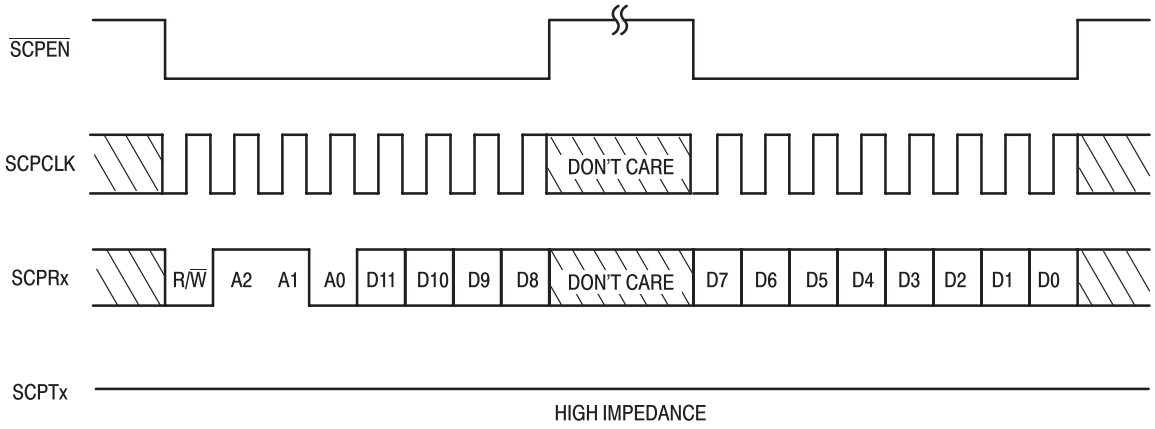


Figure 5–5. SCP eoc Register R6 Write Operation Using Double 8–Bit Transfer

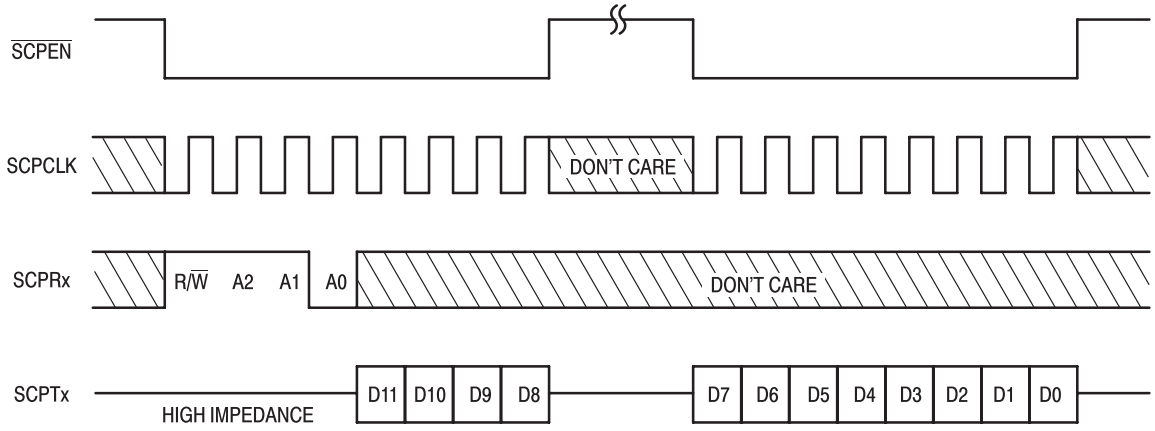


Figure 5–6. SCP eoc Register R6 Read Operation Using Double 8–Bit Transfer

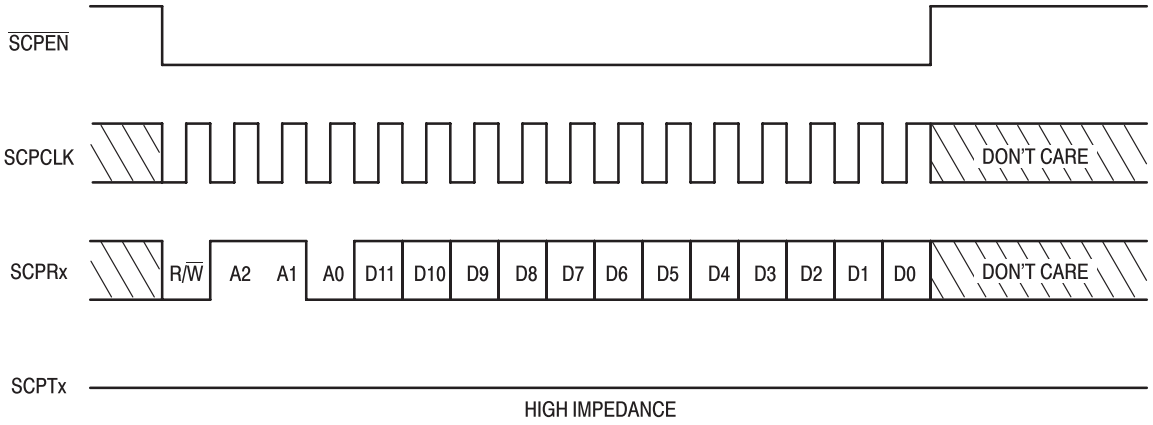


Figure 5–7. SCP eoc Register R6 Write Operation Using Single 16–Bit Transfer

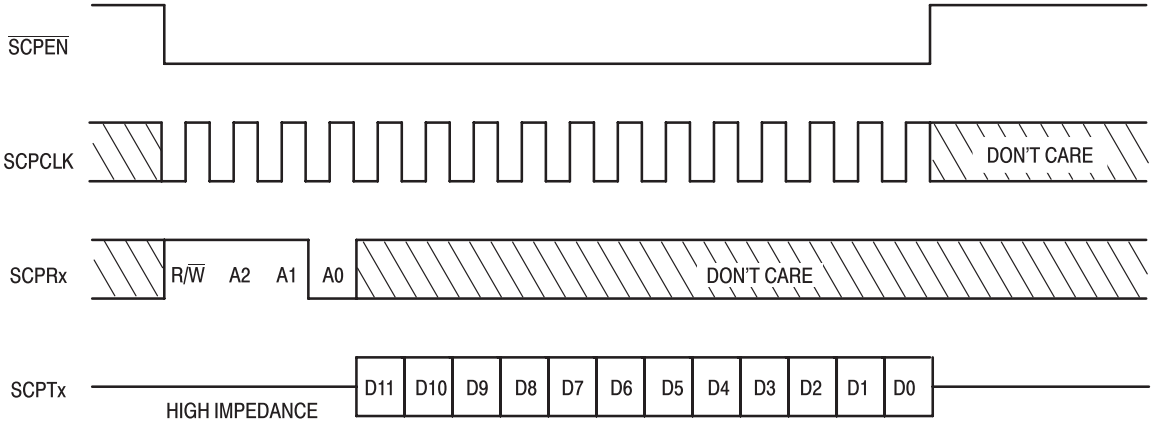


Figure 5–8. SCP eoc Register R6 Read Operation Using Single 16–Bit Transfer

5.3.1.3 BYTE REGISTER OPERATION

The 16 byte registers are addressed by addressing nibble address 7 followed by a 4–bit byte register address (A3:A0), as shown in Figures 5–9 and 5–10. A second 8–bit operation transfers the data word (D7:D0). Alternatively, these registers can be accessed with a single 16–bit operation, as shown in Figures 5–11 and 5–12.

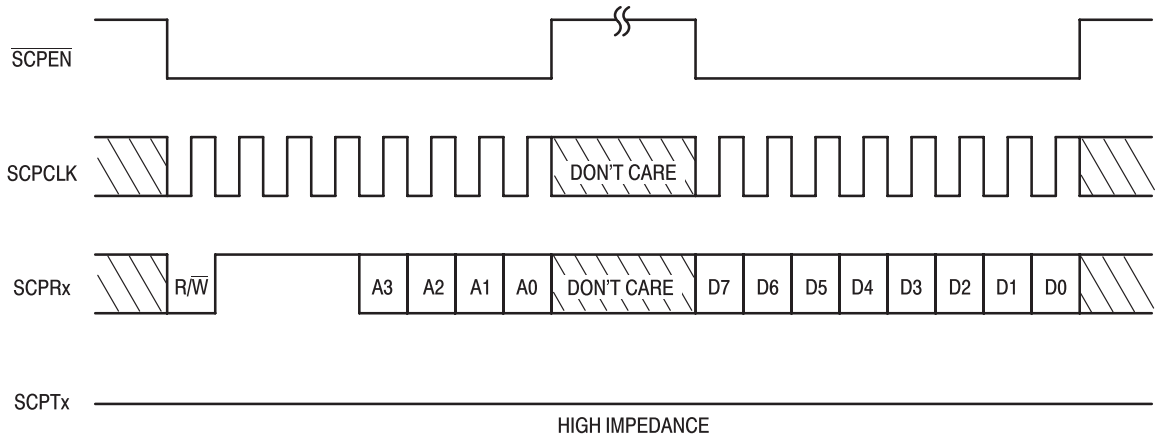


Figure 5–9. SCP Byte Register Write Operation Using Double 8–Bit Transfer

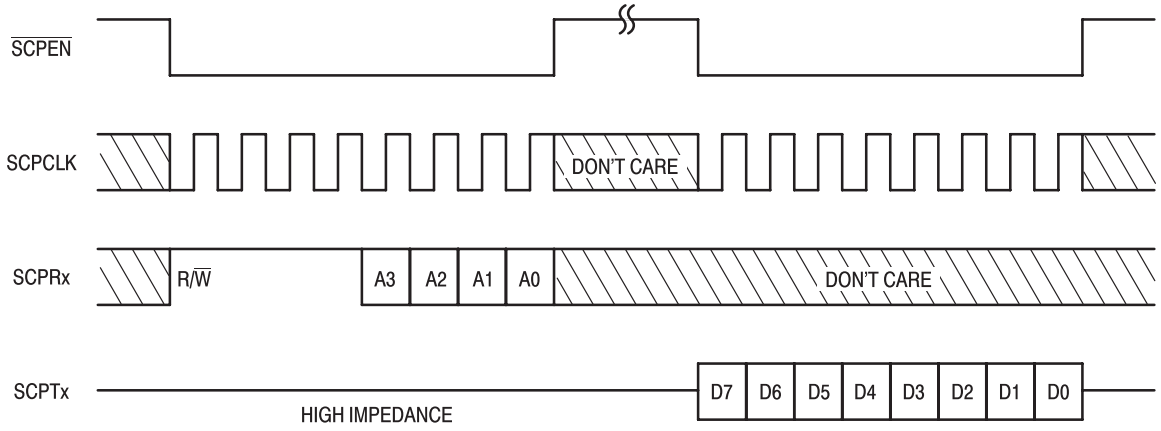


Figure 5–10. SCP Byte Register Read Operation Using Double 8–Bit Transfer

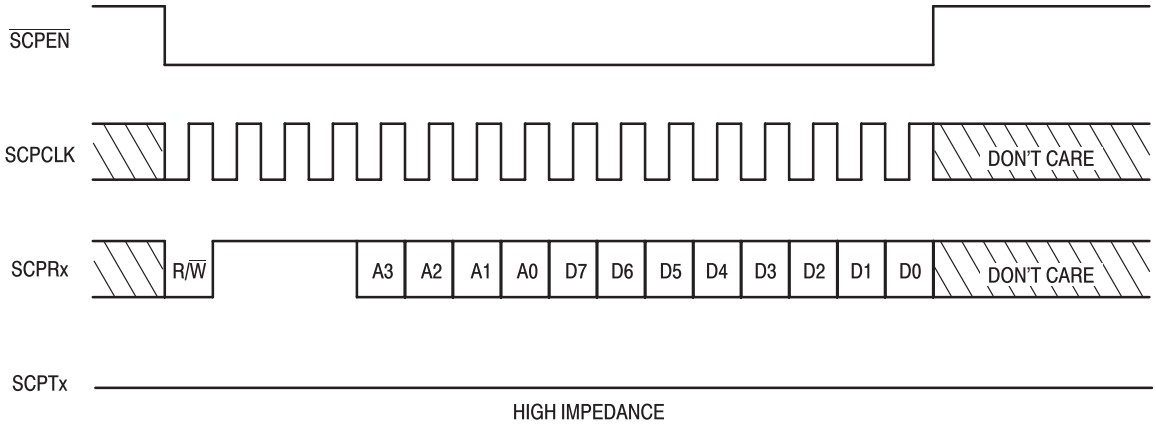


Figure 5–11. SCP Byte Register Write Operation Using Single 16–Bit Transfer

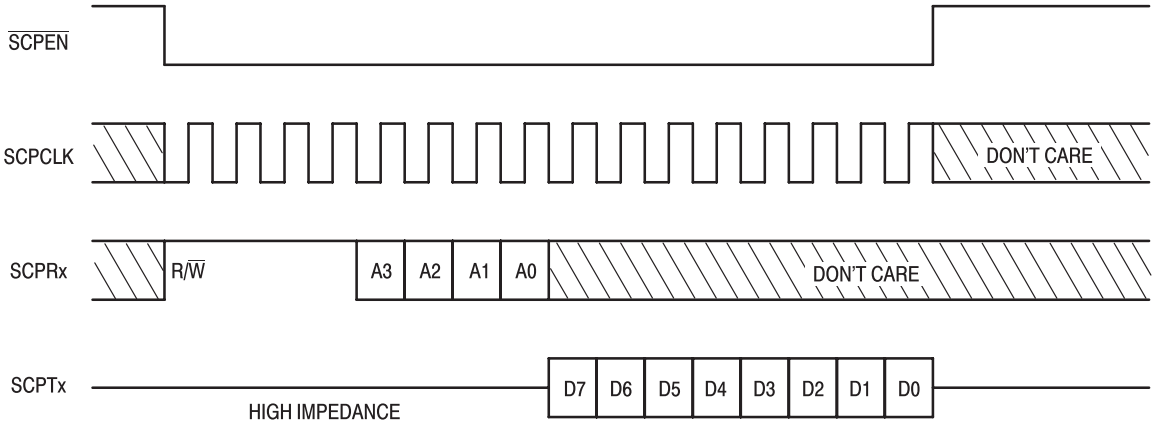
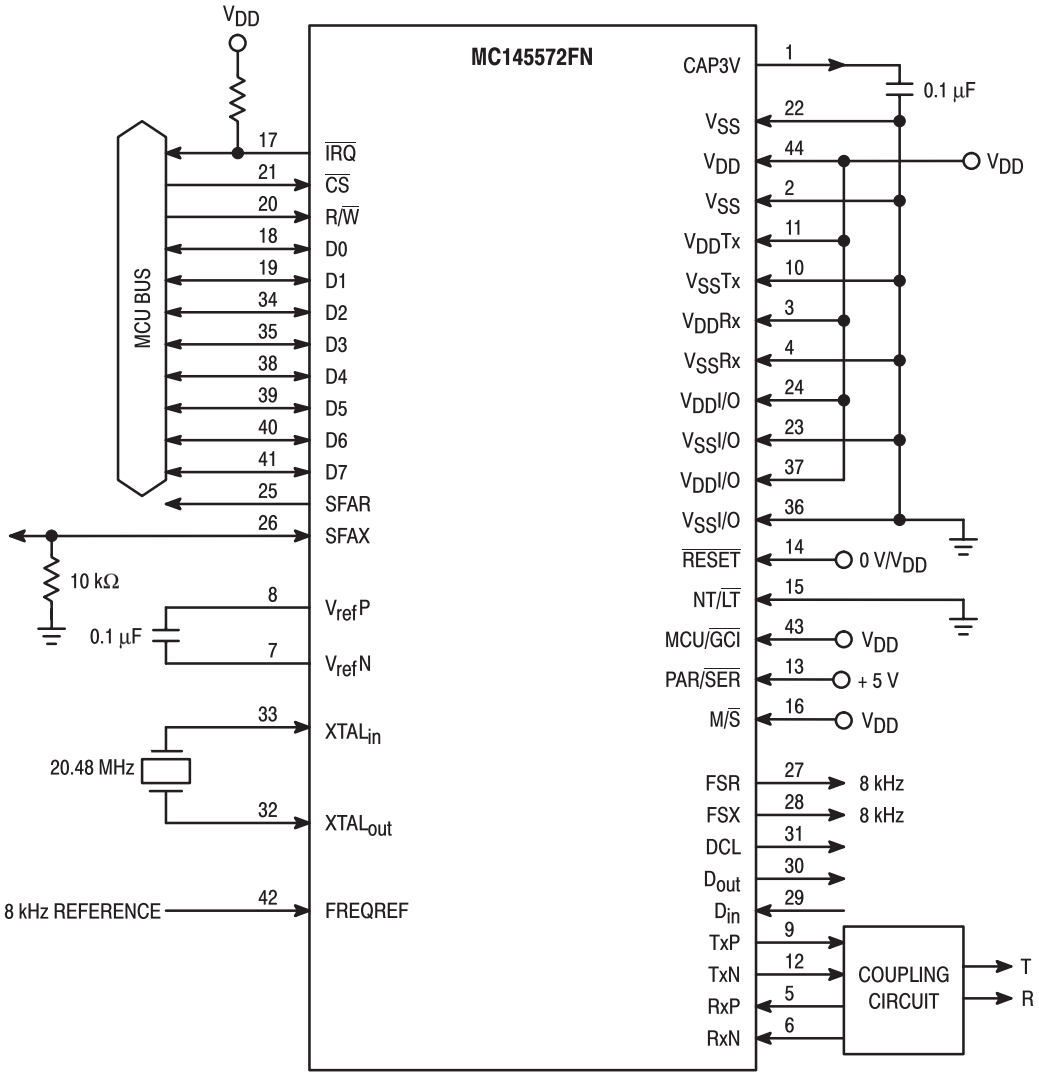


Figure 5–12. SCP Byte Register Read Operation Using Single 16–Bit Transfer

5.3.2 PCP Mode

In PCP mode, the MC145572 is configured to have a single address byte wide data port for access to the internal register set. A read/write pin (R/$\overline{W}$) and chip select pin ($\overline{CS}$) are provided to enable read or write accesses to the data port. For an external microcontroller, such as the MC68302, to access an individual nibble, byte, or overlay register; a sequence of write and read operations is required. The first access is always a write cycle that writes a pointer and internal read/write indicator to the MC145572. The pointer byte contains the Nibble or Byte register address and for the case of the Nibble register, writes the data to be written. This initial write may be followed by up to two read accesses or one write access. An open drain $\overline{IRQ}$ output pin is provided for interrupting an external MCU when a change of status is detected by the MC145572. Figure 5–13 shows pin configurations to operate the MC145572 in MCU mode using the PCP for access to the register set.



NOTE: In LT mode, the 10 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 5–13. MCU Mode with PCP Configuration

5.3.2.1 PCP NIBBLE REGISTER OPERATION

Data is written to a nibble register using a single PCP write operation. The 8–bit data word must contain the register address, write bit cleared to 0, and the data to be written as shown in Figure 5–14.

Data is read from a nibble register by first writing the nibble register address with the read indicator bit set to a 1 to the parallel data port. Next, the parallel data port is read and data from the register pointed to by the previous write operation appears on bits 0 through 3 of the port. See Figure 5–15. When NR0 through NR5 are read, software should AND the data read with $0F.

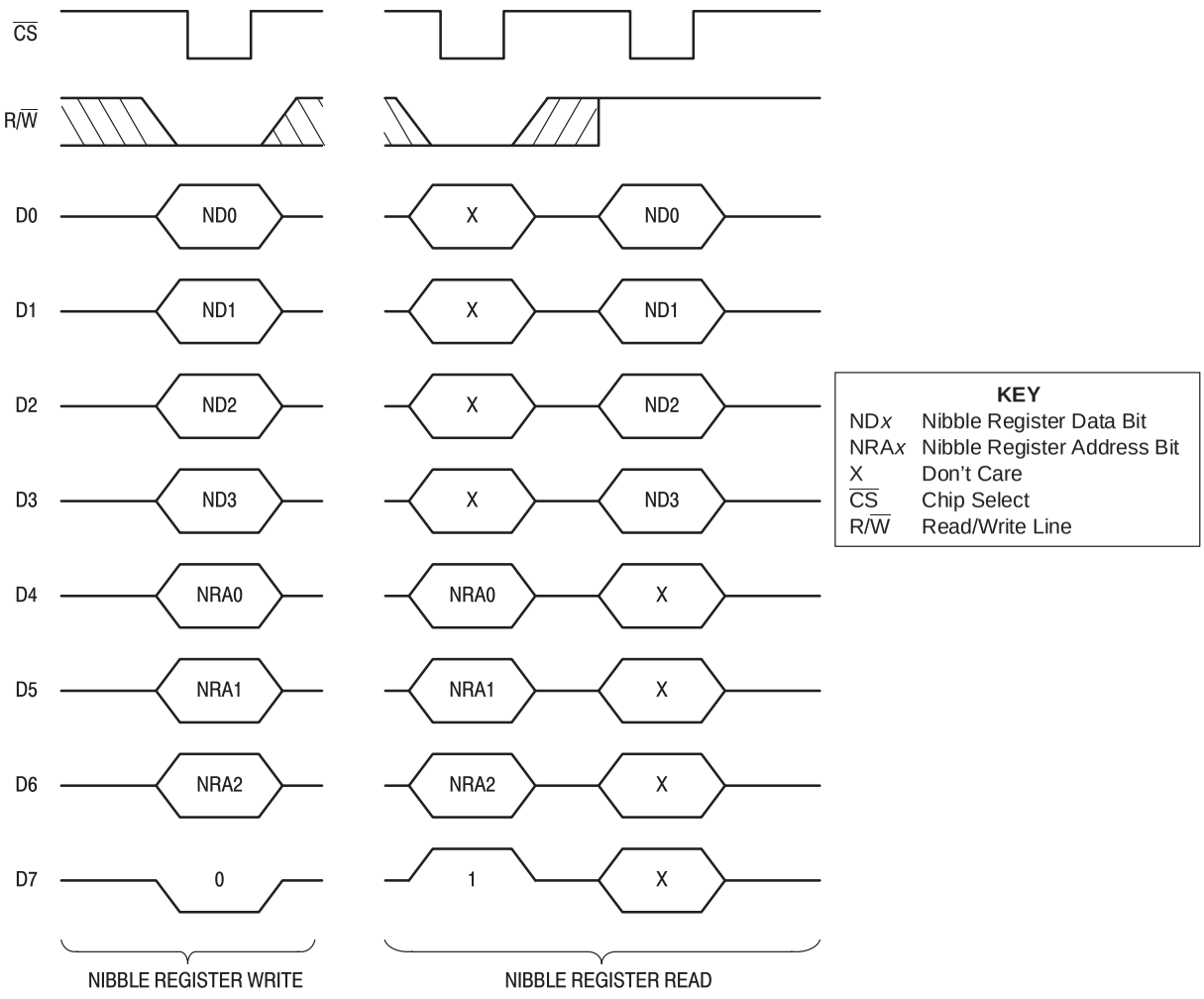


Figure 5–14. PCP Mode Nibble Register Write and Read Operations

5.3.2.2 PCP REGISTER R6 OPERATION

Data is written to Register R6, the eoc register, by writing two successive bytes to the PCP. The first byte must contain the register address, write bit cleared to 0, and the most significant four bits of data to be written, as shown in Figure 5–15.

Data is read from Register R6 by first writing a data byte containing the read/write indicator bit set to a 1 and the register address to the PCP. The data is then read from the PCP by reading two bytes. The first byte contains the most significant four bits of data in bits D3:D0. The next byte contains the low order byte of data. See Figure 5–15.

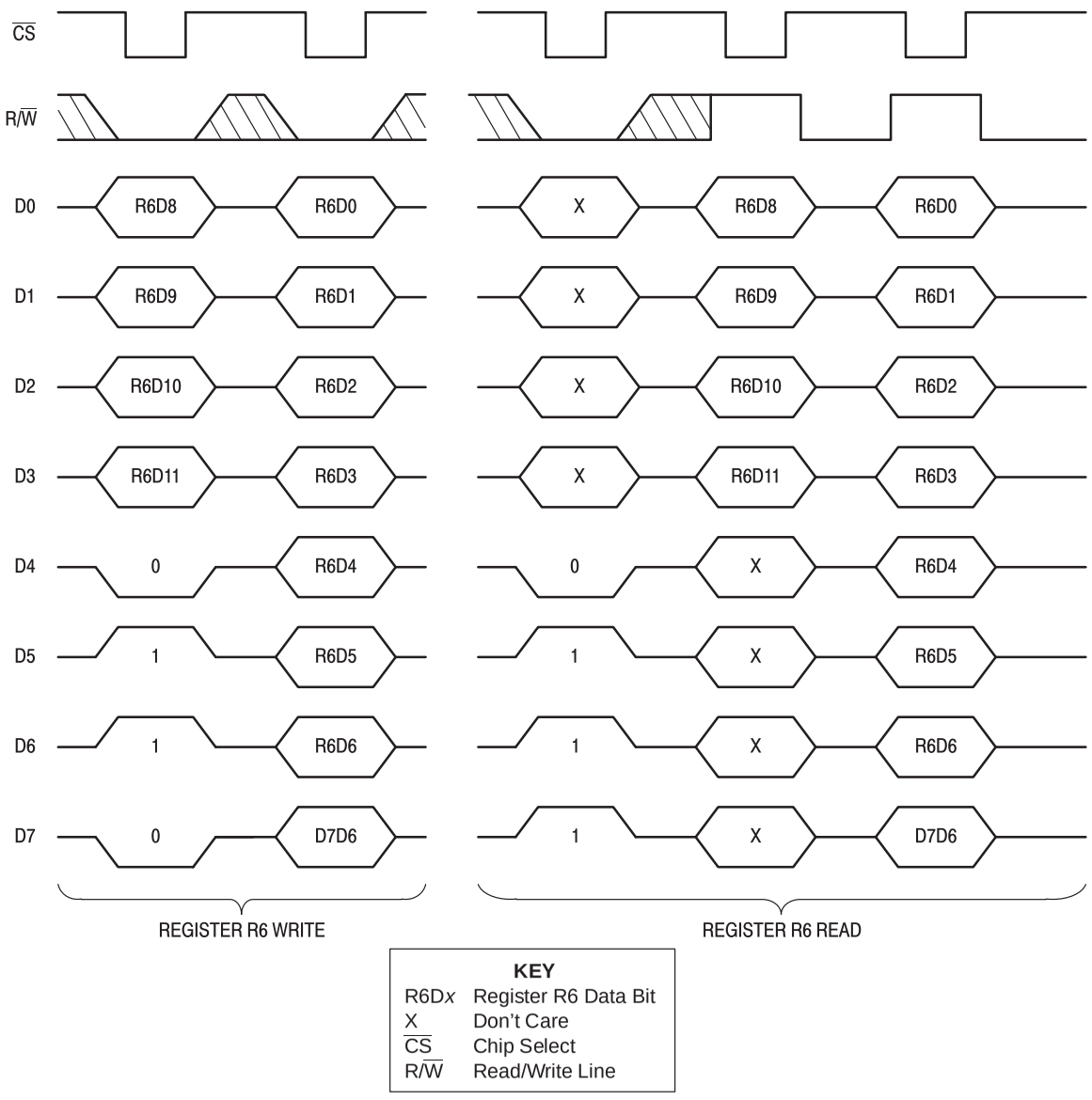


Figure 5–15. PCP Register R6 Write and Read Operations

5.3.2.3 PCP BYTE REGISTER OPERATION

Data is written to a byte register by writing two successive bytes to the PCP. The first byte must contain the register address, write bit cleared to 0, and the address of the byte register. The second byte contains the actual data to be written to the selected byte register (see Figure 5–16).

Data is read from a byte register by writing the pointer byte to the PCP, followed by a read of the selected byte register from the PCP. The first byte must contain the register address, write bit set to 1, and the address of the byte register. This is followed by a read cycle to obtain the contents of the selected byte register (see Figure 5–16).

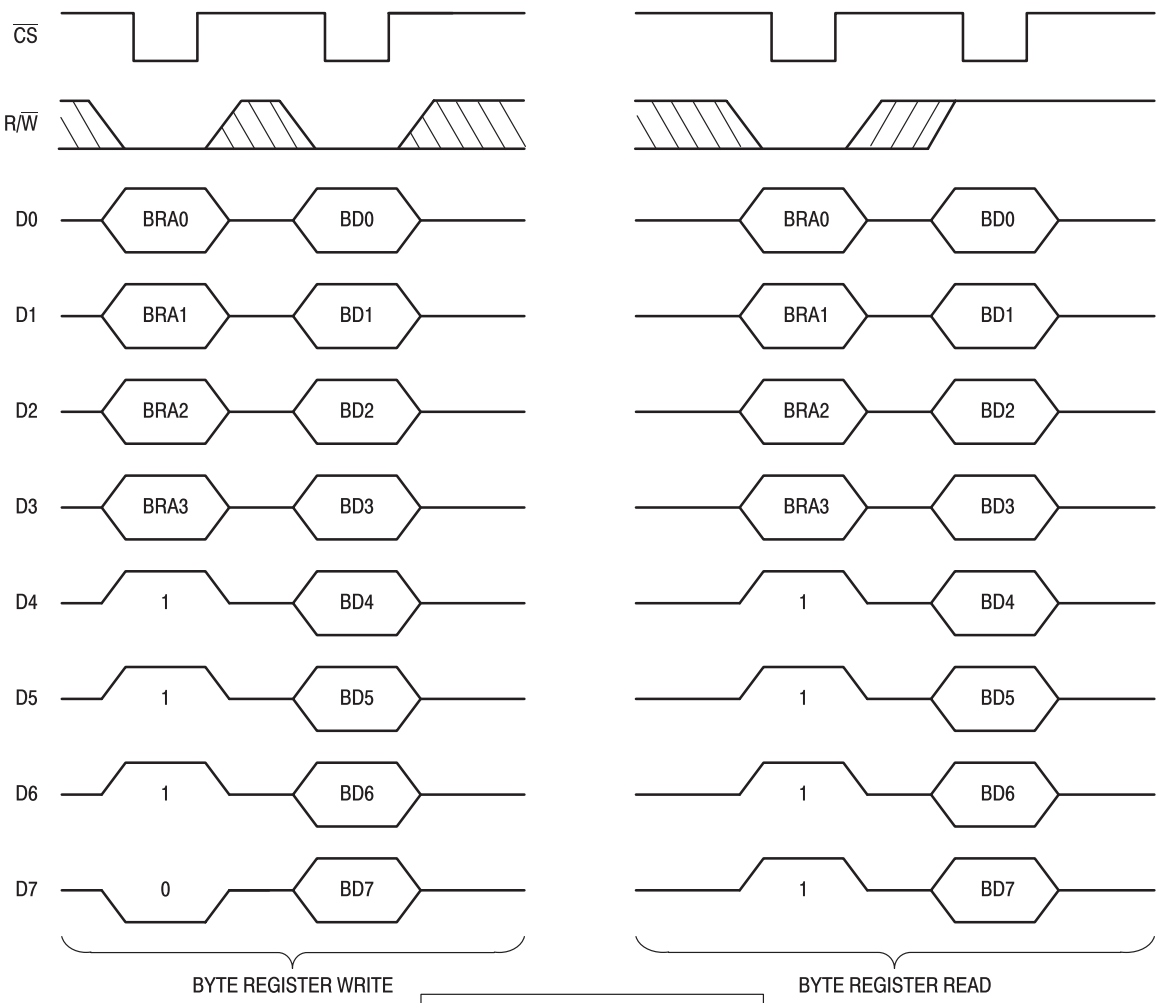


Figure 5–16. PCP Byte Register Write Operation

5.4 IDL2 TIME DIVISION BUS INTERFACE

The IDL2 interface consists of six pins: M/$\overline{S}$, FSX, FSR, DCL, D_{in}, and D_{out}. With the M/$\overline{S}$ pin, the IDL2 interface can be configured as a timing master (FSR, FSX, and DCL are outputs) or a timing slave (FSR, FSX, and DCL are inputs). The master or slave configuration is independent of NT or LT mode selection. The IDL2 interface receives 2B+D data on the D_{in} pin and buffers it through a FIFO to the U–interface Superframe Framer. Simultaneously, this block accepts 2B+D data from the U–interface Superframe Deframer, buffers it through a FIFO, and transmits it out the D_{out} pin. Refer to Figure 5–1 for a block diagram of the MC145572.

After a hardware or software reset, the MC145572 IDL2 interface is configured for short frame operation. Short frame format is compatible with the IDL interface timing used on the MC145472 U–interface transceiver. Table 5–3 details how to configure the MC145572 for the different IDL2 interface data formats. In both short frame and long frame formats, two frame sync signals are available: FSX and FSR. In GCI 2B+D data format, a single frame sync, FSC, is available.

The 2B+D data is transferred over IDL2 interface at an 8 kHz rate. Each IDL2 2B+D frame contains eight bits of B1 channel data, eight bits of B2 channel data, and two bits of D channel data. The IDL2 interface supports five different frame formats and a timeslot assigner. The frame formats are long frame and short frame synchronization, each with either 8– or 10–bit 2B+D data formats. The fifth frame format is the IDL2 GCI electrical frame format. In this format, only the 2B+D data bits of the GCI interface are accessible by MC145572. Either SCP or PCP must be used for access to the internal register set of MC145572 when IDL2 operation is enabled.

As a master, the IDL2 interface of MC145572 can be configured to output 512 kHz, 2.048 MHz, or 2.56 MHz clock rates at the DCL pin. Table 5–4 is a guide to IDL2 clock rate selection. These data rates apply to all IDL2 frame formats, including the GCI 2B+D data format. Please note that when configured for GCI electrical operation, the data rate is one–half the DCL clock rate.

As a slave, the IDL2 interface of MC145572 accepts clock rates from 256 kHz to 4.096 MHz at the DCL pin.

A separate D channel port is available when configured for MCU SCP operation.

Table 5–3. IDL2 Interface Data Format Selection

IDL2 Data Format	OR6 (b3)	OR7 (b3)	BR7 (b0)	Available Frame Syncs	D Channel Port Available	Comments
IDL2 Short Frame Format 10–Bit Frame Size (MC145472 Compatible)	0	0	0	FSX, FSR	Yes	Default after hardware or software reset
IDL2 Short Frame Format 8–Bit Frame Size (MC145472 Compatible)	0	0	1	FSX, FSR	Yes	
IDL2 Long Frame Format 10–Bit Frame Size	0	1	0	FSX, FSR	No	
IDL2 Long Frame Format 8–Bit Frame Size	0	1	1	FSX, FSR	No	
GCI 2B+D Frame Format	1	0	0	FSC	Yes	

NOTE: The timeslot assigner is enabled when one or more of OR6(b7 or b6 or b5) are set to a 1. Enabling the timeslot assigner overrides all other IDL2 frame formats.

Table 5–4. IDL2 Interface Master Mode Clock Rate Selection

Clock Rate	OR7(b4)	BR7(b2)
2.56 MHz	0	0
2.048 MHz	0	1
512 kHz	1	X

5.4.1 Short Frame Operation

Short frame operation is the same as the IDL interface used on the MC145472 and MC14LC5472 U–interface transceivers with one exception. The MC145572 provides for two 8 kHz frame sync pins, FSX and FSR, when operated in IDL2 mode. The FSX pin is used to indicate IDL2 frame synchronization for data input into the D_{in} pin for transmission onto the U–interface. The FSR pin is used to indicate IDL2 frame synchronization for data recovered from the U–interface and output to the D_{out} pin. When configured for Master mode, the MC145572 drives FSR and FSX, simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In Slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

Figures 5–17 and 5–18 show typical data formats for short frame operation as a master and configured for 8– and 10–bit frame formats, respectively. Figures 5–19 and 5–20 show typical data formats for IDL2 operation as a slave and configured for 8– and 10–bit frame formats, respectively.

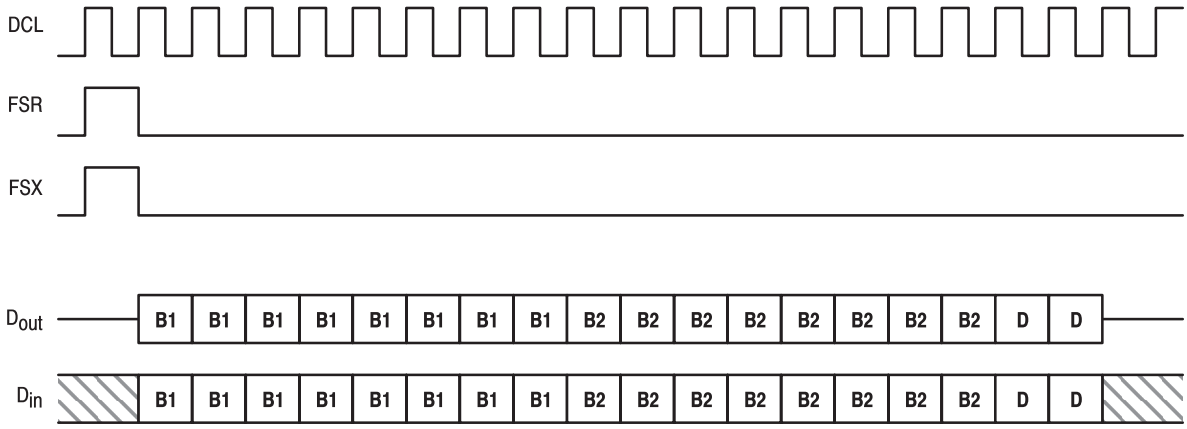


Figure 5–17. IDL2 Interface Timing in Short Frame Master Mode, 8–Bit Frames

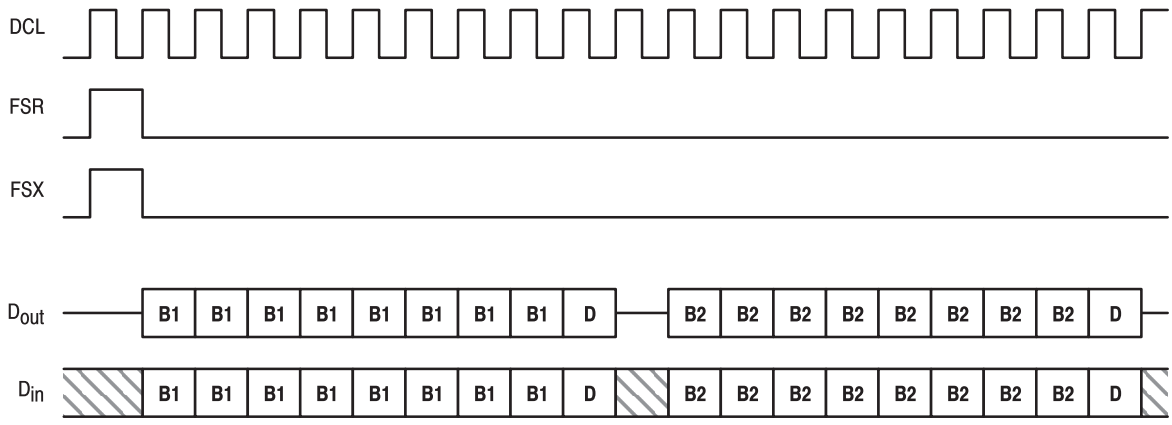


Figure 5–18. IDL2 Interface Timing in Short Frame Master Mode, 10–Bit Frames

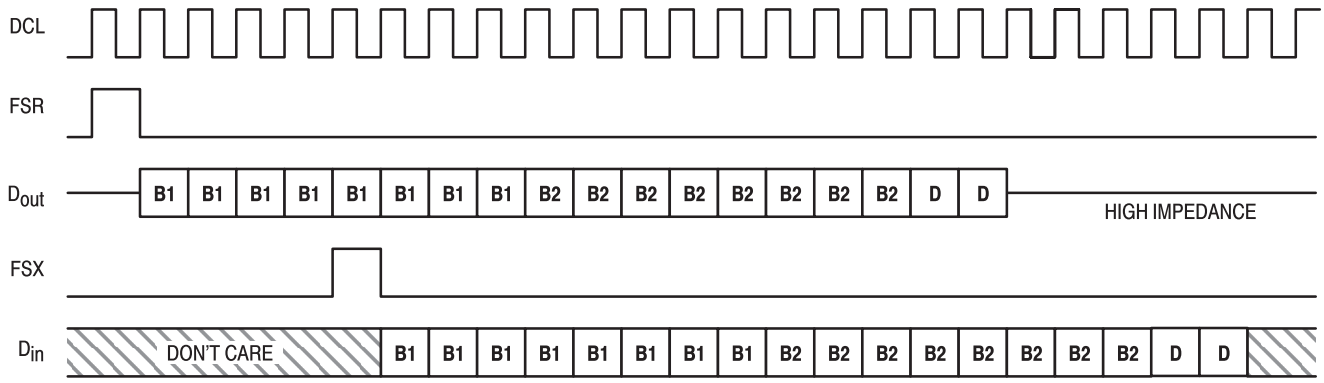


Figure 5–19. IDL2 Interface Timing in Short Frame Slave Mode, 8–Bit Frames

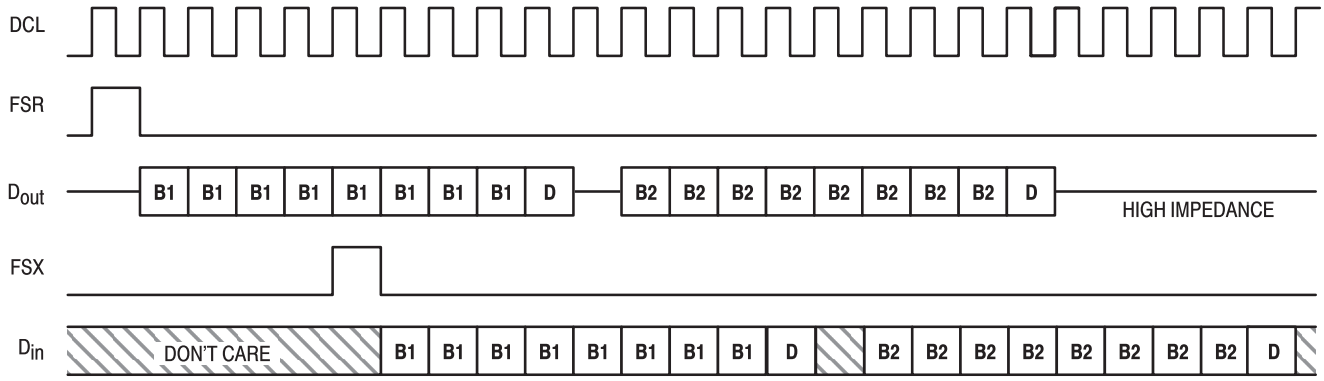


Figure 5–20. IDL2 Interface Timing in Short Frame Slave Mode, 10–Bit Frames

5.4.2 Long Frame Operation

When configured for long frame mode, the 8 kHz frame sync is active during the 2B+D data transfer. The FSX pin is used to indicate frame synchronization for data input into the D_{in} pin for transmission onto the U–interface. The FSR pin is used to indicate frame synchronization for data recovered from the U–interface and output to the D_{out} pin. When configured for Master mode, the MC145572 drives FSR and FSX simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In Slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

Figures 5–21a and 5–22a show typical data formats for long frame operation as a master and configured for 8–bit and 10–bit frame formats, respectively. Figures 5–21b and 5–22b show typical data formats for long frame operation as a slave and configured for 8–bit and 10–bit frame formats, respectively.

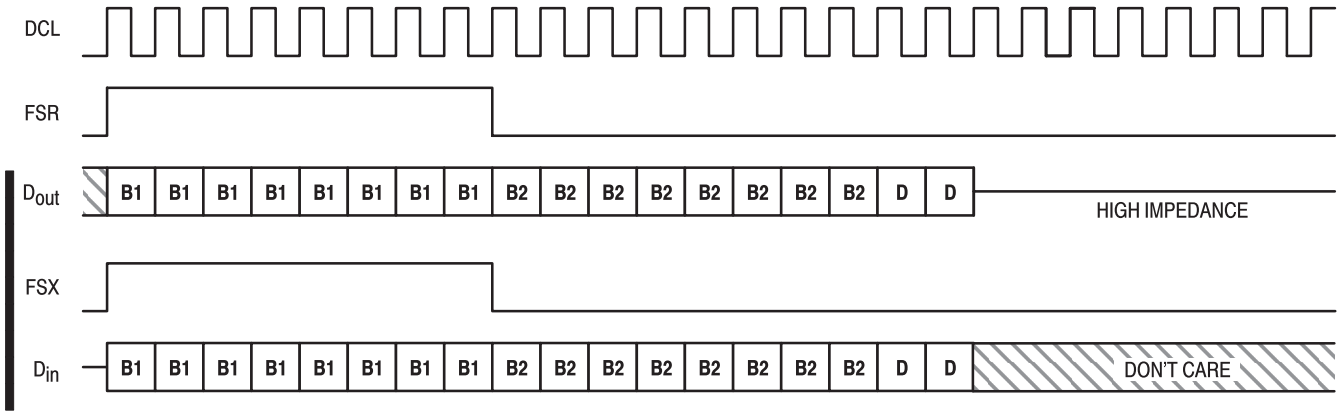


Figure 5–21a. 8–Bit Mode, Master

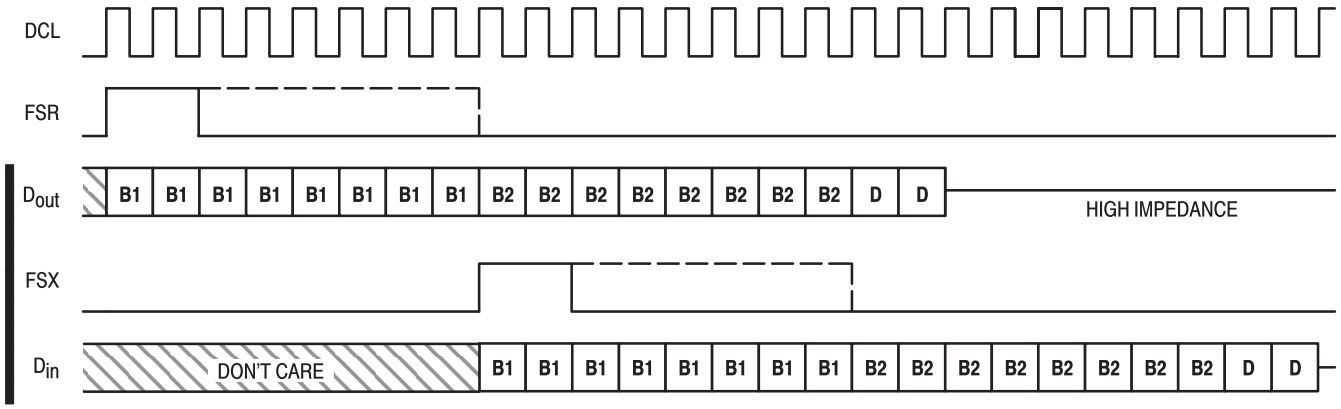


Figure 5–21b. 8–Bit Mode, Slave

Figure 5–21. IDL2 Interface Timing in Long Frame, 8–Bit Frames

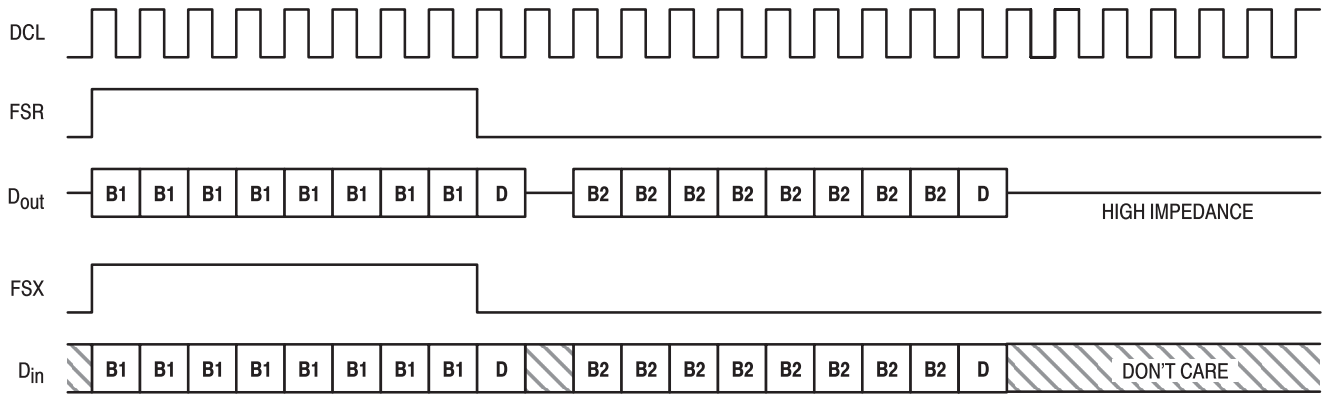


Figure 5–22a. 10–Bit Mode, Master

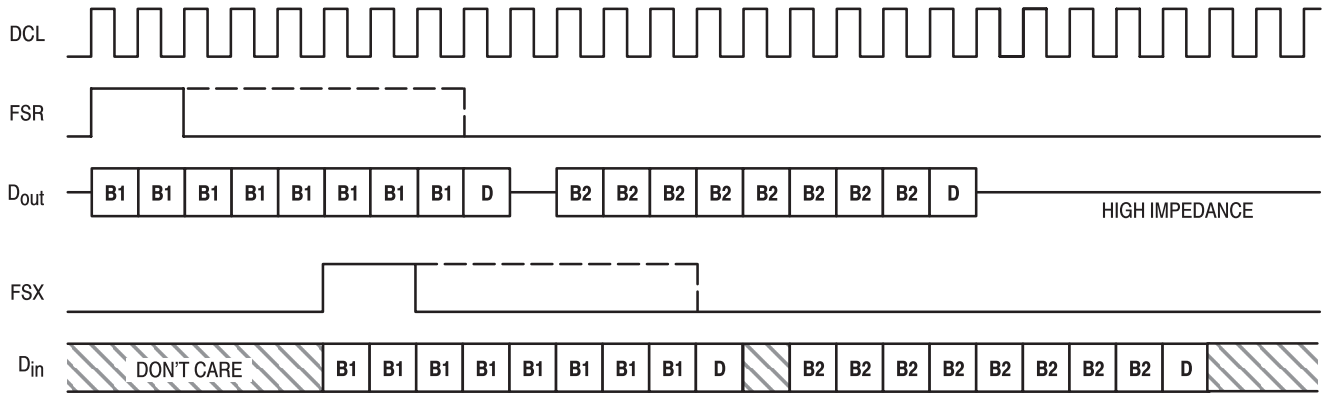


Figure 5–22b. 10–Bit Mode, Slave

Figure 5–22. IDL2 Interface Timing in Long Frame, 10–Bit Frames

5.4.3 GCI 2B+D Operation

By setting OR6(b3), GCI Mode Enable to a 1, the IDL2 interface is configured to accept GCI interface timing. In this mode, only 2B+D data is transferred between MC145572 and GCI interface. The other bits in the GCI frame are ignored. Four signal pins are available in this mode: DCL, FSC, D_{in}, and D_{out}. Control and status information for MC145572 is provided through SCP or PCP. DCL is a 2X bit clock, D_{in} accepts data from the IDL2 interface to be transmitted onto the U–interface, D_{out} transmits data received from the U–interface onto the IDL2 interface, and FSC is the 8 kHz frame synchronization pulse. D_{out} is driven only when 2B+D data is output from MC145572. During all other bit times of the GCI frame, D_{out} is high impedance. For applications having a multiplexed GCI frame structure, Overlay register OR5 bits 2:0 are used to program the active GCI channel in the multiplex.

Figure 5–23 shows the GCI data format that is transferred over the IDL2 interface. See **Chapter 8** for more details, if an application requires full GCI capability.

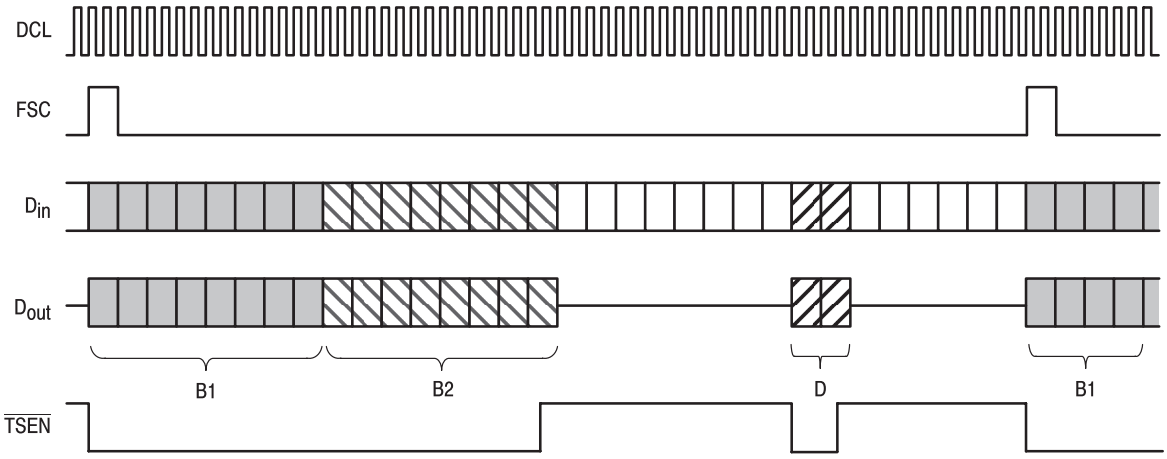


Figure 5–23. IDL2 GCI 2B+D Data Formats

5.4.4 Master and Slave Mode Operation

The MC145572 can be configured for IDL2 master or IDL2 slave operation independently of LT or NT configuration. A logic 1 selects IDL2 master operation and a logic 0 selects IDL2 slave operation.

When configured as an IDL2 slave, FSX and FSR can be independently driven by external circuitry. FSX and FSR must be synchronized to the clock applied to DCL. If there is only a single synchronization source, the FSR and FSX pins can be tied together and driven from a single source. In Slave mode, the IDL2 interface can accept an input clock at DCL between 512 kHz and 8.192 MHz.

As an IDL2 master, MC145572 drives FSX and FSR simultaneously, so that the active high time of each signal coincides with each other. The 2B+D data transfer into D_{in} and out of D_{out} occurs simultaneously. For applications where only one output synchronization pulse is required, either FSX or FSR can be used. As an IDL2 master, MC145572 outputs data clocks of 512 kHz, 2.048 MHz, and 2.56 MHz. The DCL clock rate is programmed by BR7(b2) and OR7(b4). See Table 5–4.

5.4.5 D Channel Port

When operated in MCU mode with SCP enabled, MC145572 can be configured to have a separate data port for D channel data. The D channel port is available for short frame data format and GCI 2B+D data format. When PCP is used to access the MC145572 register set, the D channel port is not available, since the pins are assigned to the data bus of the parallel port. The D channel port is enabled by setting OR8(b0), D Channel Port Enable, to a 1. After a hardware or software reset, the D channel port is disabled. Figure 5–2 shows an LT mode configuration with D channel port enabled.

The D channel port has three signals: DCH_{in} (D channel data input), DCH_{out} (D channel data output), and DCHCLK (D channel clock). When the D channel port is enabled, DCHCLK is always a clock output. The clock is a gated clock, based on whatever is on DCL. The clock occurs whenever the normal D1 and D2 bits would have occurred during the transfer taking place over D_{out} with respect to FSR. Internal buffering of the data received on DCH_{in} aligns the data for transmission onto the U–interface. DCH_{out} does not go high impedance.

When the D channel port is enabled, D channel bits are diverted to the port, and the D_{out} pin on the IDL2 interface is high impedance during the D bit times. Data bits received at IDL2 interface D_{in} pin are ignored during the D channel bit times. In timeslot assigner mode, D channel bits are transferred at the time programmed in register OR2, D_{out} D Channel Timeslot bits. Figures 5–24 through 5–26 show the D channel port timing.

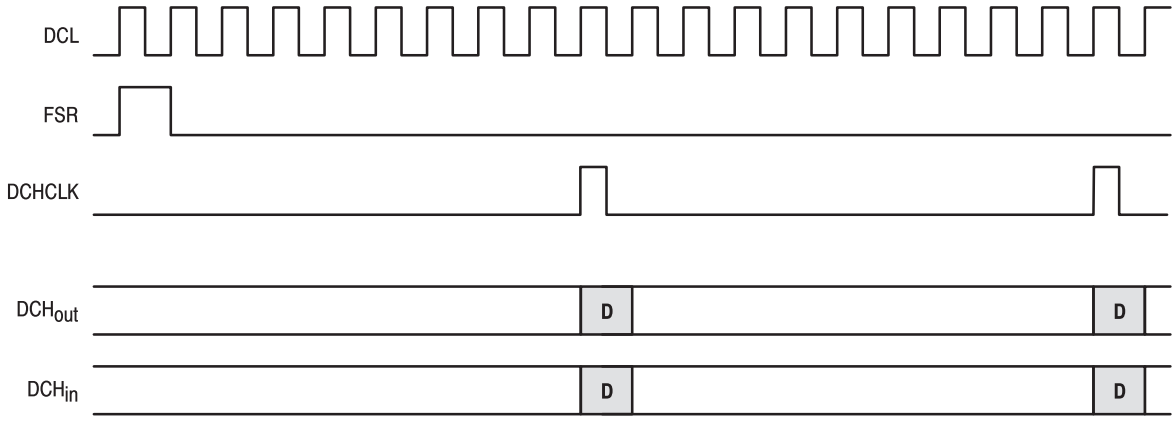


Figure 5–24. D Channel Port Timing, IDL2 10–Bit Frames

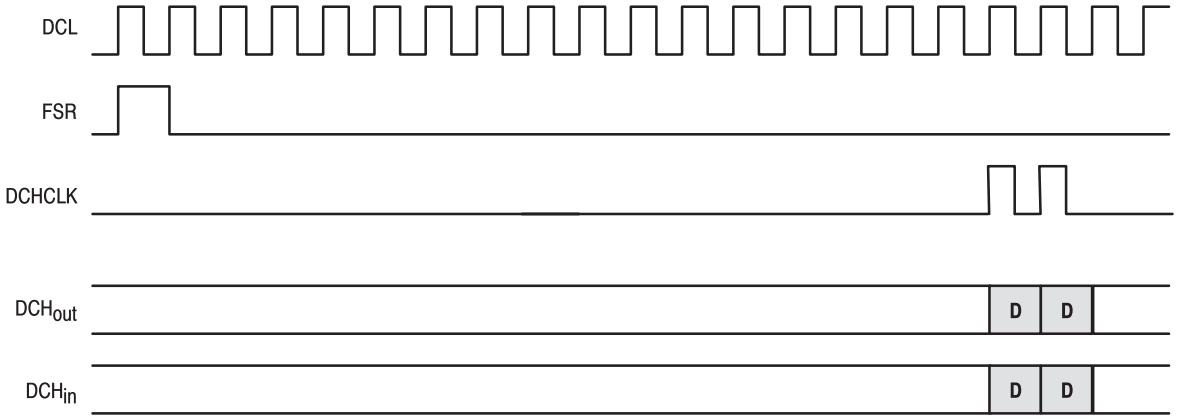


Figure 5–25. D Channel Port Timing, IDL2 8–Bit Frames

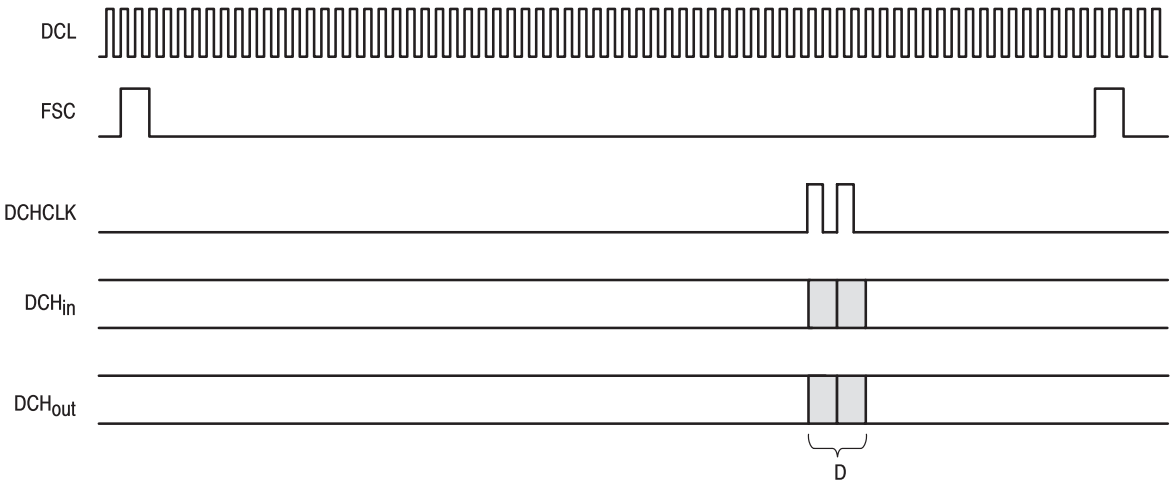


Figure 5–26. D Channel Port Timing, IDL2 GCI 2B+D Frames

5.4.6 Timeslot Assigner

The MC145572 has a timeslot assigner that can be used when configured for MCU mode. The timeslot assigner is enabled when one or more of OR6(b7, b6, or b5) are set to a 1. The starting timeslot(s) are programmed into Overlay registers OR0 – OR5. The B1, B2, and D channels are each independently programmable for both transmit and receive directions.

Timeslots are each two DCL clocks wide. Timeslot numbering starts from timeslot 0. Timeslot 0 occurs during the first two DCL clocks following FSX or FSR. DCL clocks are numbered starting from 0. Clock number 0 is the first DCL clock after the frame sync pulse FSX or FSR. Since FSX and FSR can occur at different times, DCL clocks are counted referenced to either FSX or FSR depending on which data direction is being configured. The timeslot number is calculated by counting the DCL clocks after the appropriate frame sync where it is desired to place the start of the B or D channel timeslot. This DCL count is divided by two and the resulting value is written to the appropriate timeslot register.

The D channel data is always two contiguous DCL clocks or one timeslot in duration. B channel data is always eight contiguous DCL clocks or four timeslots in duration. B channel timeslots may be programmed to start in any timeslot, though in normal applications, B channel timeslots are programmed to start on every fourth timeslot or eighth DCL clock. Data is transferred between MC145572 and the IDL2 interface only during B1, B2, or D channel timeslots that are enabled. When a B or D channel timeslot is disabled, data appearing at the D_{in} pin is ignored and the D_{out} pin is high impedance. Table 5–5 details the timeslot assigner registers in the overlay register set. See Figures 5–27 and 5–28 for timeslot format examples.

The register programming for Figure 5–27 is as follows:

OR0 = $04	OR3 = $00	OR6 = $E0
OR1 = $0B	OR4 = $08	OR7 = $20
OR2 = $01	OR5 = $0D	OR8 = $08

The register programming for Figure 5–28 is as follows:

OR0 = $00	OR6 = $50
OR2 = $0D	OR7 = $20
OR3 = $04	OR8 = $08
OR5 = $01	

The register programming for Figure 5–29 is as follows:

OR0 = $00	OR3 = $00	OR6 = $E0
OR1 = $0B	OR4 = $0B	OR7 = $00
OR2 = $08	OR5 = $08	OR8 = $09

Enabling the timeslot assigner overrides all other IDL2 frame formats with the exception of GCI 2B+D. In GCI 2B+D data format, OR5 bits 2:0 are used to select the active GCI channel.

When the D channel port is enabled, the corresponding D channel timeslot is not enabled on the IDL2 interface. Instead, the D channel data is transferred over the D channel port referenced to FSR as programmed in Overlay registers OR2 or OR5. This is also true when IDL2 GCI 2B+D mode has been enabled. The D_{out} pin of the IDL2 interface is high impedance and data at D_{in} is ignored. Figure 5–29 gives an example of D channel port operation when the timeslot assigner is enabled.

Table 5–5. Timeslot Assigner Registers

OR0	D_{out} B1 Channel Timeslot Bits (7:0)							
OR1	D_{out} B2 Channel Timeslot Bits (7:0)							
OR2	D_{out} D Channel Timeslot Bits (7:0)							
OR3	D_{in} B1 Channel Timeslot Bits (7:0)							
OR4	D_{in} B2 Channel Timeslot Bits (7:0)							
OR5	D_{in} D Channel Timeslot Bits (7:0) and GCI Slot (2:0)							
OR6	TSA B1 Enable	TSA B2 Enable	TSA D Enable	GCI Select M4 – BR0	GCI Mode Enable	Reserved	Reserved	Reserved

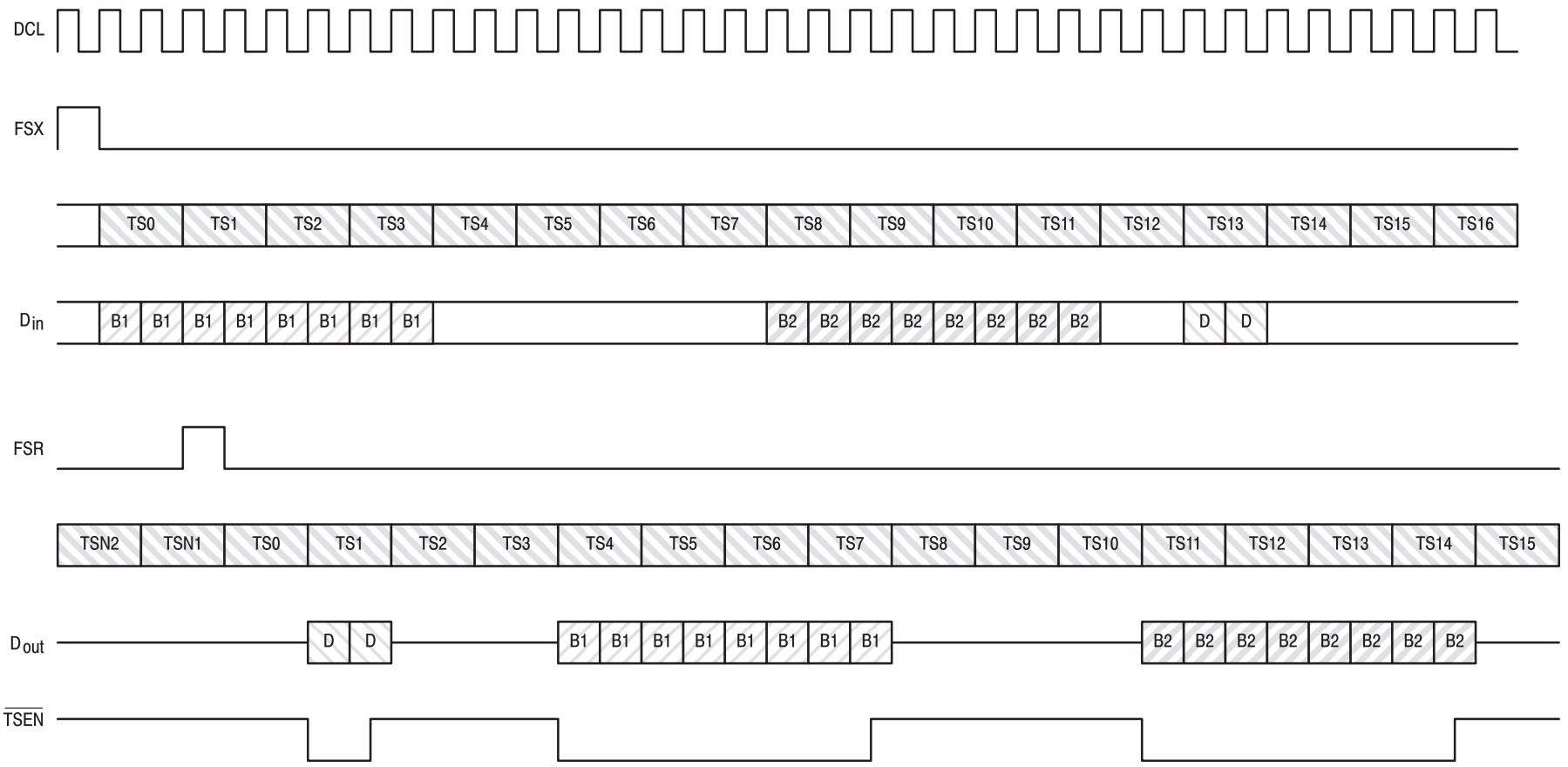


Figure 5–27. Timeslot Assigner Data Format Example

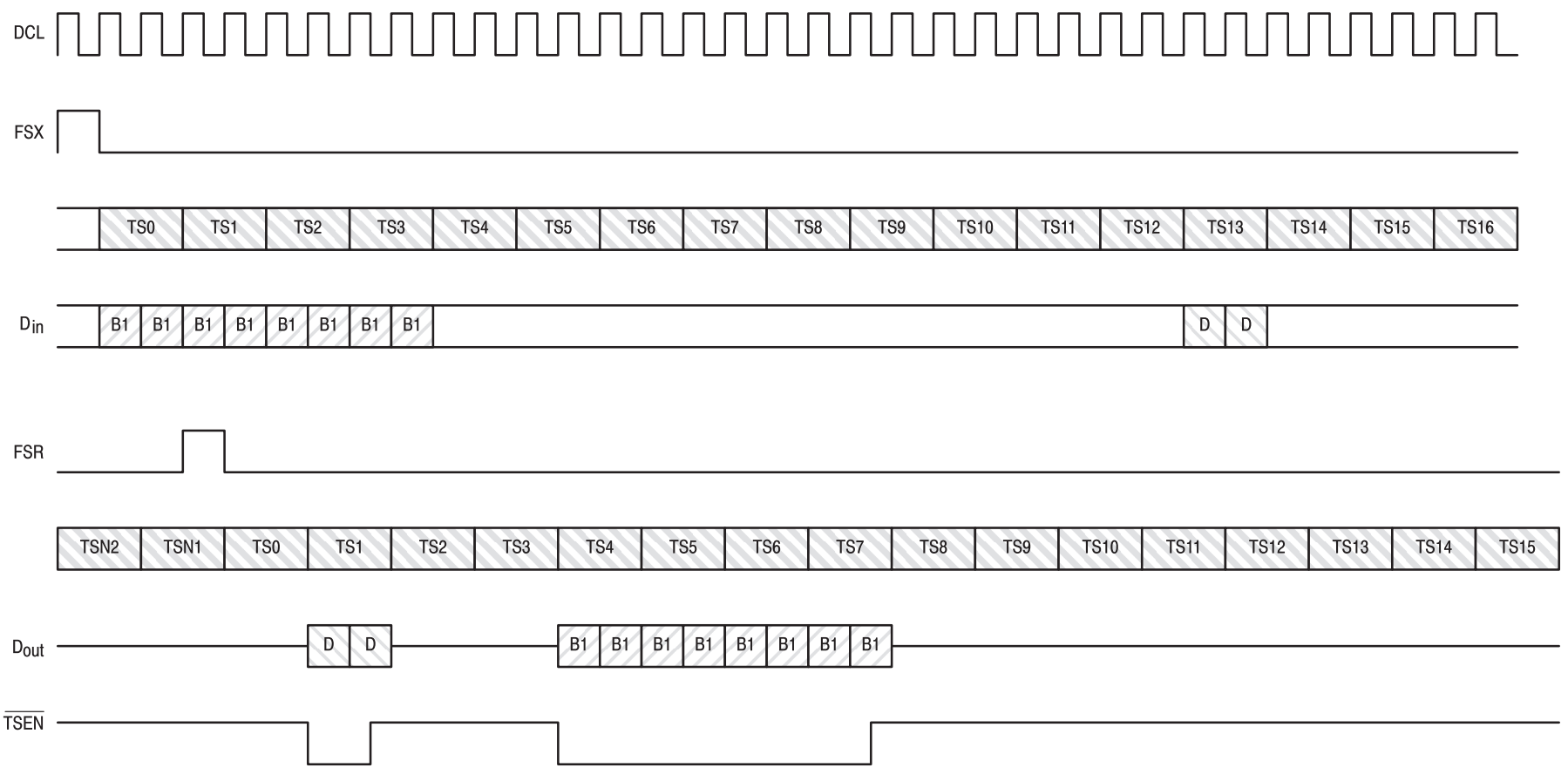


Figure 5–28. Timeslot Assigner Data Format Example, B2 Channel Not Enabled

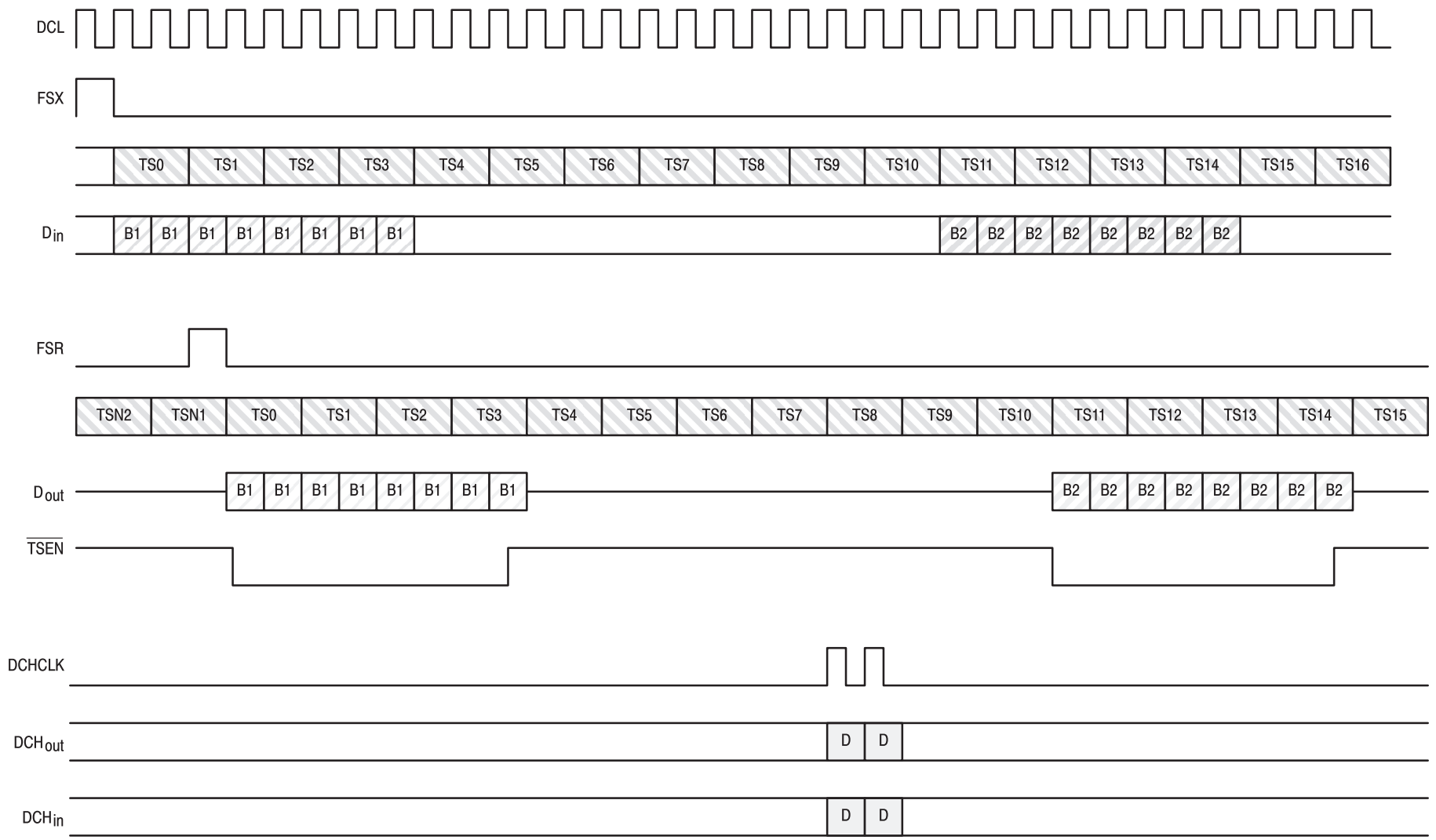


Figure 5–29. Timeslot Assigner Example with D Channel Port Enabled

NOTE: D Channel is in TS8 referenced to FSR.

5.4.7 Timeslot Selection

The MC145572, operating at a DCL clock of 4.096 MHz, allows up to 256 start times for data channels (see Table 5–6). Timeslot 0 starts immediately following the FSX/FSR pulse. Timeslot 1 is two DCL pulses later, counted from the rising edge.

Table 5–6. Maximum Number of Timeslots vs DCL Frequency

DCL Frequency	Max Timeslot (Hex)	Max Timeslot (Decimal)
4.096 MHz	$FF	255
2.56 MHz	$9F	159
2.048 MHz	$7F	127
512 kHz	$1F	31

Figure 5–30 shows the relationship of the FSR and FSX pulses, DCL, and timeslot locations. Each timeslot is on a two clock boundary, and is named TS0 to TS*n* – 1, where *n* is the maximum number of timeslots for the current operating data clock. A B channel occupies four contiguous 2–bit timeslots. A D channel occupies a single 2–bit timeslot.

The following formula calculates the maximum number of timeslots for other values of DCL frequency.

$$\frac{f_{DCL}}{16\ kHz} = \text{Maximum Number of Timeslots}$$

B and D channel registers are programmed with the following formula.

B Register Value = TS*x*

D Register Value = TS*x*

where the *x* of TS*x* is the value programmed into a register. All numbers are programmed in hex. Any B channel must be assigned to a timeslot at or before TS*n* – 4. Where TS*n* – 1 is the maximum timeslot number for the current operating data clock. The three timeslots following any B channel assignment are reserved for that B channel and may not be assigned to any other data channel.

Registers OR0 – OR5 are programmed in the above fashion.

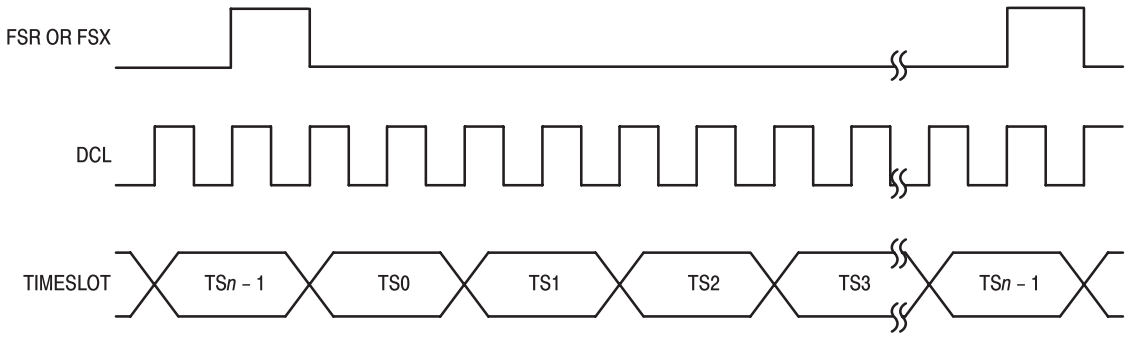


Figure 5–30. Timeslot Numbering

NOTE

If timeslot assignment mode is enabled via OR6 b(7), b(6), or b(5), then the IDL2 8/10 control bit is ignored and B channel and D channel data is placed according to OR0 – OR5. The $\overline{\text{TSEN}}$ function is available when the timeslot assigner is enabled.

5.4.8 IDL2 2B+D Data Alignment to U-Interface Superframe

The MC145572 provides signals that indicate the relationship between data transferred over the IDL2 interface and where that data is positioned in the U–interface superframe. In IDL2 short frame and long frame operation, the SFAX and SFAR pins are used to indicate the IDL2 2B+D data frame that corresponds to the first 2B+D block in basic frame 1 of the U–interface superframe. This feature is enabled by setting OR8(b1), SFAX/SFAR ENABLE to a 1 when the MC145572 is configured for IDL2 operation.

SFAX provides superframe alignment timing for data transmitted onto the U–interface. It is active during the IDL2 frame that corresponds to the 2B+D data transmitted at the start of basic frame 1 on the U–interface. In NT mode, SFAX is always an output. In LT mode, SFAX defaults to an input and is used to force alignment of the outgoing superframe, as well as indicating transfer of the first 2B+D frame of U–interface basic frame 1 into D_{in} of the IDL2 interface. When in LT mode, setting OR8(b5), SFAX Output Enable to a 1, configures SFAX as an output and indicates transfer of the first 2B+D frame of U–interface basic frame 1 into D_{in} of the IDL2 interface. When SFAX is not enabled as an input, the MC145572 selects the starting point of the transmitted superframe when in LT mode.

SFAR provides superframe alignment timing for data received from the U–interface. It is active during the IDL2 frame that outputs 2B+D data from the MC145572 that arrived at the start of basic frame 1 on the U–interface. SFAR is always an output when enabled.

When configured for GCI 2B+D operation, the FSC signal is used to indicate superframe alignment.

The superframe alignment signal(s) occur once every 96 IDL2 or GCI frames. Since frames are 125 μs in duration, this corresponds to 12 ms (96 x 125 μs), which is the duration of a U–interface superframe.

5.4.8.1 IDL2 SHORT FRAME MODE SUPERFRAME ALIGNMENT

In IDL2 short frame format, SFAX and SFAR indicate the IDL2 frame corresponding to the first 2B+D block in the U–interface superframe by pulsing high for one DCL clock time. This occurs immediately following the IDL2 frame syncs FSX and FSR (see Figures 5–31a and 5–32a). When configured as an input, SFAX must be driven high for the DCL clock period immediately following FSX and it is sampled on the falling edge of DCL.

5.4.8.2 IDL2 LONG FRAME MODE SUPERFRAME ALIGNMENT

In IDL2 long frame format, SFAX and SFAR indicate the IDL2 frame corresponding to the first 2B+D block in the U–interface superframe by pulsing high for the duration of FSX and FSR, respectively (see Figures 5–31b and 5–32b).

5.4.8.3 GCI 2B+D MODE SUPERFRAME ALIGNMENT

When configured for IDL2 GCI 2B+D data format, OR6(b3) = 1, the MC145572 uses the FSC signal to indicate superframe alignment. Inputs on SFAX are ignored.

In LT mode, when MC145572 is configured as an IDL2 slave, the FSC pin is used to force alignment of the transmitted U–interface superframe. Normally, the FSC pulse is two DCL clocks in duration. The transmit superframe alignment is set by driving FSC with a one DCL clock wide pulse once every 96 GCI frames. The 2B+D data read into the D_{in} pin, corresponding to the single clock wide FSC, is the first 2B+D frame transmitted onto the U–interface. If superframe alignment is not input to FSC, the MC145572 aligns the outgoing U–interface superframe alignment (see Figure 5–33).

When configured for Master mode and either LT or NT operation, reception of the first 2B+D data of the U–interface superframe is indicated by outputting a FSC pulse that is one DCL clock wide. This happens once every 96 GCI frames.

Figure 5–31a. Short Frame Mode

NOTE: The #1 (circled) indicates which 2B+D transfer is the first of the superframe. The clock, DCL, is continuous.

Figure 31b. Long Frame Mode

Figure 5–31. SFAR Timing

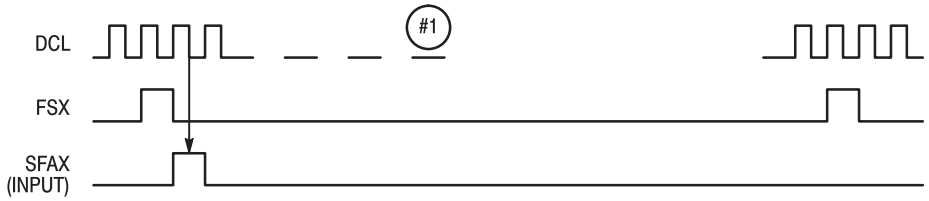
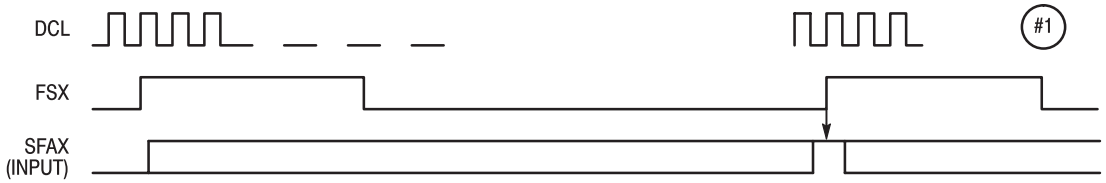


Figure 5–32a. Short Frame Mode



NOTE: The #1 (circled) indicates which 2B+D transfer is the first of the superframe. The clock, DCL, is continuous.

Figure 5–32b. Long Frame Mode

Figure 5–32. SFAX Timing

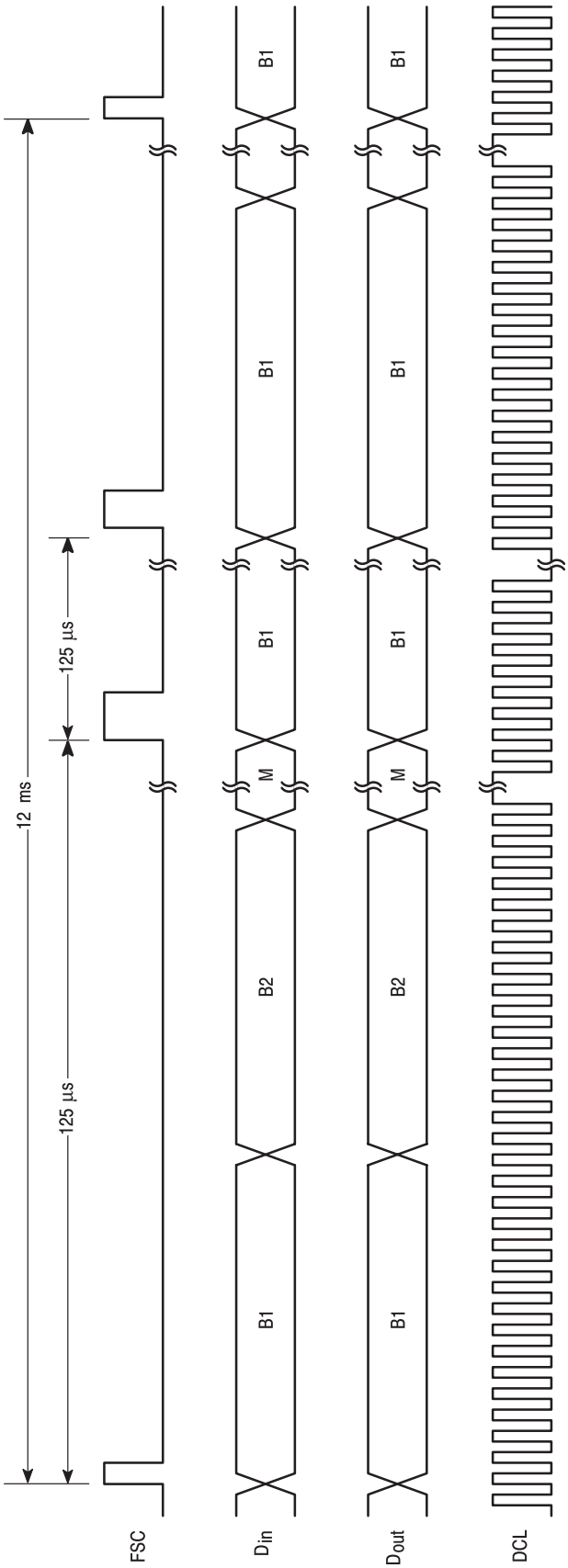


Figure 5–33. IDL2 GCI 2B+D Format Superframe Alignment Signal

In NT mode, IDL2 slave operation, any superframe alignment information that may be present on FSC is ignored. ANSI T1.601 defines a 60 ± 2 baud turnaround at the NT. This means that the transmitted Superframe Sync word in the NT–configured MC145572 is delayed 60 bauds or 750 µs from the received Superframe Sync word. On an 18,000–foot loop, the total propagation delay in both directions is approximately 6 bauds or 39 µs. This gives a worse case offset between the transmitted sync word at LT and the receive sync word at NT of approximately 790 µs or 6 IDL frames.

5.4.9 Initial State of B1 and B2 Channels

Upon initial activation, MC145572 transmits all 1s in the B and D channels onto the U–interface. Data transparency is enabled by setting Customer Enable (NR2(b0)), when the M4 channel `act` bit is received as a 1. If the Verified `act/dea` mode is enabled, see BR9(b5,b4), then data transparency onto the U–interface is automatically enabled when the M4 channel `act` bit is received as a 1.

5.5 FRAME SYNC TO U-INTERFACE PROPAGATION DELAYS

Due to the MC145572 having separate FIFOs for receive and transmit directions, there is a propagation delay between data being input into the IDL2 or GCI interfaces and that same data being transmitted onto the U–interface. Likewise, there is a delay between when data is received at the U–interface and is transmitted onto the IDL2 or GCI interfaces. Table 5–7 gives the minimum and maximum delays for both NT and LT modes of operation. For any given activation, the delay remains fixed, but the propagation delay through the MC145572 will vary from activation to activation.

Table 5–7. FIFO Delays Through the MC145572

Delay Path	Min	Max	Units
NT Mode FSX to U–Interface Transmission Delay	196	315	µs
NT Mode U–Interface to FSR Transmission Delay	281	400	µs
LT Mode FSX to U–Interface Transmission Delay	184	328	µs
LT Mode U–Interface to FSR Transmission Delay	281	400	µs

NOTE

The total end–to–end delay is the sum of the transmit FIFO delay in the originating transceiver and the receive FIFO delay at the destination transceiver.

5.6 LOOPBACKS

The MC145572 U–interface transceiver supports four different loopback types, each having various modes. The four types are: 1) U–Interface Loopback, 2) IDL2 Interface Loopback, 3) Superframe Framer–to–Deframer Loopback, and 4) External Analog Loopback. Each of these loopback modes is selected by setting bits in the appropriate register(s). Any combination of loopbacks may be invoked, including simultaneous loopbacks toward the U–interface and toward the IDL2 interface. These loopbacks are available as transparent or non–transparent. “Transparent” means that a loopback passes the data on through to the other side, as well as looping it back. “Non–transparent” means that the data is blocked from being passed downstream and is replaced with the idle code (all 1s).

5.6.1 U-Interface Loopback

A U–interface loopback configuration is shown in Figure 5–34. As the shaded portion of the block diagram shows, this loopback mode exercises virtually the entire U–interface transceiver. The 2B1Q symbols are received from the far–end transmitter, recovered, passed through the IDL2 interface block, and transmitted back to the far–end receiver.

The four most significant bits of BR6 control the U–interface loopback modes. The loopback occurs in the IDL2 interface section of MC145572. Data appearing at the D_{in} pin is ignored (i.e., not transmitted onto the U–interface). By setting U–Loop Transparent (BR6(b4)), to a 1, the loopback is made transparent and the D_{out} pin is enabled, permitting transfer of recovered data onto the IDL2 interface. When U–Loop Transparent (BR6(b4)), is reset to a 0, the B and D channels at the D_{out} pin are forced to idle 1s when a loopback is enabled. If IDL2 Invert (BR7(b4)) is set to a 1, then the B and D channels at the D_{out} pin idle at all 0s.

The U–interface loopback is selected by setting one or more of U–loop B1, U–loop B2, or U–loop 2B+D (BR6(b7:b5)) to a 1. To enable loopback of B1 channel data to the U–interface, U–loop B1 (BR6(b7)) is set to a 1. To enable loopback of B2 channel data to the U–interface, U–loop B2 (BR6(b6)) is set to a 1. To enable loopback of 2B+D data to the U–interface, U–loop 2B+D (BR6(b5)) is set to a 1. The 2B+D loopback overrides any B1 or B2 channel loopback that has been enabled. When the Automatic eoc Processor in the MC145572 is enabled, the logical OR of loopback modes enabled by the Automatic eoc Processor and loopback modes selected in BR6 are enabled. As a result, the external microcontroller can always enable a loopback whether the U–interface transceiver is operated with the Automatic eoc Processor or not.

When the U–interface transceiver is operating without the Automatic eoc Processor, loopback modes can be disabled by setting to a 1 and then resetting to a 0, the Return to Normal bit, NR0(b0). This clears all bits in BR6 and clears the `crc` Corrupt Control bit, BR8(b3). The loopback modes can also be cleared by resetting the appropriate bits in BR6 to a 0.

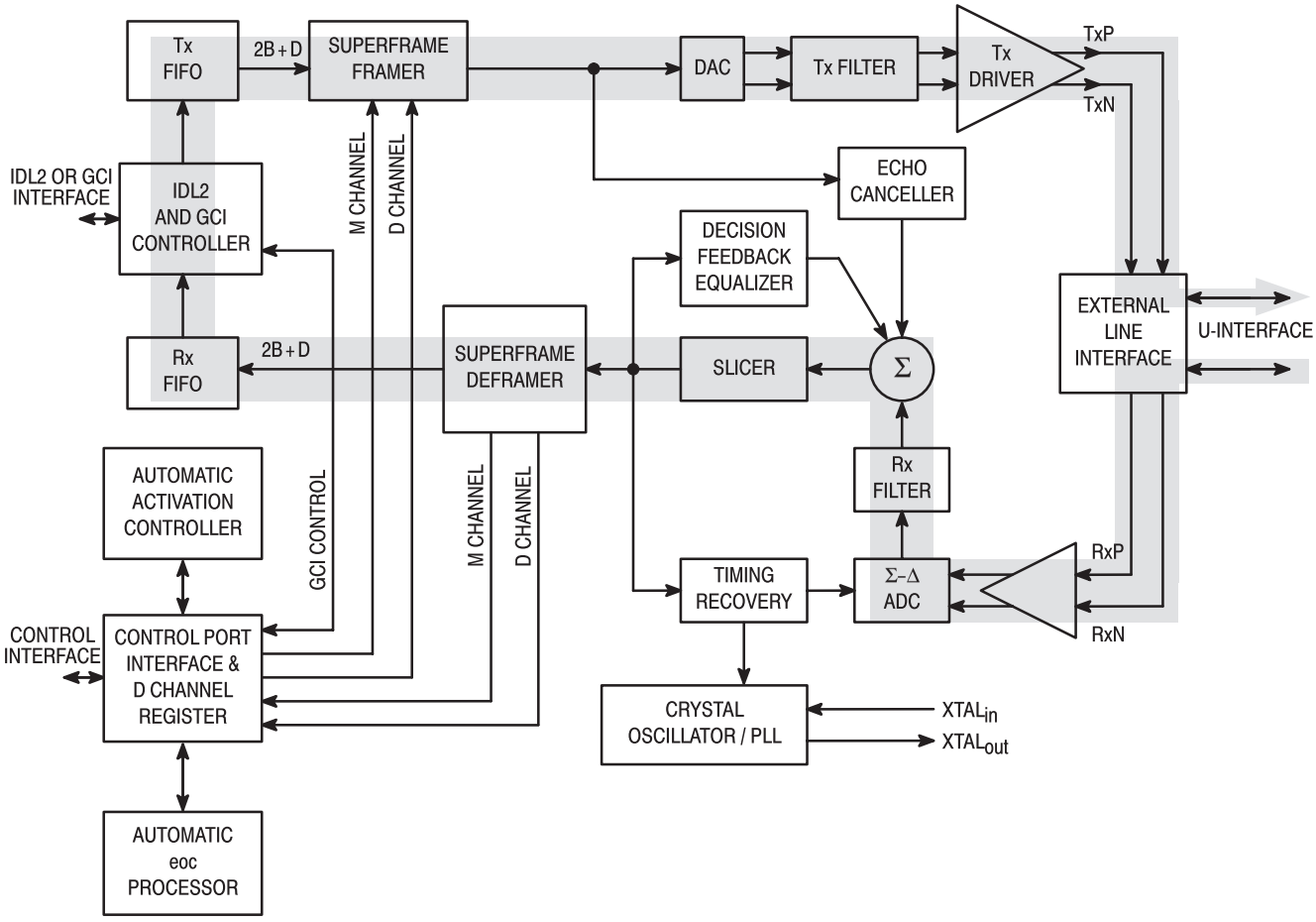


Figure 5–34. U–Interface Loopback Block Diagram

5.6.2 IDL2 Interface Loopback

An IDL2 interface loopback is shown in Figure 5–35. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and sends the same data back out the IDL2 Tx pin.

The four least significant bits of BR6 control the IDL2 Interface loopback modes. The loopback occurs in the IDL2 interface block of the MC145572. By setting IDL2–Loop Transparent (BR6(b0)) to a 1, the loopback is made transparent and the data input on the D_{in} pin is transmitted onto the U–interface. When IDL2–Loop Transparent (BR6(b0)) is reset to a 0, the data transmitted on the U–interface is forced to idle 1s when an IDL2 interface loopback mode is enabled.

An IDL2 interface loopback is selected by setting one or more of the registers IDL2–loop B1, IDL2–loop B2, or IDL2–loop 2B+D (BR6(b3:b1)) to a 1. To enable loopback of B1 channel data to the IDL2 interface, IDL2–loop B1 (BR6(b3)) is set to a 1. To enable loopback of B2 channel data to the IDL2 interface, IDL2–loop B2 (BR6(b2)) is set to a 1. To enable loopback of 2B+D data to the IDL2 interface, IDL2–loop 2B+D (BR6(b1)) is set to a 1. The 2B+D loopback mode overrides any B1 or B2 channel loopback that has been enabled. IDL2 interface loopback modes are independent of U–interface loopback modes and, as a result, these loopback modes can be operational simultaneously.

IDL2 interface loopback modes can be disabled by setting to a 1 and then resetting to a 0, the Return to Normal bit (NR0(b0)). This clears all bits in BR6 and the `crc` Corrupt Control bit, (BR8(b3)). IDL2 interface loopback modes can also be cleared by resetting the appropriate bits in BR6 to a 0.

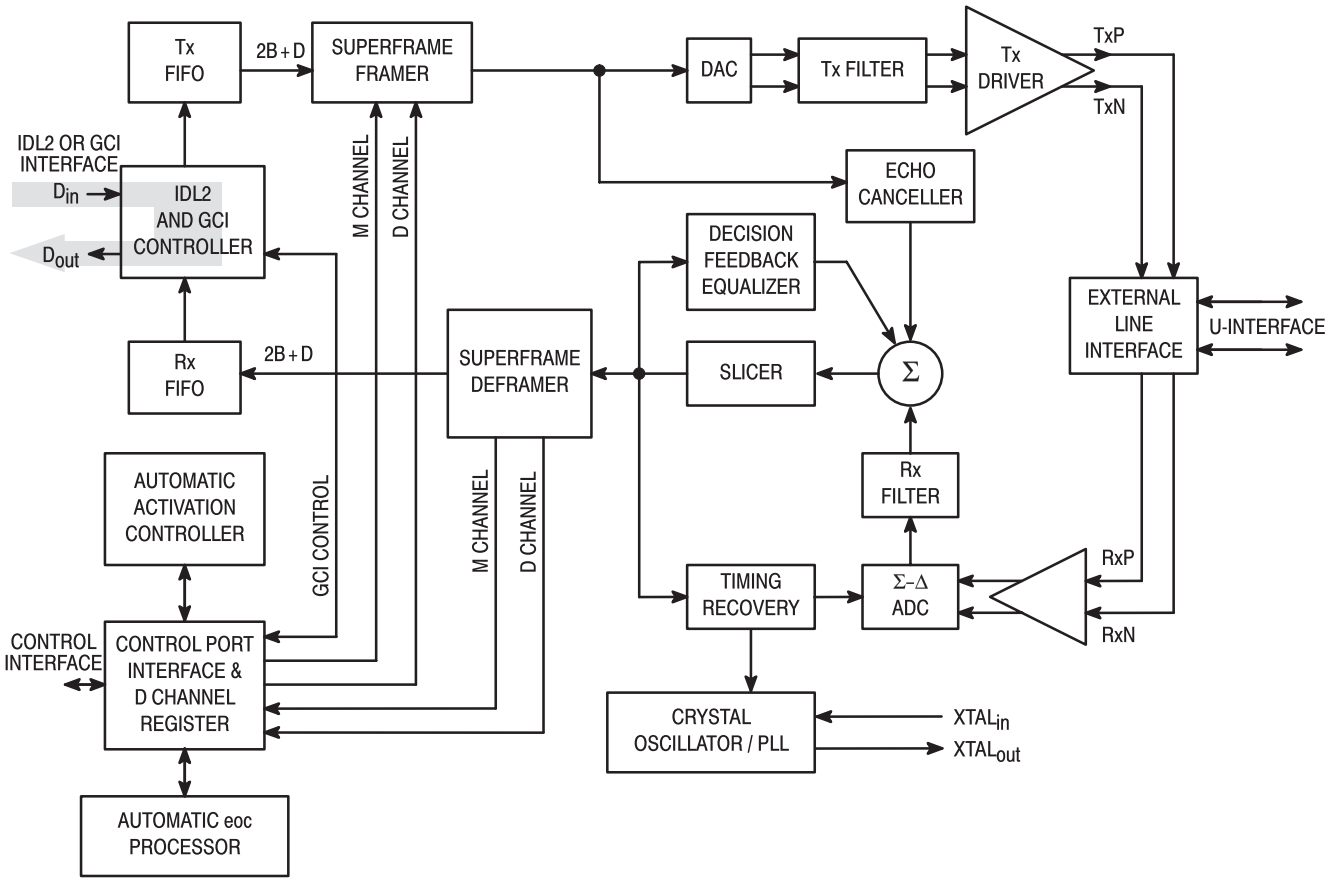


Figure 5–35. IDL2 Interface Loopback Block Diagram

5.6.3 Superframe Framer-to-Deframer Loopback

A Superframe Framer–to–Deframer loopback is shown in Figure 5–36. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the D_{in} pin and M channel data via the SCP, performs all of the superframe framing and subsequent deframing functions, and sends the same data back out the D_{out} pin and SCP. This loopback mode is intended primarily for diagnostic purposes.

Register BR14(b4) controls the Superframe Framer–to–Deframer Loopback mode. The loopback of B, D, and M channel data occurs between the output of the Superframe Framer block of the MC145572 and the Superframe Deframer input. In this loopback mode, the Tx Driver is disabled. A 1 written to BR14(b4) enables the mode and a 0 disables the mode. In addition, Match Scrambler (BR8(b2)) and Receive Window Disable (BR8(b1)) should be set to a 1.

The procedure to enable the Superframe Framer–to–Deframer loopback for a single NT–configured U–interface transceiver follows, with all numbers given in hexadecimal.

```
BR8 = B7      Match Polynomials, Receive Window Disable, set NT/LT Invert,
              transmit Frame Control state SN3.
```

Wait 5 seconds for the PLL to stabilize.

```
BR14 = 10     Enable Framer-to-Deframer Loopback, Enable CLKs. Enable CLKs is
              optional and enables SYSCLK to display an Eye Pattern.
BR12 = 89     Control Steer, Hold Activation State, Force Linkup.
BR13 = 0C     Accumulate DFE Output and Enable DFE Updates. Disable Echo
              Cancellers.
NR2 = 1       Set Customer Enable.
```

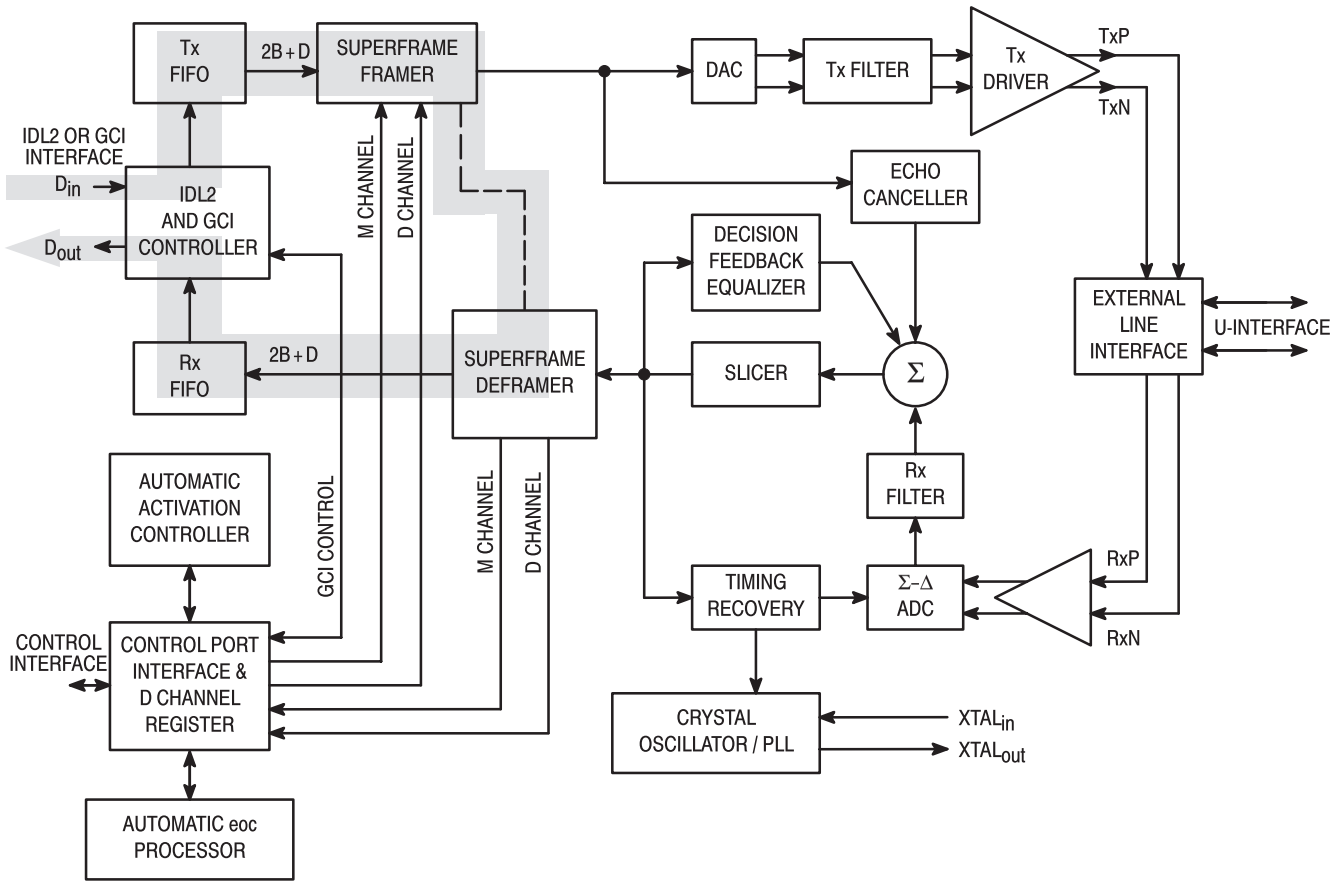


Figure 5–36. Superframe Framer–to–Deframer Loopback Block Diagram

The procedure to enable the Superframe Framer–to–Deframer loopback for a single LT–configured U–interface transceiver follows, with all numbers given in hexadecimal.

```
NR0 = 8       Assert reset, not required.
NR0 = 0       Deassert reset, not required.
BR14 = 10     Enable Framer-to-Deframer Loopback, Enable CLKs. Enable CLKs is
              optional and enables SYSCLK to display an Eye Pattern.
BR8 = B6      Match Polynomials, Receive Window Disable, do not set NT/LT
              Invert, transmit Frame Control state SL3.
BR12 = 89     Control Steer, Hold Activation State, Force Linkup.
BR13 = 0C     Accumulate DFE Output and Enable DFE Updates. Disable Echo
              Cancellers.
NR2 = 1       Set Customer Enable.
```

To turn off the Superframe Framer–to–Deframer loopback.

```
BR14 = $00
BR8 = $00
BR12 = $00
BR13 = $00
```

5.6.4 Superframe Framer-to-Deframer Loopbacks in Systems Having Multiple MC145572s

This section describes how to enable the Superframer Framer–to–Deframer loopback in applications where multiple MC145572s are normally operated in NT mode. A typical application is remote access equipment having four to eight MC145572 devices connected to a single time division multiplex bus. This time division mutliplex bus is connected to either an MPC860MH or 68MH360. The purpose of this section is to ensure that the DCL and FSR signal timing to the MC145572 device on which the loopback is being performed is derived from that same MC145572.

In NT systems, the 20.48 MHz clocks of the individual MC145572s are not synchronized to each other when all the transceivers are deactivated. Thus, when performing a Superframer Framer–to–Deframer loopback (or external analog loopback), a specific transceiver's DCL and FSR/FSX signals must not be traceable to another MC145572. This ensures that clock slips do not occur between the DCL/FSR signals and the 20.48 MHz clock of the MC145572 device under test.

In LT mode configurations, this is normally not a problem, since all of the MC145572s have their 20.48 MHz oscillators locked to system backplane timing. There will never be any clock slips.

Systems having multiple NT mode U transceivers on a TDM bus come in two types of architectures.

System Type No. 1: One U transceiver is configured as the TDM master and the others are configured as TDM slaves.

System Type No. 2: All U transceivers are configured as TDM slaves (M/$\overline{S}$ pin connected to V_{SS}). One U transceiver is selected to provide a locked system clock from which is derived the DCL and FSR/FSX signals that are provided to all U transceivers. Typically in such systems, there is a mux that allows the locked clock to be selected from one of the U transceivers. This allows any transceiver to provide the master clock. The clock source can come from the FREQREF pin (see OR8(b4) description), BUFXTAL pin, or SYSCLK pin.

In either type of system architecture, the Superframe Framer–to–Deframer loopback can be done on only one MC145572 at a time.

System Type No. 1: The transceiver on which the loopback test is performed is put into TDM master mode. This is done by connecting the M/$\overline{S}$ pin to V_{DD} or setting BR7(b1) to a 1, in the case of the M/$\overline{S}$ pin hardwired to V_{SS}. The other MC145572s are put into slave mode.

System Type No. 2: Enable the mux to select its reference clock source from the transceiver on which the loopback test is being performed.

Below is the procedure to perform the MC145572 Superframe Framer–to–Deframer loopback on the MC145572.

Make sure that there is a 10 kΩ pulldown resistor on the SFAX pin.

Set BR8(b0) = 1 to put the selected MC145572 into LT mode. (For devices with the NT/LT pin connected to V_{DD}.)

Set BR8(b0) = 0 to ensure the selected MC145572 is in LT mode. (For devices with the NT/LT pin connected to V_{SS}.)

Wait 5 seconds for the MC145572 on–chip PLL to stabilize. Write the following data to the MC145572 registers.

```
BR14 = $10
BR8 = $B7
BR12 = $89
BR13 = $0C
NR2 = $01
```

Configure the IDL bus or timeslot assigner for the bus format required to send/receive data with the MC145572.

The MC145572 is ready for the loopback test when NR1 reads as $0B.

To turn off the Superframe Framer–to–Deframer loopback.

```
BR14 = $00
BR8 = $00
BR12 = $00
BR13 = $00
```

5.6.5 External Analog Loopback

An external analog loopback is shown in Figure 5–37. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the D_{in} pin, and transmits the data out the Tx Driver pins. The 2B1Q signal passes through the external line interface circuitry and back into the receiver input pins. The signal is then recovered and sent out the D_{out} pin. It is recommended that Tip and Ring be physically disconnected from the U–interface twisted wire pair. This is perhaps the easiest way to assure that the transmitted signal is not properly terminated, resulting in very little trans–hybrid loss. Do not use a 135–ohm termination resistor.

OR7 bits 6 and 7 can be used to modify operation of the analog loopback. In order to use them, they must be set prior to setting OR9 (b5). These bits must be cleared after the analog loopback is turned off. These bits are cleared after any reset. See OR7 description for more details.

Since the entire 2B1Q superframe is being looped back, loopback data includes the 2B+D channels and all of the M channels. For instance, data written by an external microcontroller to the eoc, M4, and M5/M6 registers (R6, BR0, and BR2), is looped back and can be read from the eoc, M4, and M5/M6 registers (R6, BR1, and BR3).

For both NT and LT applications, ensure that a 10 kΩ pulldown resistor is connected to SFAX pin.

Procedure to enable analog loopback when operating NT/LT pin is connected to V_{DD} (NT mode).

```
BR8(b0) = 1   Put into LT mode.
```

Delay 5 seconds to allow PLL to stabilize.

```
BR10 = $01    Enable Overlay Register set.
OR8 = $22     Enable SFAX pin as output (only required for applications that
              do not have the 10 kΩ Pulldown Resistor).
OR9 = $20     Enable Analog Loopback.
BR10 = $00    Disable Overlay Register set.
```

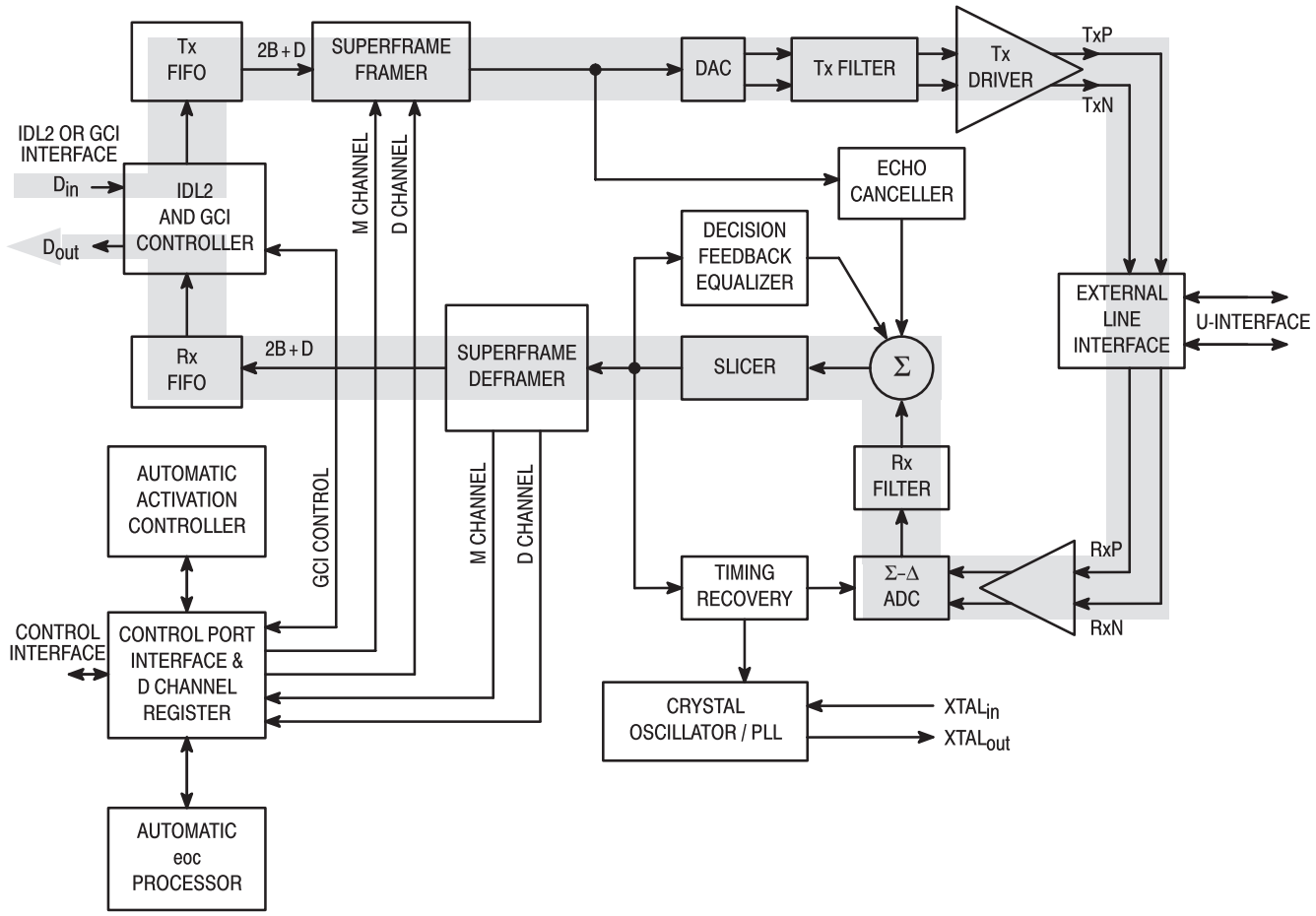


Figure 5–37. External Analog Loopback Block Diagram

Once the MC145572 has activated, NR1 reads as $B.

Procedure to turn off analog loopback when the NT/LT pin is connected to V_{DD} (NT mode).

```
BR10 = $01    Enable Overlay Register set.
OR8 = $00     Turn off SFAX pin (only required for applications that do not
              have the 10 kΩ Pulldown Resistor).
OR9 = $00     Turn off Analog Loopback bit.
BR10 = $00    Disable Overlay Register set.
BR8(b0) = 0
```

Procedure to enable analog loopback when the NT/LT pin is connected to V_{SS} (LT mode).

If the application software asserts any reset to the MC145572 prior to initiating the loopback, wait 5 seconds after deasserting the reset to allow the PLL to stabilize.

```
BR10 = $01    Enable Overlay Register set.
OR8 = $22     Enable SFAX pin as output (only required for applications that
              do not have the 10 kΩ Pulldown Resistor).
OR9 = $20     Enable Analog Loopback.
BR10 = $00    Disable Overlay Register set.
```

Once the MC145572 has activated, NR1 reads as $B.

Procedure to turn off analog loopback when the NT/LT pin is connected to V_{SS} (LT mode).

```
BR10 = $01    Enable Overlay Register set.
OR8 = $00     Turn off SFAX pin (only required for applications that do not
              have the 10 kΩ Pulldown Resistor).
OR9 = $00     Turn off Analog Loopback bit.
BR10 = $00    Disable Overlay Register set.
```

NOTE

In LT mode, the enabling/disabling of the SFAX pin is only required if the pin has not been tied to ground through a 10 kΩ resistor.

5.6.6 External Analog Loopbacks in Systems Having Multiple MC145572s

Systems having multiple NT mode U transceivers on a TDM bus come in two types of architectures.

System Type No. 1: One U transceiver is configured as the TDM master and the others are configured as TDM slaves.

System Type No. 2: All U transceivers are configured as TDM slaves. One U transceiver is selected to provide a locked system clock from which is derived the DCL and FSR/FSX signals that are provided to all U transceivers. Typically, in these systems there is a mux that allows the locked clock to be selected from one of the U transceivers. This allows any transceiver to provide the master clock. The clock source can come from the FREQREF pin (see OR8(b4) description), BUFXTAL pin, or SYSCLK pin. See **Section 5.6.4** for further background material.

The external analog loopback can be done on only one MC145572 at a time.

System Type No. 1: The transceiver that the loopback test is performed on is put into master mode. The others are put into slave mode.

System Type No. 2: Enable the mux to select its reference clock source from the transceiver on which the loopback test is being performed.

Procedure to perform the MC145572 external analog loopback while in NT slave mode.

Make sure that there is a 10 kΩ pulldown resistor on the SFAX pin.

Set BR8(b0) = 1, to put the selected MC145572 into LT mode.

Wait 5 seconds for the MC145572 on–chip PLL to stabilize.

```
BR10 = $01
OR9 = $20
BR10 = $00
NR2 = $01
```

Configure the IDL bus or timeslot assigner for the bus format required to send/receive data with the MC145572.

The MC145572 is ready for loopback test when NR1 reads as $0B.

To turn off the loopback.

```
BR10 = $01
OR9 = $00
BR10 = $00
```

6

MCU MODE ACTIVATION AND DEACTIVATION

6.1 INTRODUCTION

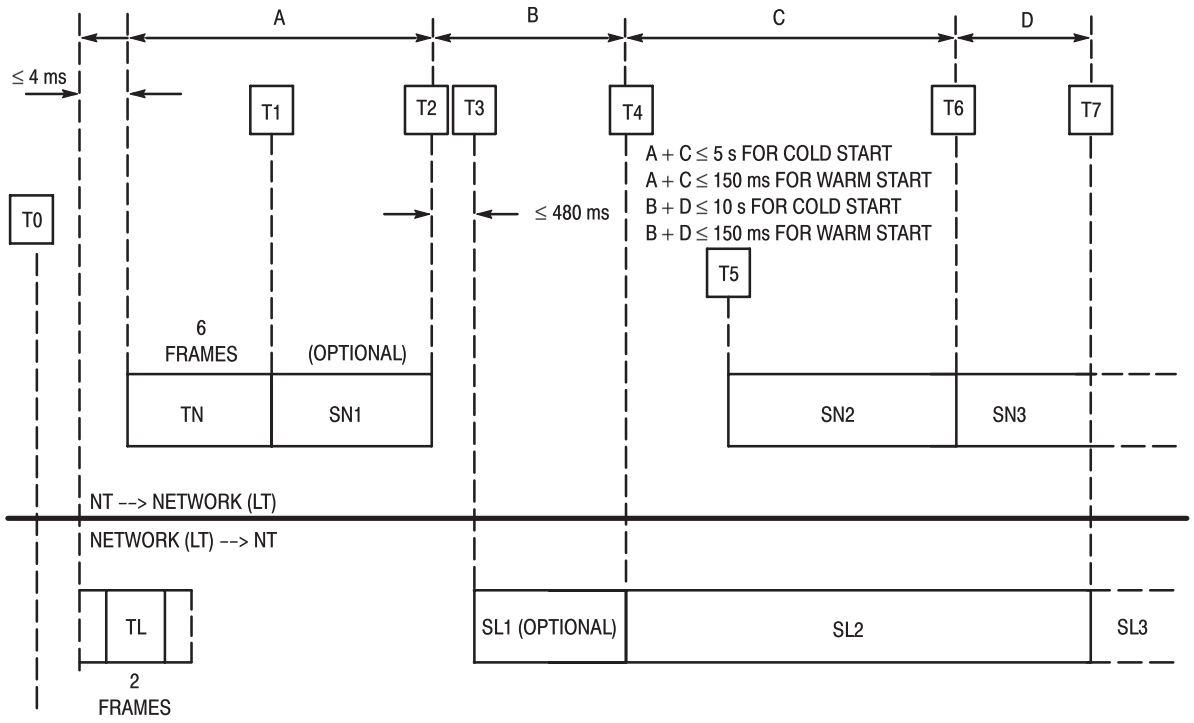
This chapter describes the activation and deactivation procedure for the MC145572. It is assumed that MC145572 is configured for the IDL2 mode of operation. The material covered in this chapter is useful for all applications. It is strongly recommended that this chapter be read when the GCI mode operation is to be used. **Chapter 8** gives a detailed functional description of the GCI mode operation including the activation and deactivation time flow diagrams.

Activation or start–up is the process U–interface transceivers use to initiate a robust full–duplex communications channel. This process, which may be initiated from either the LT or NT mode U–interface transceiver, is a well–defined sequence of procedures during which the training of the equalizers and echo cancellers at each end of the transmission line takes place. Two types of activation, cold start or warm start, may occur. The MC145572 is capable of automatically supporting both types.

Deactivation is the process used to gracefully end communication between the U–interface transceivers at each end of the transmission line. Only the LT mode U–interface transceiver may initiate a deactivation procedure.

ANSI T1.601–1992 defines ten activation signals, described in Tables 6–1 and 6–2, for the U–interface transceivers to use during the activation procedure. For instance, six basic frames of signal TN are transmitted by the NT when it wants to wake up the LT or in response to the LT transmitting TL. Two basic frames of signal TL are transmitted by the LT when it wants to wake up the NT. When the NT is in the fully operational mode, it transmits the signal known as SN3 and receives SL3 from the LT end. Conversely, when the LT is in fully operational mode, it transmits SL3 and receives SN3. Only when the U–interface is fully activated, with the NT transmitting signal SN3 and the LT transmitting SL3, are the 2B+D channels of data capable of being transmitted over the U–interface.

ANSI T1.601–1992 defines the M4 channel `act` bit, see BR0(b7) and BR1(b7), which signals the far–end U–interface transceiver that the near–end is capable of transparently passing 2B+D data. Figure 6–1 shows the activation diagram from the ANSI T1.601 specification. This figure can be used in conjunction with this text to understand the activation sequence.



Time	Description of Event or State
T0	RESET state.
T1	Network and NT are awake.
T2	NT discontinues transmission, indicating that NT is ready to receive signal.
T3	Network responds to termination of signal and begins transmitting signal toward NT.
T4	Network begins transmitting SL2 toward NT, indicating that the network is ready to receive SN2.
T5	NT begins transmitting SN2 toward the network, indicating that NT has acquired SW frame and detected SL2.
T6	NT has acquired superframe marker, and is fully operational.
T7	Network has acquired superframe marker, and is fully operational.

Figure 6–1. ANSI U–Interface Transceiver Activation State Diagram

6.2 ACTIVATION SIGNALS FOR NT MODE

When configured as an NT, the MC145572 U–interface transceiver can transmit any of the signals shown in Table 6–1. The actual procedure undertaken by the device using these five signals is described later in this chapter. **Section 4.4.9** describes how to control the transmit framer when it is desired to generate signals for test purposes.

Table 6–1. NT Mode Activation Signals

Information Station	Description
TN	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of six frames.
SN0	No signal transmitted.
SN1	Synchronization word present, no Superframe Synchronization word (ISW), and 2B+D+M = 1.
SN2	Synchronization word present, no Superframe Synchronization word (ISW), and 2B+D+M = 1.
SN3	Synchronization word present, Superframe Synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 `act` bit = 1. When M4 `act` = 0, transmitted 2B+D data = 1.

6.3 ACTIVATION SIGNALS FOR LT MODE

When configured as an LT, the MC145572 U–interface transceiver can transmit any of the signals shown in Table 6–2. The actual procedure undertaken by the device using these five signals is described later in this chapter. **Section 4.4.9** describes how to control the transmit framer when it is desired to generate signals for test purposes.

Table 6–2. LT Mode Activation Signals

Information Station	Description
TL	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of two frames.
SL0	No signal transmitted.
SL1	Synchronization word present, no Superframe Synchronization word (ISW), and 2B+D+M = 1.
SL2	Synchronization word present, Superframe Synchronization word (ISW) present, 2B+D = 0, and M = Normal.
SL3	Synchronization word present, Superframe Synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 `act` bit = 1. When M4 `act` = 0, transmitted 2B+D data = 0.

6.4 ACTIVATION INITIATION

The MC145572 U–interface transceiver can be activated in either of two ways. The external microcontroller can explicitly issue Activation Request (NR2(b3) = 1) or the transceiver detects an incoming 10 kHz wake–up tone. An LT configured U–interface transceiver searches for an NT sending the TN wake–up tone. An NT configured U–interface transceiver searches for an LT sending the TL wake–up tone. In IDL2 mode, the Activation in Progress status bit (NR1(b0)) is set to a 1 when an incoming 10 kHz wake–up tone is detected. In either case, Activation Request being set or a wake–up tone being detected, the U–interface transceiver proceeds with activation automatically and signals the result of the activation to the external microcontroller by setting status bits in NR1 to $B.

An NT configured U–interface transceiver always initiates activation by sending a TN tone to the LT. This is done in response to the LT sending a TL or when the Activation Request bit (NR2(b3)) is set to a 1.

An LT configured U–interface transceiver initiates activation by sending the TL tone when the Activation Request bit is set to a 1 by an external microcontroller. The NT U–interface transceiver responds to the TL tone by sending a TN tone back to the LT U–interface transceiver. Otherwise, the LT U–interface transceiver waits for an unsolicited incoming TN tone from the NT U–interface transceiver and self–activates. Regardless of how activation is initiated, the LT U–interface transceiver automatically activates from the point where it detects the incoming TN tone from the NT transceiver.

When configured for MCU mode, all appropriate maintenance channel registers should be initialized prior to setting Activation Request (NR2(b3)) or immediately after detecting Activation in Progress (NR1(b0)) = 1. In GCI mode, the MC145572 automatically initializes the maintenance channel registers.

Some applications, such as U–repeaters, may require longer than 15 seconds of activation time. The 15–second activation timer can be disabled by setting Activation Timer Disable (BR11(b0)) to a 1.

6.5 ACTIVATION OF U-INTERFACE BY NT

NT mode activation initiation is accomplished by setting Activation Request (NR2(b3)) to a 1. The NT U–interface transceiver initiates activation of the U–interface by transmitting TN for a time period of six frames (9 ms) toward the LT. At this time, the NT U–interface transceiver also sets Activation in Progress (NR1(b0)) to a 1. Transmission of TN is immediately followed by transmission of SN1 while the echo cancellers are trained.

From Figure 6–1, it can be seen that the NT transceiver has a period of time during activation where the LT end is guaranteed to be quiet. This is to permit the MC145572 to train its echo cancellers during the transmission of SN1.

After the MC145572 ends transmission of SN1 it waits up to 480 ms for LT to transmit a signal, SL1 or SL2. The MC145572 then recovers timing information and transmits SN2. When full duplex operation has been achieved, bits NR1(b3, b1, b0) are each set to a 1 and SN3 is enabled for transmission. SN3 is transmitted with only the maintenance channel bits active until transparent 2B+D transmission is enabled by setting Customer Enable (NR2(b0)) to a 1, or the M4 channel `act` bit has been received when the MC145572 is configured for the Verified `act` mode. See BR9(b5,b4) for more about Verified `act`.

If SN3 is not reached within 15 seconds, activation is automatically aborted, Error Indication (NR1(b2)) is set to a 1, and bits NR1(b3, b1, b0) are each reset to a 0. The 15–second activation timer is started when Activation in Progress (NR1(b0)) is set to a 1. The Activation Request bit (NR2(b3)) is internally reset to a 0 when Activation in Progress (NR1(b0)) is set to a 1.

6.6 ACTIVATION OF U-INTERFACE BY LT

LT mode activation initiation is accomplished by setting Activation Request (NR2(b3)) to a 1. The LT initiates activation of the U–interface by transmitting TL for a period of two frames (3 ms) toward NT. At this time, the LT U–interface transceiver also sets Activation in Progress (NR1(b0)) to a 1. After LT stops sending TL, the NT transmits TN and SN1 and trains its echo cancellers. The LT then waits for loss of the far–end signals, TN and SN1.

Loss of TN and SN1 reception is immediately followed by the LT transmission of SL1, while the LT end echo cancellers are trained. From Figure 6–1, it can be seen that the LT transceiver has a period of time during activation where the NT end is guaranteed to be quiet. This is to permit the MC145572 to train its echo cancellers during the transmission of SL1 and part of SL2. During SL2, the MC145572 looks for a far–end signal. The MC145572 then recovers timing information and trains for full duplex operation. When full duplex operation has been achieved, NR1(b3, b1, b0) are each set to a 1 and SL3 is transmitted with the M channel bits active. The 2B+D channels become active when Customer Enable (NR2(b0)) is set to a 1.

If activation continues for more than 15 seconds it is aborted, Error Indication (NR1(b2)) is set to a 1, and bits NR1(b3,b1,b0) are each reset to a 0. The 15–second activation timer is started when Activation in Progress (NR1(b0)) is set to a 1. Activation Request (NR2(b3)) is internally reset to a 0 when Activation in Progress (NR1(b0)) is set to a 1.

6.7 ACTIVATION INDICATION

The Linkup status bit (NR1(b3)) is used to signify that the loop is active. With MC145572 configured as an NT, this corresponds to NT transmitting SN3 and receiving SL3. With MC145572 configured as an LT, this corresponds to LT transmitting SL3 and receiving SN3. When the U–interface is fully active, Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are set to a 1.

When the LT U–interface transceiver is activated and ready to pass 2B+D data, the M4 channel `act` bit should be set per ANSI T1.601–1992. This is done by setting BR0(b7) to a 1. Also, it is required that Customer Enable (NR1(b0)) be set to a 1 when the M4 channel verified `act/dea` mode is not enabled. This must be done after activation from the receive $\overline{\text{RESET}}$ state. Refer to **Section 4.4.10**, for more details on Verified `act/dea` and control of M4 channel bits.

Whenever the MC145572 detects loss of Superframe Synchronization, NR1 becomes $8 and an interrupt is generated if enabled. This indicates that loss of Superframe Synchronization has been detected. When Superframe Synchronization is lost for more than 480 ms, MC145572 always deactivates and sets NR1 = $4 error indication, and issues an interrupt if enabled. When the error condition causing loss of Superframe Synchronization goes away before 480 ms has elapsed, NR1 returns to $B and an interrupt is generated if enabled. It is not necessary to set Customer Enable (NR2(b0)) to a 1 when NR1 returns to $B.

The MC145572 continually monitors the error on its recovered signal. If the internally monitored error rate becomes too large, MC145572 loses data transparency and NR1 changes to $A or $8 and issues an interrupt. Note that loss of Superframe Synchronization always means that data transparency is lost, but loss of data transparency does not always mean that Superframe Synchronization is lost. Also, note that loss of signal always means that Superframe Synchronization is lost. There is no time

limit on how long NR1 may read as $A when data transparency is lost. There is a 480–ms time limit on NR1 reading as $8. ANSI T1.601 only indicates that U–interface transceivers must deactivate when Superframe Synchronization or receive signal is lost for more than 480 ms. If the error condition goes away, NR1 returns to $B and an interrupt is generated, if enabled.

Loss of Superframe Synchronization may be due to a high internally detected error rate on recovered data or the temporary loss of received signal.

6.8 NT DEACTIVATION PROCEDURES AND WARM START

ANSI T1.601 specifies that NT can not initiate deactivation. The MC145572 deactivates to a warm start condition when Deactivation Request (NR2(b2)) is set to a 1 prior to LT deactivating the U–interface. This should be done in response to the M4 channel dea bit being received as 0 by NT when the loop is active. If Deactivation Request (NR2(b2)) is not set to a 1 before LT deactivates the U–interface, MC145572 deactivates to a cold start condition and gives an error indication interrupt. Deactivation Request is automatically set if the M4 maintenance bits are operated with automatic verification of activation and deactivation. So when LT deactivates the line, NT deactivates to a warm start condition. See BR9(b5:b4) and OR7(b0) for more information.

6.9 LT DEACTIVATION PROCEDURES

ANSI T1.601 specifies that only LT can deactivate the U–interface. This is done in the MC145572 by setting Deactivation Request (NR2(b2)) to a 1.

Prior to deactivating, LT should notify NT of the pending deactivation by clearing the M4 channel dea bit towards NT for at least three superframes. Then, deactivate LT by setting Deactivation Request (NR2(b2)) to a 1.

The MC145572, when configured as an LT, has a mode in which the M4 channel can be updated and sent for exactly three superframes before deactivation occurs. This is done in the following manner. Set Superframe Update Disable (NR2(b1)) to a 1 to disable maintenance channel updates. Reset the M4 channel dea bit (BR0(b6)) to a 0 to indicate that the LT initiated deactivation. Reset Superframe Update Disable (NR2(b1)) to a 0 and simultaneously set Deactivation Request (NR2(b2)) to a 1 to re–enable maintenance channel updates and initiate deactivation. The LT U–interface transceiver then updates the maintenance channel Superframe Framer bits and sends exactly three superframes with the M4 channel dea bit reset to a 0. The U–interface transceiver then deactivates per ANSI T1.601–1992.

6.10 INITIAL STATE OF B1 AND B2 CHANNELS

The MC145572 comes out of hardware or software reset with customer data disabled. This corresponds to Customer Enable (NR2(b0)) reset to 0. When the M4 channel Verified act/dea mode is not used, it is required that Customer Enable (NR1(b0)) be set to a 1, to enable data transparency when NR1 becomes $B after initial activation. The B1, B2, and D channels transmitted on the IDL interface are automatically enabled after the MC145572 activates. Data on the B1 channel from the U–interface corresponds to data in the B1 channel timeslot on the IDL interface. Data on the B2 channel from the U–interface corresponds to data on the B2 channel timeslot on the IDL interface. The B1 and B2 channel timeslots on the IDL interface can be swapped by setting Swap B1/B2 (NR5(b0)) to a 1.

6.11 ADDITIONAL NOTES

6.11.1 Maintenance Channel Bits

The received eoc, M4, M5, and M6 channel bits are available in registers R6, BR1, and BR3 once linkup has been attained. The Customer Enable bit (NR2(b0)) affects only the two B channels and the D channel. See BR0 – BR3 and BR9 descriptions for a full description of the maintenance channel bits and their control.

6.11.2 Indication of Transmit States and Repeater Applications

BR8(b7:b4), Frame State 3 through Frame State 0, indicates the current state of the Superframe Framer. In a U–interface repeater, it may be necessary to have NT continue transmitting SN2 until LT–configured MC145572 receives SN3. Software must monitor the transmit state at least once every millisecond to determine when NT starts transmitting SN2. When start of SN2 transmission is detected, write $A to BR8(b7:b4) to hold the transmit framer in SN2. Once LT indicates full activation, the transmit framer can be allowed to proceed to SN3 by writing $0 to BR8(b7:b4).

It may also be necessary to disable the 15–second activation timer in repeater applications. This is done by setting Activation Timer Disable (BR11(b0)) to a 1 prior to initiating activation or when Activation in Progress, NR1 = $1, is detected.

7

MCU MODE MAINTENANCE CHANNEL OPERATION

7.1 INTRODUCTION

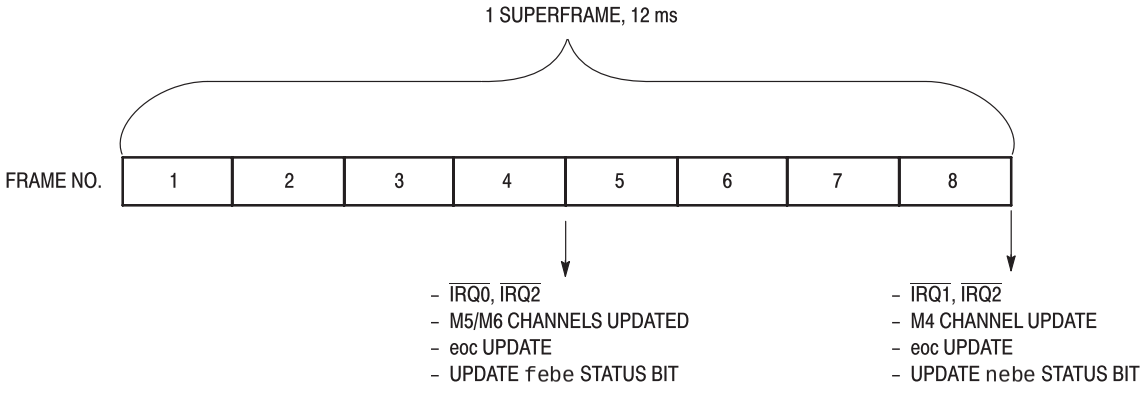
When configured for MCU mode operation, the MC145572 provides a very flexible interface to the 4 kbps maintenance channel (M channel), defined in ANSI T1.601–1992. The maintenance channel consists of 48 bits sent by both the LT and NT configured U–interface transceivers during the course of a superframe. These 48 bits are divided into 6 subchannels, designated M1 through M6, each consisting of 8 bits per superframe. The eoc consists of M1, M2, and M3. The overhead bits, such as `crc`, `febe`, `act`, and `dea`, are contained in subchannels M4, M5, and M6.

An external microcontroller can read from or write to the maintenance channel via the SCP or PCP interfaces. Interrupts to an external microcontroller can be enabled when an eoc, M4, M5, or M6 channel register is updated. Maintenance channel registers can be configured to update when a new value is detected between successive superframes, when a bit changes, or when two or three successive superframes of a new value are detected. The M4 channel `act` bit, BR1(b7), can also be configured to automatically enable or disable customer data when in NT or LT mode of operation. The M4 channel `dea` bit, BR1(b6), can also be configured to automatically issue a deactivation request in NT mode of operation. The maintenance channel registers are updated only when Superframe Sync, NR1(b1), is set to a 1.

Sections 7.5 and 7.6 provide information of interest to designers of LULT/LUNT (Line Unit Like–LT/Line Unit Like–NT1) type line cards for use in digital loop carrier systems using end–to–end performance monitoring.

See the BR9 description in **Section 4.4.10** for more details on maintenance channel register operations. Figure 7–1 shows the relationship between the received superframe and when the interrupt line is asserted when the appropriate interrupts have been enabled.

The text in this chapter is based on an ANSI T1.601 compliant application. Due to the flexibility of the MC145572 register interface, it can easily be used in proprietary applications.



NOTE: Since the eoc register, R6, is updated after basic frames 4 and 8, $\overline{IRQ2}$ can occur at either location, or both, depending on the setting of BR9(B7:b6).

Figure 7–1. Maintenance Channel Interrupt Timing

7.2 EMBEDDED OPERATIONS SUBCHANNEL

The eoc subchannel can operate in one of three modes. The eoc register, R6, can be updated and an interrupt generated on every received eoc frame, and on a successful trinal–check of a new eoc frame. This applies to the NT and LT modes of operation. In NT mode, the MC145572 also provides an Automatic eoc Processor for automatic decoding and response to the ANSI T1.601–1992 eoc messages. The R6 update occurs only when Superframe Sync, NR2(b1), has been detected and set to a 1. When the microcontroller writes to eoc register R6, the new eoc word is loaded into the Superframe Framer on the next eoc frame boundary, assuming the automatic eoc mode is not enabled. These modes are selected by eoc Control 1 and eoc Control 0, BR9(b7:b6).

In Trinal–Check mode, R6 is updated when three consecutively received eoc frames are the same. When the automatic eoc mode with trinal–check has been selected and the U–interface transceiver is operating as an NT, the decoded eoc is acted on when a valid trinal–check has occurred and R6 is updated.

R6 can be configured to update on every eoc frame by setting eoc Control 1 and eoc Control 0, BR9(b7:b6), each to a 1. The update occurs every 6 ms, even if no change has been detected between eoc frames. This mode must be used for proprietary and non–ISDN basic rate applications.

CAUTION

Read text in **Section 4.4.10** concerning Trinal–Check mode very carefully.

R6 is updated in all modes of operation. This permits an external microcontroller to monitor eoc messages when the Automatic eoc Processor is enabled in NT mode. R6 is updated at the mid–point or at the end of a superframe.

Regardless of the mode of operation, an update of R6 generates an interrupt whenever Enable $\overline{\text{IRQ2}}$, NR4(b2), is set to a 1.

7.3 M4 SUBCHANNEL AND DATA TRANSPARENCY

The M4 subchannel operates in one of four modes set in BR9(b5:b4). The received M4 data from the Superframe Deframer is available in BR1. The transmitted M4 subchannel data is written to Byte register BR0. See BR9 in **Section 4.4.10** and Verified act and Verified dea, BR3(b2:b1), in **Section 4.4.4** for more details on the M4 channel register operations. When set to a 1, the M4 Trinal Mode bit, OR7(b0), configures the M4 uoa, sai, dea, and act bits to be updated after a trinal–check. See descriptions for BR0, BR9, and OR7 for more details.

M4 Control mode 0,0 is the dual consecutive mode of operation with automatic verification of the M4 act bit in LT and NT modes and automatic verification of the M4 dea bit in NT mode. In this mode, once Superframe Sync, NR2(b1), is set to a 1, BR1 and Verified act, BR3(b2), are updated when the Superframe Deframer detects that an M4 channel bit has changed state and has remained in that state for two consecutive superframes. The M4 maintenance subchannel bits act, dea, sai, and uoa can be configured for trinal–checking by setting OR7(b0) to a 1.

When OR7(b0) is set to a 1, the received M4 bit positions in BR1 corresponding to act, dea, sai, and uoa are updated on a trinal–check regardless of the programmed M4 Control bits in BR9(b5, b4). The remaining bits in BR1 are updated according to the programmed M4 Control bits in BR9(b5, b4). Note that the Verified act/dea mode BR9(b5, b4) = 0,0 operates on trinal–checked M4 act and dea bits when OR7(b0) is a 1. See Table 4–7 and **Sections 4.4.10 and 4.5.8**.

In either the LT or NT modes of operation, customer data transparency is achieved by the logical OR of Verified act, BR3(b3), and Customer Enable, NR2(b0). This means when the received M4 act bit is a 1 and the M4 channel is configured in the Verified act/dea mode, data transparency is automatically enabled. If the Verified act/dea mode is not enabled, Customer Enable, NR2(b0), must be set to a 1 to permit transmission of 2B+D data onto the U–interface.

When Customer Enable, NR2(b0), is set to a 1, data transparency occurs on the next IDL frame boundary, not the next superframe boundary. The recommended procedure is for firmware in NT1 to assert the act bit, BR0(b7), to a 1 after it has determined that NT1 is ready for layer two transmission. This should be immediately followed by setting Customer Enable, NR2(b0), to a 1. Section 6.4.6.6 of

ANSI T1.601–1992 indicates that data transparency may occur during the last superframe having its act bit equal to 0 or during the first superframe having its act bit equal to 1.

In the NT mode of operation, the M4 dea bit is checked for a 0 and the logical OR of Verified dea, BR3(b1), and deactivation Request, NR2(b2), ensures that the NT U–interface transceiver deactivates in a controlled manner and will reactivate in warm start mode on a subsequent activation attempt. An interrupt is generated when BR1 is updated, if Enable $\overline{\text{IRQ1}}$, NR4(b1), is set to a 1.

M4 Control mode 0,1 is the dual consecutive mode of operation. BR1 is updated when the Superframe Deframer detects that an M4 subchannel bit has changed state and has remained in that state for two consecutive superframes and Superframe Sync, NR2(b1), is set to a 1. An interrupt is generated at this time, if Enable $\overline{\text{IRQ1}}$, NR4(b1), is set to a 1.

M4 Control mode 1,0 is the delta mode of operation. The M4 channel register is updated with new M4 channel data whenever any single bit changes between received M4 frames. An interrupt is generated at this time, if Enable $\overline{\text{IRQ1}}$, NR4(b1), is set to a 1.

M4 Control mode 1,1 updates the M4 channel register BR1 on every received superframe. In this mode, the Superframe Deframer does not check for a change in data between received M4 frames. An interrupt is generated at this time, if Enable $\overline{\text{IRQ1}}$, NR4(b1), is set to a 1.

7.4 M5 AND M6 CHANNELS

The M5 and M6 channels operate in the same modes as the M4 channel bits, except for the automatic verification mode. The received M5 and M6 data from the Superframe Deframer is available in BR2. See BR9 for details on the operating modes of the M5 and M6 channels. These channels are configured as a pair. An interrupt is generated when BR2 is updated and Enable $\overline{\text{IRQ0}}$, NR4(b0), is set to a 1. As defined by ANSI T1.601–1992, these are reserved maintenance channels and should be initialized to 1s. The M5 and M6 maintenance channels are available for proprietary applications which do not have to comply with ANSI T1.601.

7.5 febe AND nebe BITS

The MC145572 has extensive febe and nebe maintenance capabilities. The state of the received computed nebe and of the received febe is available through the register interface. Also, two independent febe and nebe counters are available for performance monitoring purposes.

The received febe from the last completed superframe is available in Received febe, BR3(b4). It is updated at the end of each superframe when both Superframe Sync and Linkup, NR1(b3, b1), are set to a 1.

The febe/nebe Control bit, BR9(b1), controls operation of the transmitted febe status bit. When BR9(b1) is set to a 1, the transmitted febe bit is set to whatever is set in the febe input, BR2(b4). When BR9(b1) is reset to a 0, the transmitted febe is set active, if the computed nebe is active or if febe input, BR2(b4), is active. In this case, “active” means 0. BR9(b1) reset to 0 is the normal mode of operation and no intervention is required by an external MCU for the MC145572 to send the outgoing febe bit.

In NT and LT mode operation when BR9(b1) is set to a 1, BR2(b4) must be cleared to a 0 at the end of reception of basic frame 8 when it is desired to force an outgoing febe. BR2(b4) must be set to a 1 at the end of reception of basic frame 8 when no outgoing febe is required. Software should always configure BR2(b4) for the correct outgoing febe once each superframe. In digital loop carrier applications, this guarantees that there will be a one–to–one correspondence between the febe status received from the digital carrier system and the febe transmitted on the U–interface. The febe is transmitted at the end of basic frame 2. See Figure 7–1 and **Section 7.7** for interrupt timing information.

The computed nebe of the last completed superframe is available in Computed nebe, BR3(b3). This bit is set or cleared as a result of a crc of the last superframe received. This bit is updated at the end of each superframe. The Computed nebe is reset to a 0 when a crc error is detected, and is set to a 1 when no crc error is detected. When either Superframe Sync or Linkup, NR1(b3, b1), are reset to a 0, the Computed nebe bit is forced to a 0.

The current febe count is maintained in BR4. The count in BR4 is incremented only when the received febe bit is detected active (0) at the end of the superframe. When OR7(b1) is a 0, the febe counter does not wrap around when the count reaches $FF. When OR7(b1) is a 1, the febe counter wraps around and continues counting from 0. Also, BR4 should be reset to 00 after Linkup is detected during activation. This is done by the external microcontroller writing 00 to BR4. The count is incremented when both Superframe Sync and Linkup in NR1(b1, b3) are set to a 1 and the received febe bit is a 0. Received febe is available in BR3(b4) and is a 0 when active.

The current nebe count is maintained in BR5. The count in BR5 is incremented only when the Computed nebe bit is detected active (0) at the end of the superframe. The count is also incremented once per superframe during loss of synchronization, i.e., if Superframe Sync, NR2(b1), drops to a 0 when Linkup, NR2(b3), is set to a 1. When OR7(b1) is a 0, the nebe counter does not wrap around when the count reaches $FF. When OR7(b1) is a 1, the nebe counter wraps around and continues counting from 0. Also, BR5 should be reset to 00 after Linkup is detected during activation. This is done by the external microcontroller writing 00 to BR5. The count is incremented when both Superframe Sync and Linkup in NR1(b1, b3) are set to a 1 and when an error is detected in the received crc. A Computed nebe is active when the received crc does not exactly match the calculated crc on the received superframe data. The Computed nebe is available in BR3(b3) and is a 0 when a crc error has been detected.

7.6 FORCE CORRUPT crc

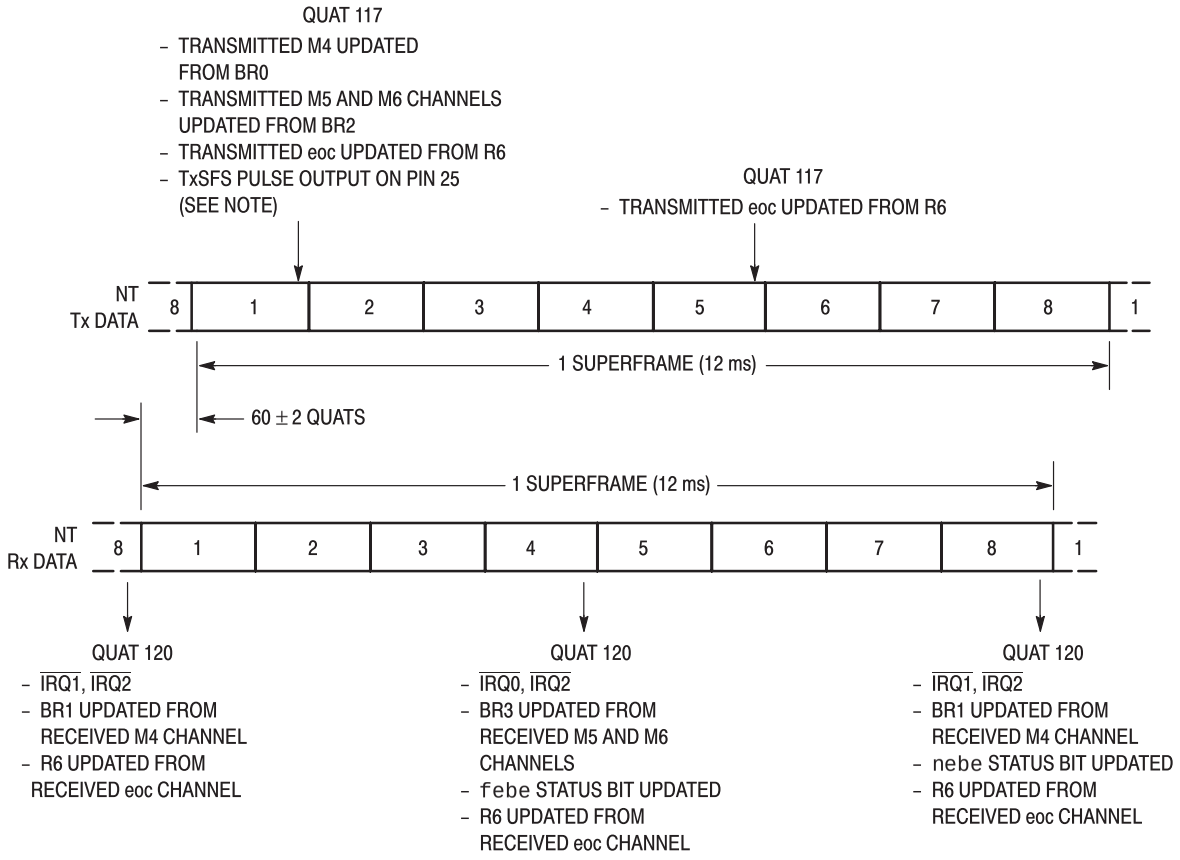
The MC145572 provides a mechanism where the outgoing crc can be corrupted. The transmitted crc is corrupted when BR8(b3) is set to a 1. The crc corruption is accomplished by inverting the transmitted crc bits. See Table 7–1. The next two paragraphs are of particular interest to designers of digital loop carrier system LULT and LUNT type line cards.

In NT mode operation, when it is desired to corrupt the outgoing crc, BR8(b3) should be set at the end of reception of basic frame 4 and must be cleared at the end of reception of basic frame 8. This inverts the outgoing crc in transmitted basic frames 4, 5, 6, and 7 of the current transmitted superframe. See Figure 7–2. When crc Corrupt mode, OR7(b2), is set to a 1, it is not necessary to clear BR8(b3), since it is cleared automatically at the end of the transmitted superframe. This guarantees that the corrupt crc will be transmitted only in the current superframe and that there will be a one–to–one correspondence between the corrupt crc status received from a digital carrier system and the corrupt crc transmitted on the U–interface. See **Section 7.7.**

In LT mode operation, when it is desired to corrupt the outgoing crc, BR8(b3) should be set at the end of reception of basic frame 8 and must be cleared at the end of reception of basic frame 8. This inverts the outgoing crc in transmitted basic frames 1 through 8 of the current transmitted superframe. See Figure 7–3. When crc Corrupt mode, OR7(b2), is set to a 1, it is not necessary to clear BR8(b3), since it is cleared automatically at the end of the transmitted superframe. This guarantees that the corrupt crc will be transmitted only in the current superframe and that there will be a one–to–one correspondence between the corrupt crc status received from a digital carrier system and the corrupt crc transmitted on the U–interface. See **Section 7.7.**

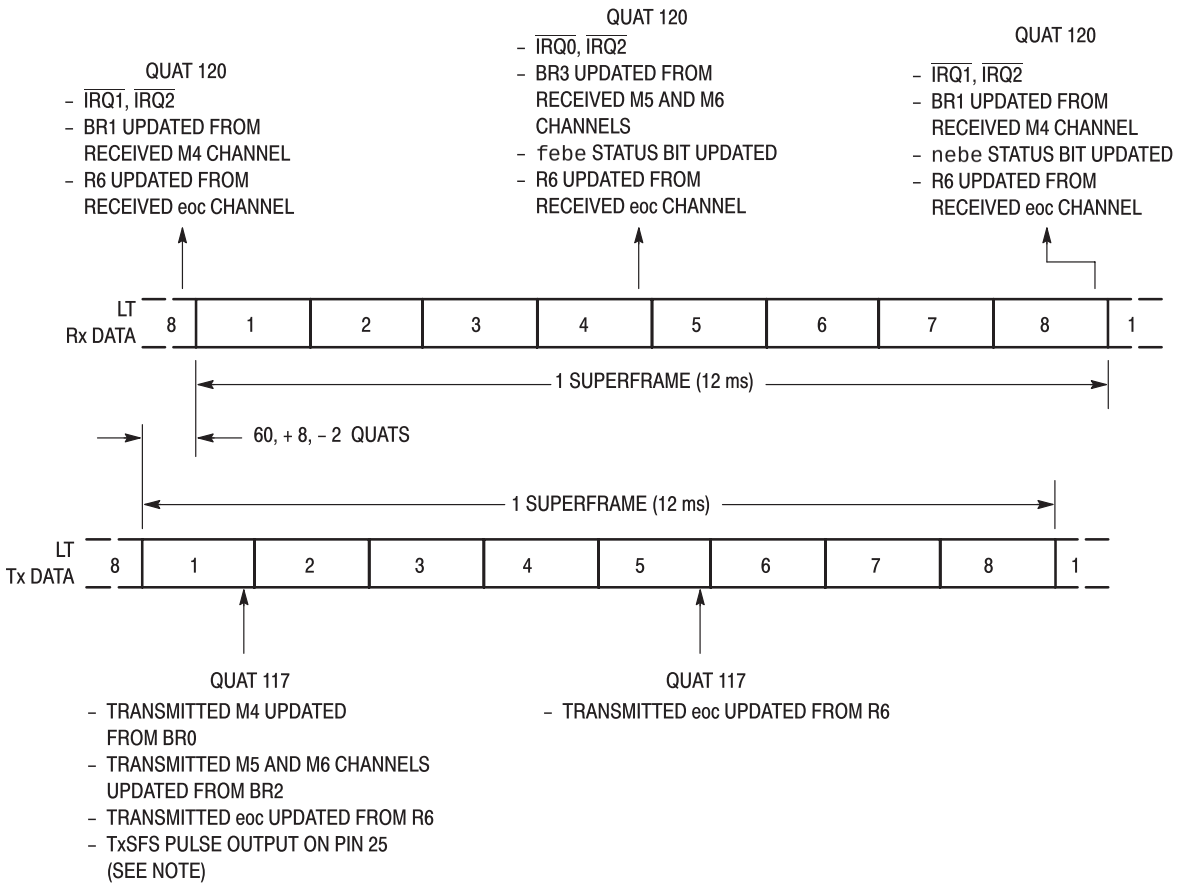
Table 7–1. Transmitted crc Configuration

BR8(b3)	OR9(b2)	Effect on Transmitted crc
0	X	No effect, transmitted crc is a good crc and far–end transceiver receives it correctly. This is the default mode after any reset.
1	0	Transmitted crc is continuously corrupted by inverting the crc symbols. This causes the far–end transceiver to detect crc errors. BR8(b3) must be returned to a 0 to stop the transmission of bad crcs.
1	1	Transmitted crc is corrupted only until the end of the current U–interface superframe. Then BR8(b3) is cleared to 0.



NOTE: Due to internal delays, the actual sync word marker on the TxP and TxN pins occurs 8 quats later than the TxSFS pulse. See Figure 10–20.

Figure 7–2. NT Mode Maintenance Channel Updates



NOTE: Due to internal delays, the actual sync word marker on the TxP and TxN pins occurs 8 quats later than the TxSFS pulse. See Figure 10–20.

Figure 7–3. LT Mode Maintenance Channel Updates

The crc Corrupt mode bit, OR9(b2), modifies the operation of crc Corrupt, BR8(b3). When OR9(b2) is a 1, the operation of the crc Corrupt bit, BR8(b3), is modified so that a corrupt crc is transmitted only to the end of the current U–interface superframe. Then BR8(b3) is cleared to a 0. If it is desired to corrupt the transmitted crc again, then BR8(3) must be set to a 1 again. This is very useful for digital loop carrier applications, since software does not have to clear BR8(b3) in order to guarantee a one–to–one correspondence between crc received from the digital loop carrier system and crcs transmitted onto the U–interface. For digital loop carrier applications, BR9(b1) is set to a 1 if it is desired to have end–to–end performance monitoring. The outgoing febe should be updated at the same time that the outgoing M4 channel register is updated. This update should be done for every superframe.

7.7 MAINTENANCE CHANNEL INTERRUPTS AND UPDATES

This section provides details on when interrupts are generated and when the internal Superframe Framer reads maintenance channel registers to include their contents in the outgoing transmitted superframe. This information is particularly useful when designing LUNT and LULT line cards for digital loop carrier systems. The basic frames and Quat positions are numbered as in the ANSI T1.601 specification. A Quat is the ANSI T1.601 term for the symbols transmitted over the U–interface. Basic frames are numbered from 1 through 8. The Quats in each basic frame are numbered from 1 through 120.

The M4, M5/M6, and eoc maintenance subchannels can be used for signalling in proprietary applications. When the M4 or M5/M6 subchannels are configured to update on every received frame in the subchannel, the update interval is 12 ms or once every superframe. The receive data interrupt for the M5/M6 subchannel occurs at the end of basic frame 4. The receive data interrupt for the M4 channel occurs at the end of the superframe or basic frame 8. See Figures 7–1, 7–2 and 7–3, and register BR9 description for more details.

When the eoc subchannel is configured to update on every received eoc frame, the update interval is 6 ms, or twice each superframe. The eoc receive data interrupt can occur at the end of basic frame 4 or at the end of basic frame 8. See register description for BR9 for more details.

The receive and transmit registers for the maintenance channels are double buffered. Figure 7–2 indicates where maintenance channel registers are updated from the superframe received at NT. Figure 7–2 also indicates the points where the U–interface transceiver transfers data from the maintenance channel registers into the transmitted superframe when the MC145572 is configured for NT mode. Figure 7–3 indicates where maintenance channel registers are updated from the superframe received at the LT end of the loop. Figure 7–3 also indicates the points where the U–interface transceiver transfers data from the maintenance channel registers into the transmitted superframe when the MC145572 is configured for LT mode.

For digital loop carrier applications, maintenance channel registers R6, BR1, and BR3 must be programmed to update on every received frame. Do not use trinal or dual consecutive checking. The reason for this, is intermediate nodes need to do local processing of the eoc messages and must transmit the messages upstream or downstream on a frame–by–frame basis. See explanations for Byte register 9. Note that the eoc maintenance subchannel R6 is updated with a new received eoc message twice each superframe. The MC145572 should be configured so that interrupts are generated when BR1, BR3, and R6 are updated. See explanations for Nibble registers 3 and 4. The interrupt for BR3 ($\overline{IRQ0}$) may not need to be enabled, since BR3 is updated at the same time as R6 at the end of a superframe. When an interrupt occurs, data can be read from the appropriate maintenance channel register (BR1, BR3, or R6) and transmitted over the digital loop carrier system. At this time, the maintenance channel data that has been received from the digital loop carrier system can be written to the registers for the outgoing superframe (BR0, BR2, or R6).

If the M4 channel and eoc interrupts are enabled to occur on the reception of every frame, it is possible for the software to determine if eoc interrupt has occurred at the end of basic frame 4 or at the end of basic frame 8. When eoc interrupt occurs at the end of basic frame 4, eoc interrupt status bit, NR3(b2), is set and M4 channel interrupt status bit, NR3(b1), is clear assuming that M4 channel register, BR1, was read immediately following the previous M4 channel interrupt. When eoc interrupt and M4 interrupts occur at the end of basic frame 8, both NR3(b2) and NR3(b1) are set.

The MC145572 does not provide any direct mechanism whereby an external microcontroller can determine when registers, for outgoing maintenance data, can be updated. This timing must be

derived from the interrupts generated when the receive maintenance subchannel registers are updated. Figures 7–2 and 7–3 show the appropriate timings. It is possible to configure the TxSFS/SFAX/S0 pin as SFAX and use the pulse to generate a 12–ms periodic interrupt. Note though that SFAX indicates the 2B+D frame in the IDL2 interface that will be transmitted onto the first 2B+D position in basic frame 1 of the U–interface superframe. Due to the internal FIFOs, it is not possible to guarantee a fixed time between SFAX and the location of the superframe marker on the U–interface.

At the NT end, the ANSI T1.601 specification requires a turnaround delay of 60 ± 2 quats. The MC145572 has a 60–quat turnaround time. This means that the transmitted Superframe Sync word occurs 60 quats later than the received Superframe Sync word. From an interrupt service routine point of view, updating BR0, BR2, and R6, the worst case time should be assumed to be 60 quats + 117 quats = 177 quats, or 2.2 ms. The system software designer should allow extra margin to be safe. A quat is 12.5 μs in duration.

At the LT end of the loop, the received Superframe Sync word is 60 – 2 + 8 quats later than the transmit Superframe Sync word. The 2–quat uncertainty comes from the ANSI T1.601 specification for NT turnaround time of 60 ± 2 quats on a 0 length loop. The + 8 figure includes worst case propagation delay on an 18,000–foot loop. From an interrupt service routine point of view, the worst case assumption is that the receive Superframe Sync word occurs 68 quats after the transmitted Superframe Sync word. For example, from Figure 7–3, the time between when R6 is updated with the receive eoc data and when R6 must be updated with the transmitted eoc data, can be calculated as follows: 117 – 68 = 49 quats or 612.5 μs. The system software designer should leave extra margin to be safe.

8

GCI MODE FUNCTIONAL DESCRIPTION

8.1 FUNCTIONAL OVERVIEW

The MC145572 is configurable for the General Circuit Interface or GCI operation. GCI is a time division multiplex bus, that combines the ISDN 2B+D data and control/status information onto four signal pins. There are two clocks per data bit and a single frame synchronization pulse, FSC.

In GCI mode, the MC145572 supports the full set of commands and indications over the Command/Indicate channel. The monitor channel is used for sending and receiving maintenance channel messages and accessing the internal MC145572 registers.

As a GCI slave, the MC145572 accepts clock frequencies between 512 kHz and 8.192 MHz. As a GCI master, the MC145572 operates at either 512 kHz or 2.048 MHz. Figure 8–1 is a typical configuration for the MC145572 in GCI mode. The MC145572 is configured for GCI operation when the MCU/GCI pin is tied low. The PAR/SER pin must also be tied low.

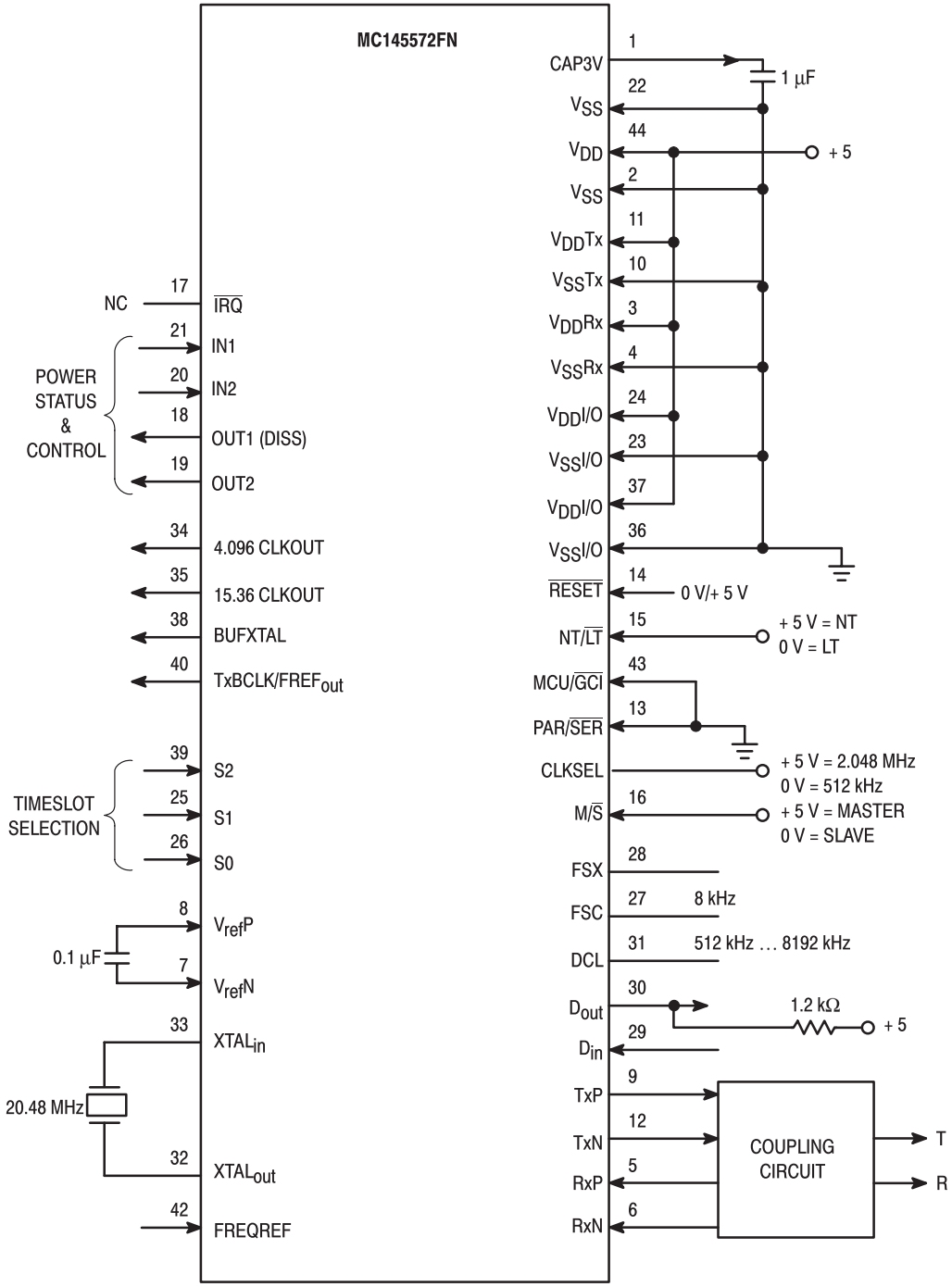


Figure 8–1. MC145572 Configuration for GCI Operation

Table 8–1. GCI Master Mode Clock Rate Selection

Clock Rate	CLKSEL
512 kHz	0
2.048 MHz	1

8.2 INTERFACE SIGNALS

Seven signal pins are available for the time division multiplex bus interface in GCI mode.

- S2, S1, S0 — Used to select the active GCI channel in multiplexed GCI frames.
- DCL — 2x data clock.
- FSC — The 8 kHz frame synchronization pulse.
- D_{in} — The MC145572 reads data from the GCI interface into this pin during the active GCI channel selected by S2, S1, S0.
- D_{out} — In GCI mode, this pin is an open drain output and must be pulled to V_{DD} through a resistor. The MC145572 outputs data to the GCI interface from this pin during the active GCI channel selected by S2, S1, S0.

During all other GCI channels, if present, D_{out} is off. D_{in} accepts data during the channel selected by S0, S1, and S2. During other GCI channels, if present, D_{in} ignores any data that is present.

8.3 GCI FRAME STRUCTURE

The GCI interface supports two types of frame formats: the single GCI channel and the multiplexed GCI channel formats. A single GCI channel has the following subchannels: two B channels, Monitor channel, ISDN D channel, Command/Indicate channel, and A and E bits. See Figure 8–2.

Referring to Figure 8–2, the two B channels are used to convey customer data between the MC145572 and other GCI devices. The Monitor channel bits are used to convey register and maintenance information between the MC145572 and other GCI devices. The D bits carry the ISDN basic access D channel. The Command/Indicate bits are used for activation and deactivation of the MC145572 and for control functions. The A and E bits are used as handshake signals during the transfer of monitor channel messages.

A multiplexed GCI frame contains from two to eight GCI frames in each 125 µs period. Table 8–2 summarizes the number of GCI frames that can be multiplexed into a 125 µs period. Figure 8–3 shows how multiple GCI frames are multiplexed into a 125 µs period.

Table 8–2. Multiplexed GCI Frame Configuration

Mode	Clock	Maximum GCI Frames in Multiplex
GCI Master	512 kHz	1
GCI Master	2.048 MHz	4
GCI Slave	512 kHz	1
GCI Slave	4.096 MHz	8

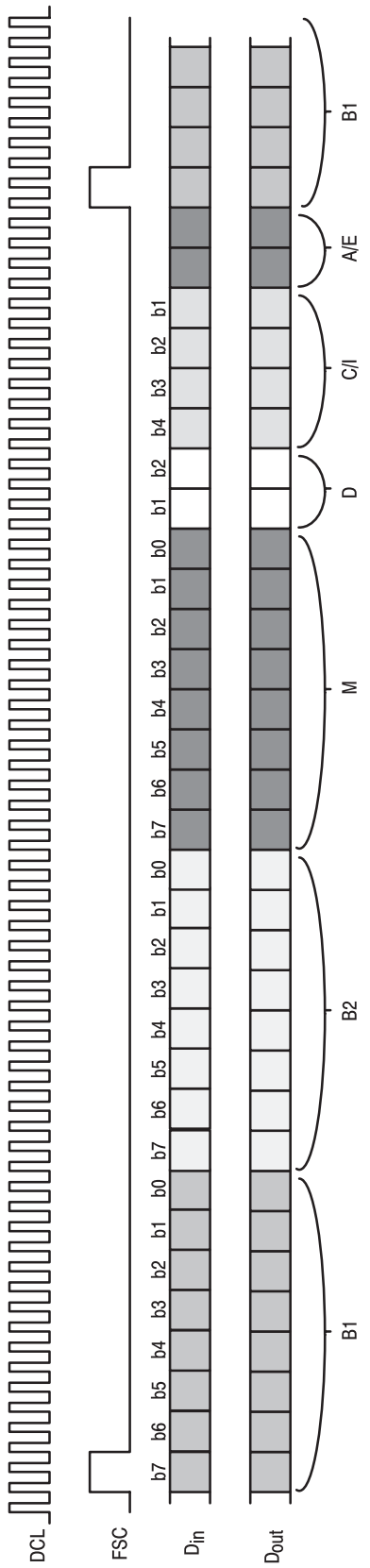


Figure 8–2. Single Channel GCI Format

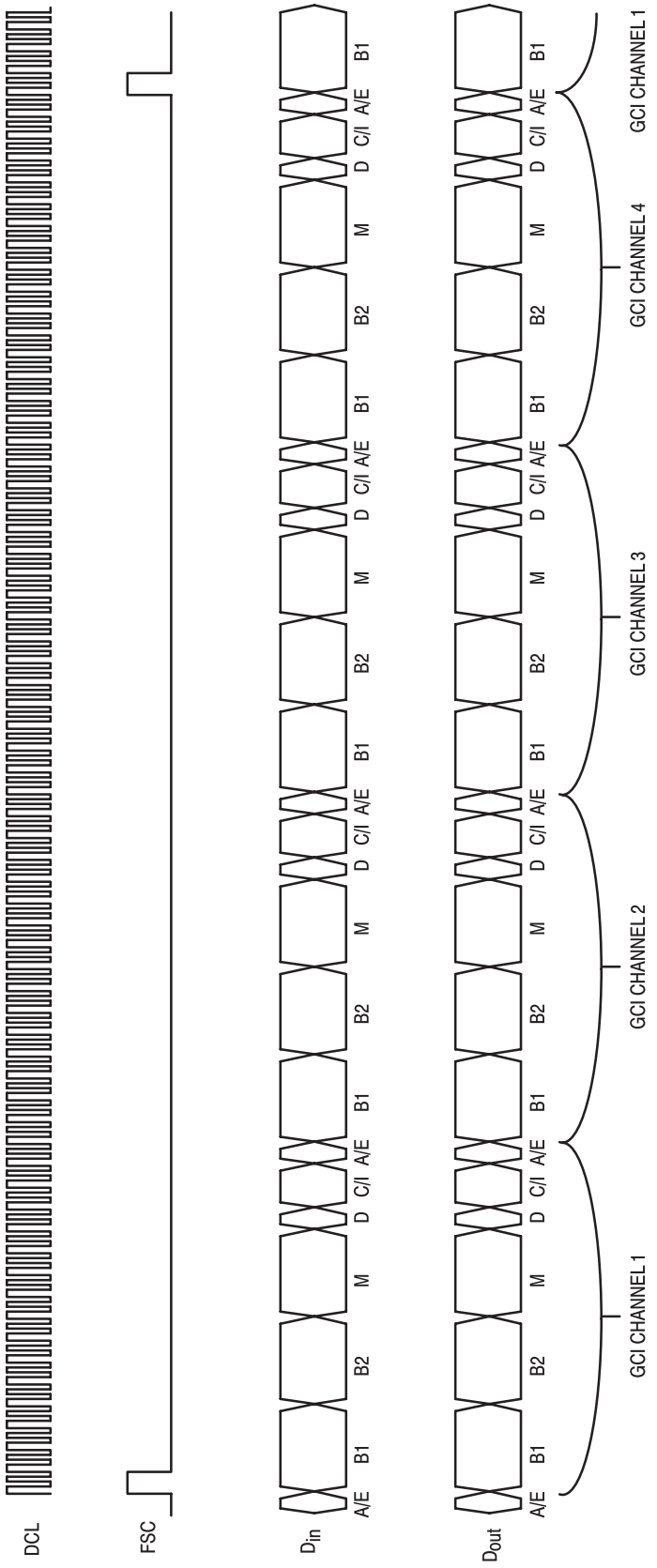


Figure 8–3. Multiplexed GCI Format Example

8.3.1 Monitor Channel Operation

The Monitor channel is used to access the internal registers of the MC145572 in order to support U–interface maintenance channel operations. All Monitor channel messages are two bytes in length. Each byte is sent twice to permit the receiving GCI device to verify data integrity. In ISDN applications, the Monitor channel is used for access to the U–interface maintenance messages.

The A and E bits in the GCI channel are used to control and acknowledge Monitor channel transfers between the MC145572 and another GCI device. When the Monitor channel is inactive, the A and the E bit times from D_{out} are both high impedance. The A and E bits are active when they are driven to V_{SS} during their respective bit times. Pull-up resistors are required on D_{in} and D_{out}. The E bit indicates the transmission of a new Monitor channel byte. The A bit from the opposite direction is used to acknowledge the Monitor channel byte transfer.

An idle Monitor channel is indicated by both A and E bits being inactive for two GCI frames. The A and E bits are high impedance when inactive. The Monitor channel data is $FF.

The originating GCI device transmits a byte onto the Monitor channel after receiving the A and E bits equal to 1 for at least two consecutive GCI frames. The originating GCI device also sets its outgoing E bit to 0 in the same GCI frame as the byte that is transmitted. The transmitted byte is repeated for at least two GCI frames, or is repeated in subsequent GCI frames, until the MC145572 acknowledges receiving two consecutive GCI frames containing the same byte.

Once the MC145572 acknowledges the first byte, the sending device sets E to high impedance and transmits the first frame of the second byte. Then, the second byte is repeated with the E bit low until it is acknowledged. See Figures 8–4 through 8–8 for details of Monitor channel procedure.

The destination GCI device verifies that it has received the first byte by setting the A bit to 0 towards the originating GCI device for at least two GCI frames. Successive bytes are acknowledged by the receiving device setting A to high impedance on the first instance of the next byte, followed by A being cleared to 0 when the second instance of the byte is received.

The entire register set of the MC145572 can be accessed via the Monitor channel. All M4 channel activity is automatically handled by the MC145572 when configured for GCI mode. The MC145572 issues Monitor channel messages whenever the received eoc, M4, or M5/M6 messages received from the U–interface change, and appropriate dual–checking or trinal–checking of bits has been done. In normal GCI operation it is not necessary to read or write the internal registers of the MC145572.

If the receiving GCI device does not receive the same Monitor channel byte in two consecutive GCI frames, it indicates this by leaving A = 0 until two consecutive identical bytes are received. The last byte of the sequence is indicated by the originating GCI device setting its E bit to a 1 for two successive GCI frames. Figure 8–5 shows an example of an delayed GCI Monitor channel message.

8.3.2 Monitor Channel Messages and Commands

The MC145572 supports three basic types of Monitor channel messages. The first group of messages are commands that read or write the internal register set of the MC145572. See **Chapter 4** for a complete description of the MC145572 register set. The second group of messages are responses from the MC145572. These responses are transmitted by the MC145572 after it receives a register read or write command over the Monitor channel. The third group of Monitor channel messages are interrupt indication messages. These are transmitted by the MC145572 whenever a change is detected in the Maintenance Channel Receive registers BR1, BR3, or R6.

8.3.2.1 MONITOR CHANNEL COMMANDS

A GCI device transmits Monitor channel commands to a receiving MC145572 to gain access to its internal register set. The receiving MC145572 then transmits a Monitor channel response message onto the Monitor channel for commands that request data to be read from an internal register. Commands that write data to an internal MC145572 register are accepted and acted upon, but the MC145572 does not issue a response message. Monitor channel commands are given in Table 8–3.

The MC145572 acknowledges all messages it receives over the Monitor channel. If an invalid message is received, the MC145572 acknowledges it, but does not take any action.

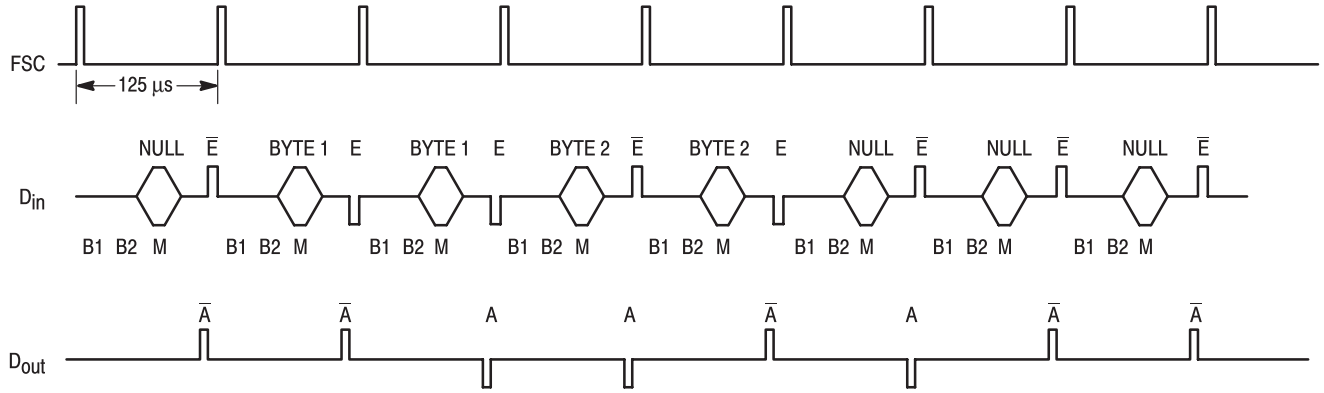


Figure 8–4. Monitor Channel Access Protocol

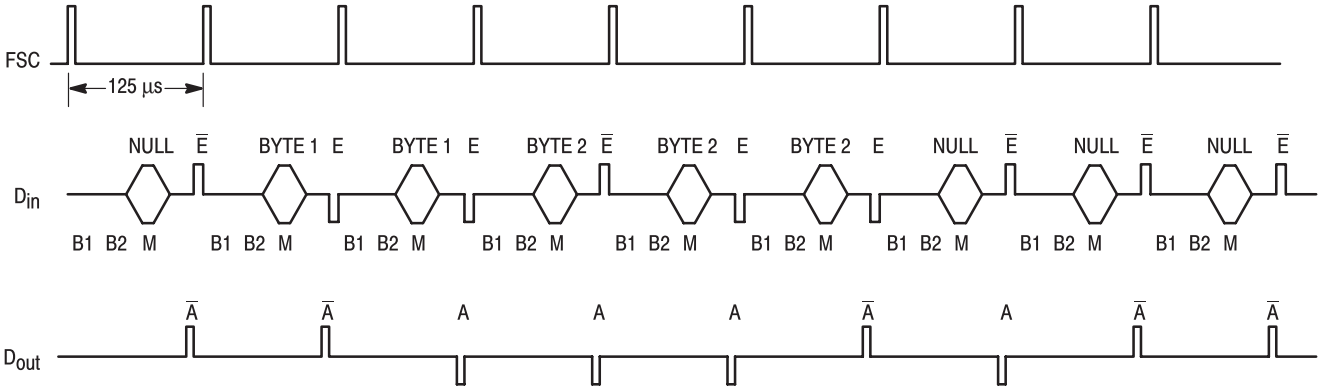


Figure 8–5. Monitor Channel Protocol with Delay

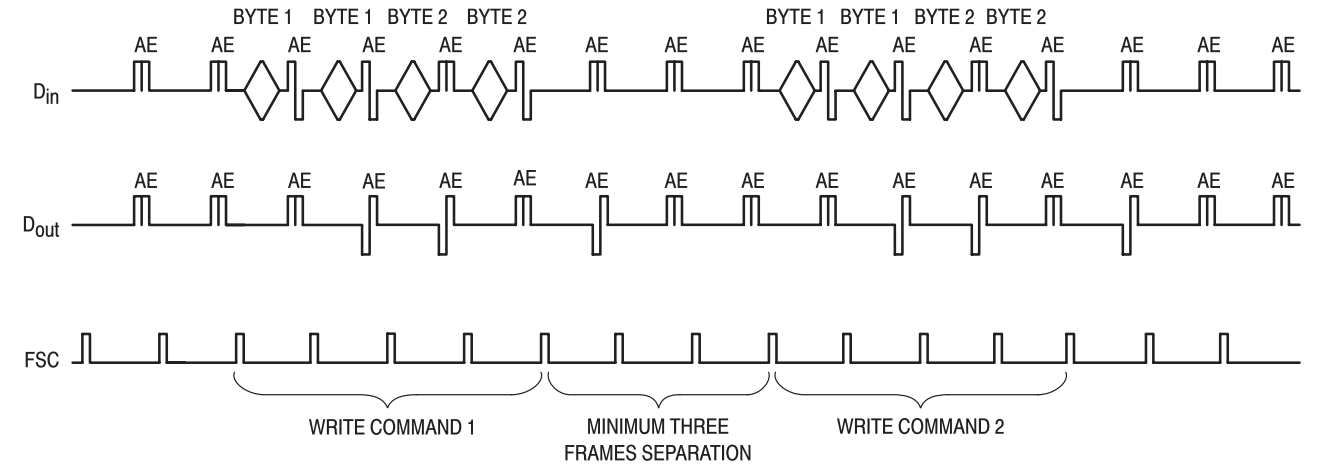


Figure 8–6. Monitor Channel Register Write Sequence

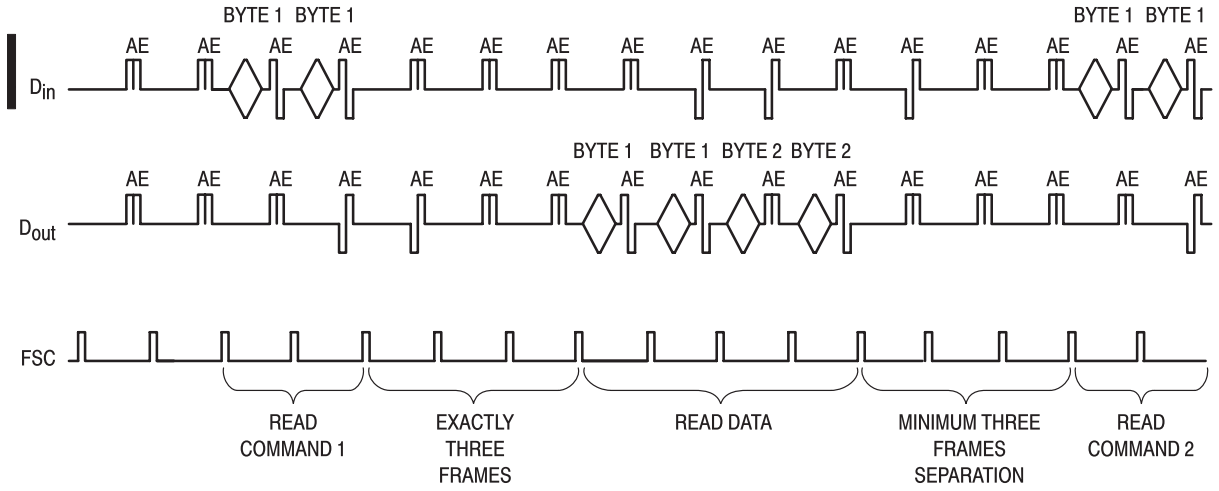


Figure 8–7. Monitor Channel Register Read Sequence

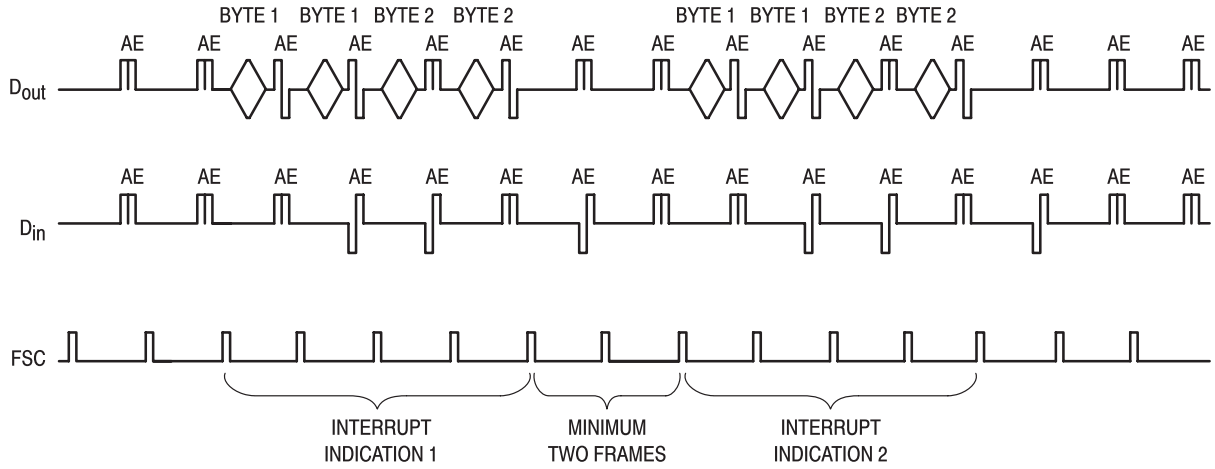


Figure 8–8. Monitor Channel Multiple Interrupt Indications Sequence

Table 8–3. Monitor Channel Commands

Byte 1								Byte 2								
msb							lsb	msb							lsb	
b17	b16	b15	b14	b13	b12	b11	b10	b27	b26	b25	b24	b23	b22	b21	b20	
0	0	0	0	ba3	ba2	ba1	ba0	d7	d6	d5	d4	d3	d2	d1	d0	Byte Write
0	0	0	1	ba3	ba2	ba1	ba0									Byte Read
0	0	1	0	na3	na2	na1	na0	d3	d2	d1	d0	x	x	x	x	Nibble Write
0	0	1	1	na3	na2	na1	na0									Nibble Read
0	1	0	1	0	0	0	0									eoc Read
0	1	1	0	a1	a2	a3	dm	i1	i1	i3	i4	i5	i6	i7	i8	eoc Write
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Device Identification
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	NOP

NOTES:

1. For byte register accesses, the address range of ba3, ba2, ba1, ba0 is hexadecimal 0 – F. The bits d7 through d0 are data that is written to the byte register.
2. For nibble register accesses, the address range of na3, na2, na1, na0 is hexadecimal 0 – 5. The bits d3 through d0 are data that is written to a nibble register.
3. The bits a1 through a3, dm, and i1 through i8 are data that is written to the eoc register.
4. For non–ISDN applications, the data written to the eoc register uses the convention that bit a1 is the most significant bit and bit i8 is the least significant bit.
5. The receiving device does not issue a response to a register write command.
6. Byte or nibble read commands consist of byte 1 only. Byte 2 is not transmitted to the MC145572. In response to a read command, the MC145572 responds with two bytes as indicated in Table 8–4. See Figure 8–7.

8.3.2.2 MONITOR CHANNEL RESPONSE MESSAGES

The Monitor channel response messages are transmitted onto the GCI Monitor channel by the MC145572 in response to a register read command. The Monitor channel response messages are given in Table 8–4.

Table 8–4. Monitor Channel Response Messages

b17	b16	b15	b14	b13	b12	b11	b10	b27	b26	b25	b24	b23	b22	b21	b20	
0	0	0	1	ba3	ba2	ba1	ba0	d7	d6	d5	d4	d3	d2	d1	d0	Byte Read
0	0	1	1	na3	na2	na1	na0	d3	d2	d1	d0	x	x	x	x	Nibble Read
0	1	0	1	a1	a2	a3	dm	i1	i1	i3	i4	i5	i6	i7	i8	eoc Read
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Device Identification

NOTES:
1. If a maintenance channel is updated in the MC145572 receive deframer at the same time a register read command is received, then an interrupt indication message is issued first. The indication message takes priority over requests for register reads. All queued interrupt indication messages are issued before the response to the register read message. It is important for software to always check the message code in byte 1 of any received message.
2. The bits a1 through a3, dm, and i1 through i8 are data that is read from the eoc register. The bits d7 through d0 are data that is read from a register.
3. For non–ISDN applications, the data written to the eoc register uses the convention that bit a1 is the most significant bit and bit i8 is the least significant bit.

8.3.2.3 MONITOR CHANNEL INTERRUPT INDICATION MESSAGES

The Monitor channel interrupt indication messages are *automatically* transmitted onto the GCI Monitor channel by the MC145572 when its receiver deframer updates one of the maintenance channel registers BR1, BR3, or eoc register R6. The maintenance channel registers are updated when the trinal checking of bits or messages has been completed. All outstanding interrupt indication messages are transmitted prior to any response messages being transmitted. The Monitor channel interrupt indication messages are given in Table 8–5.

When a Monitor channel interrupt indication message is transmitted by the MC145572, the corresponding internal register is read and the interrupt is automatically cleared.

Table 8–5. Monitor Channel Interrupt Indication Messages

b17	b16	b15	b14	b13	b12	b11	b10	b27	b26	b25	b24	b23	b22	b21	b20	
0	0	0	0	0	0	0	0	d7	d6	d5	d4	d3	d2	d1	d0	M5/M6 int.
0	0	1	0	0	0	0	0	d7	d6	d5	d4	d3	d2	d1	d0	M4 int.
0	1	0	0	a1	a2	a3	dm	i1	i1	i3	i4	i5	i6	i7	i8	eoc int.

NOTES:
1. The bits a1 through a3, dm, and i1 through i8 are data that is read from eoc register R6.
2. For non–ISDN applications, the data read from the eoc register uses the convention that bit a1 is the most significant bit and bit i8 is the least significant bit.
3. The data byte returned by the M5/M6 interrupt corresponds to the byte as read from Byte register BR3 in the SCP interface mode register map. The bits d7 through d0 are data that is read from a register.
4. The data byte returned by the M4 interrupt corresponds to the byte as read from Byte register BR1 in the SCP interface mode register map.

8.3.3 Command/Indicate Channel Operation

The Command/Indicate, or C/I channel, is used to activate and deactivate the MC145572. Some control functions such as loopbacks are also supported over the C/I channel. C/I codes are four bits in length and must be received for two consecutive GCI frames before they are acted upon.

C/I channel bits are numbered bit 4 through 1, with bit 4 being the most significant bit. The C/I/ channel bits are transmitted starting with bit 4.

C/I channel commands are used to activate, or deactivate the MC145572. They are also used to implement loopbacks and perform control functions. Some C/I channel commands may cause the MC145572 to issue a C/I channel response. Table 8–6 summarizes the C/I channel commands and indications.

C/I channel indications are used to notify a layer 2 device, that certain events have occurred, such as a change in activation status.

In normal GCI operation, the M4 channel `act`, `dea`, `uoa`, `sai`, `ps1`, `ps2`, and reserved status bits are handled automatically. It is possible to set bits in the MC145572 register map using Monitor channel commands that will override the automatic operation of the M4 channel.

Table 8–6. C/I Channel Commands and Indications

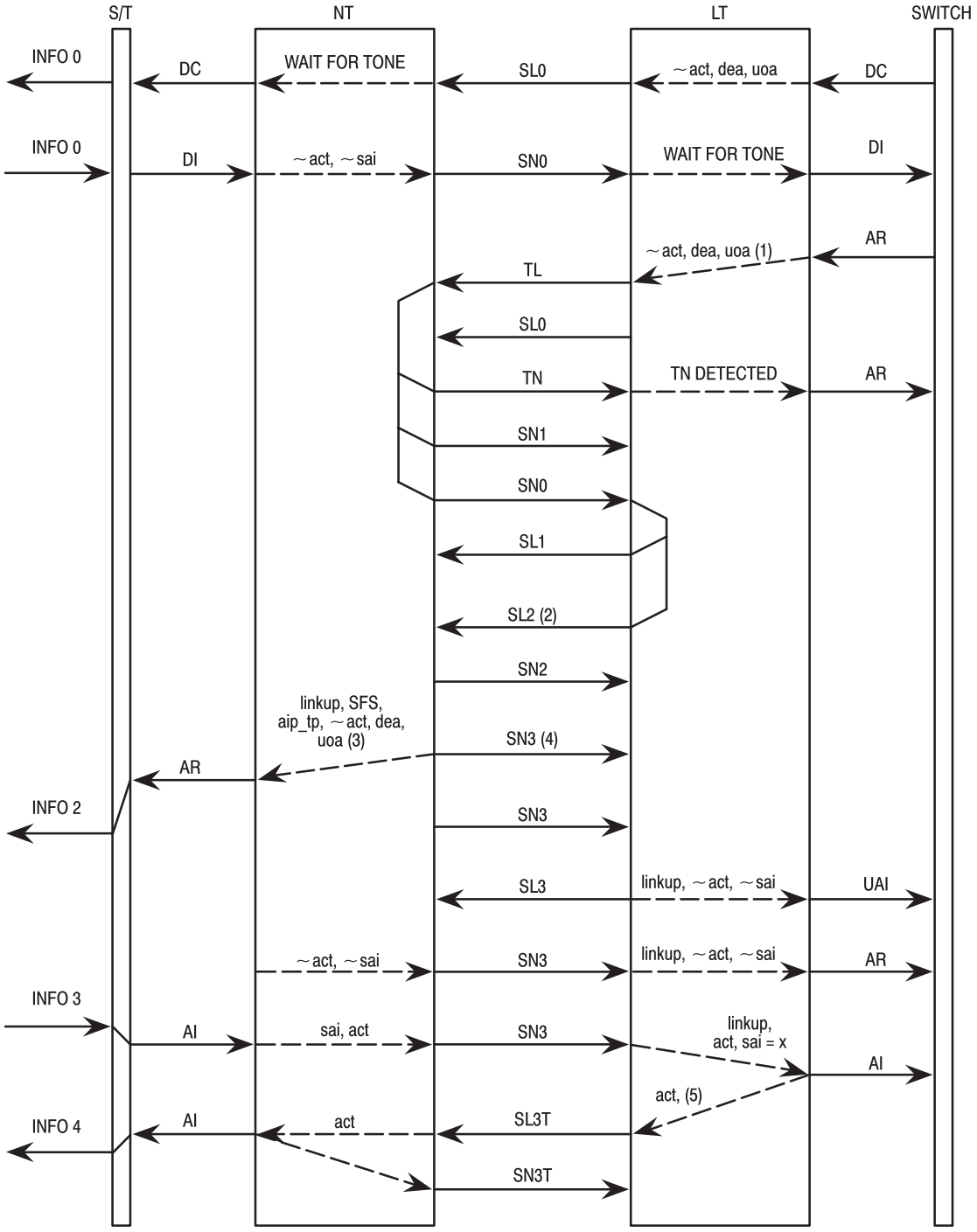
C/I Codeword				LT Mode		NT Mode	
b4	b3	b2	b1	Command	Indication	Command	Indication
0	**0**	0	0	**DR**	**—**	**—**	**DR**
0	**0**	0	1	**RES**	**DEAC**	**RES**	**—**
0	**0**	1	0	**LTD2**	**—**	**NTD2**	**—**
0	**0**	1	1	**LTD1**	**—**	**NTD1**	**—**
0	**1**	**0**	**0**	**—**	**RSY**	**—**	**RSY**
0	**1**	**0**	**1**	**—**	**EI2**	**—**	**EI2**
0	**1**	**1**	**0**	**—**	**—**	**—**	**—**
0	**1**	**1**	**1**	**UAR**	**UAI**	**—**	**—**
1	**0**	0	0	**AR**	**AR**	**AR**	**AR**
1	**0**	0	1	**—**	**—**	**—**	**—**
1	**0**	1	0	**ARL**	**—**	**ARL**	**—**
1	**0**	1	1	**—**	**—**	**—**	**—**
1	**1**	**0**	**0**	**—**	**AI**	**AI**	**AI**
1	**1**	**0**	**1**	**—**	**—**	**—**	**—**
1	**1**	**1**	**0**	**—**	**—**	**—**	**AIL**
1	**1**	**1**	**1**	**DC**	**DI**	**DI**	**DC**

NOTES:

AI	Activation indication	AR	Activation request
AIL	2B+D loopback received over eoc channel, perform loopback at S/T interface in 2–chip NT1	DC	Deactivation confirm
		DI	Deactivation indication
ARL	Activation request with local analog loopback	EI2	Error indication
DEAC	Deactivation request accepted	LTD2	(LT mode), NTD2 (NT mode), set pin “OUT2” high when command is active
DR	Deactivation request		
LTD1	(LT mode), NTD1 (NT mode), sets pin “OUT1” high when command is active	RSY	Loss of sync – resync requested
		UAR	U–only activation request
RES	Reset		
UAI	U–only activation indication		

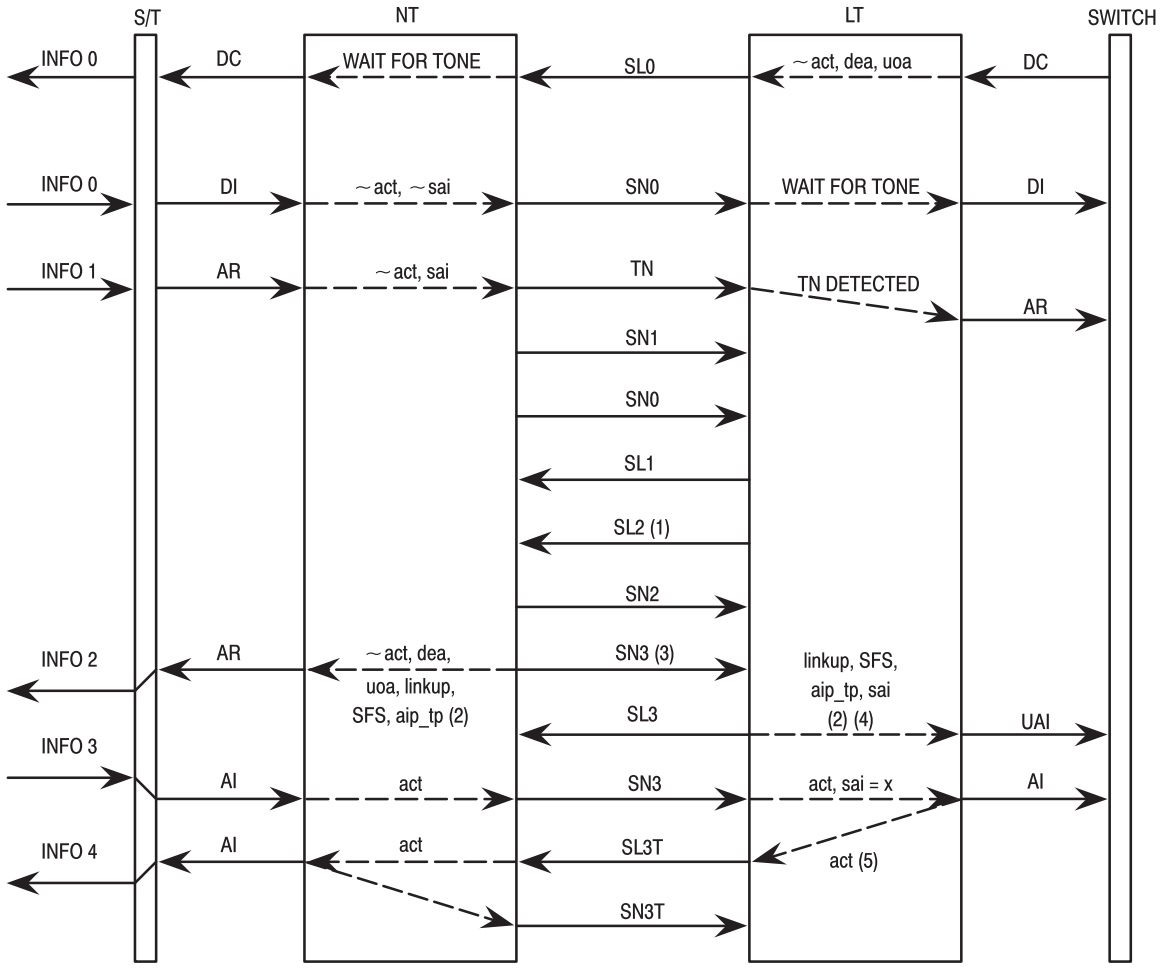
8.4 GCI ACTIVATION AND DEACTIVATION TIME DIAGRAMS

This section contains the time flow diagrams that detail the various activation and deactivation scenarios for the MC145572 U–interface transceiver. Figures 8–9 through 8–17 are the activation diagrams for the MC145572 operating in GCI mode. Figures 8–18 and 8–19 are the activation state diagrams for NT and LT mode operation.



NOTES:
1. No change in transmitted maintenance bits at this time.
2. Maintenance bits are sent with meaningful data (‘Normal’ field in Table 5, T1E1.4).
3. linkup, SFS, aip_tp correspond to NR1 bits 3, 1, and 0, respectively.
4. No change in upstream maintenance bits: act = 0, sai = 0.
5. The downstream act bit is set by issuance of the AI indication.

Figure 8–9. Time Diagram for Total Activation Initiated by the Network



NOTES:
1. Maintenance bits are sent with meaningful data (‘Normal’ field in Table 5, T1E1.4).
2. linkup, SFS, aip_tp correspond to NR1 bits 3, 1, and 0, respectively.
3. No change in upstream maintenance bits: act = 0, sai = 0.
4. Because the upstream sai bit was set by the (upstream) AR command, the indication UAI will never be issued and AR continues to appear on the C/I channel.
5. The downstream act bit is set by issuance of the AI indication.

Figure 8–10. Time Diagram for Total Activation Initiated by the Terminal Equipment

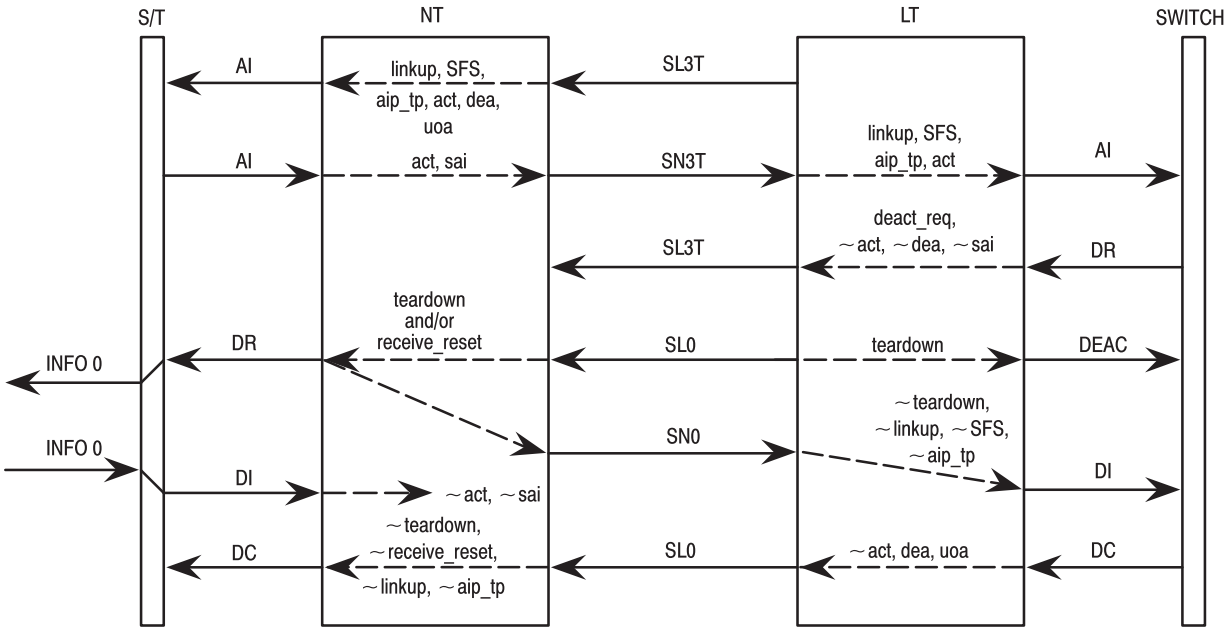


Figure 8–11. Time Diagram for Deactivation (Always Initiated by the Network)

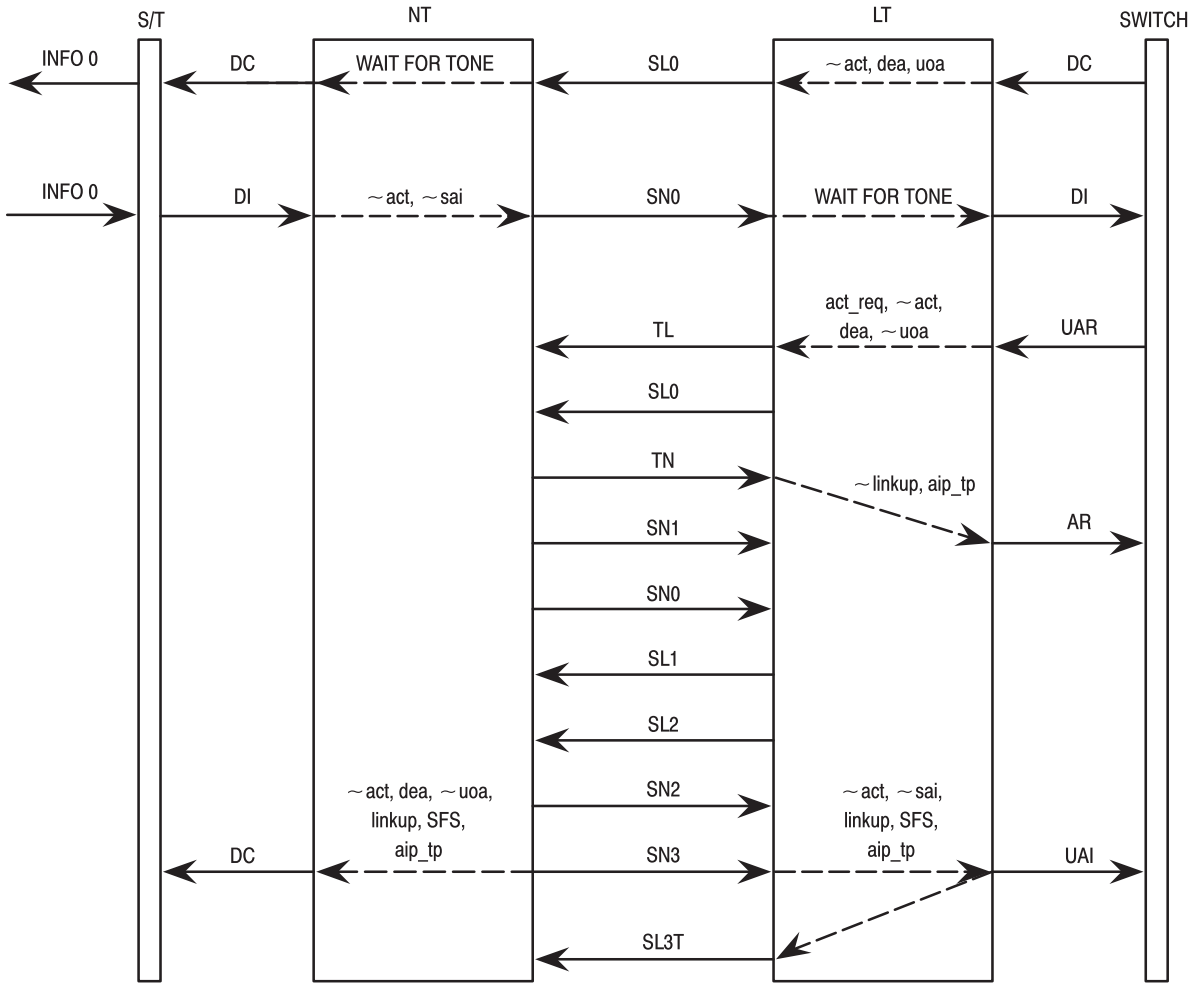


Figure 8–12. Time Diagram of a U–Only Activation (Always Initiated by the Network)

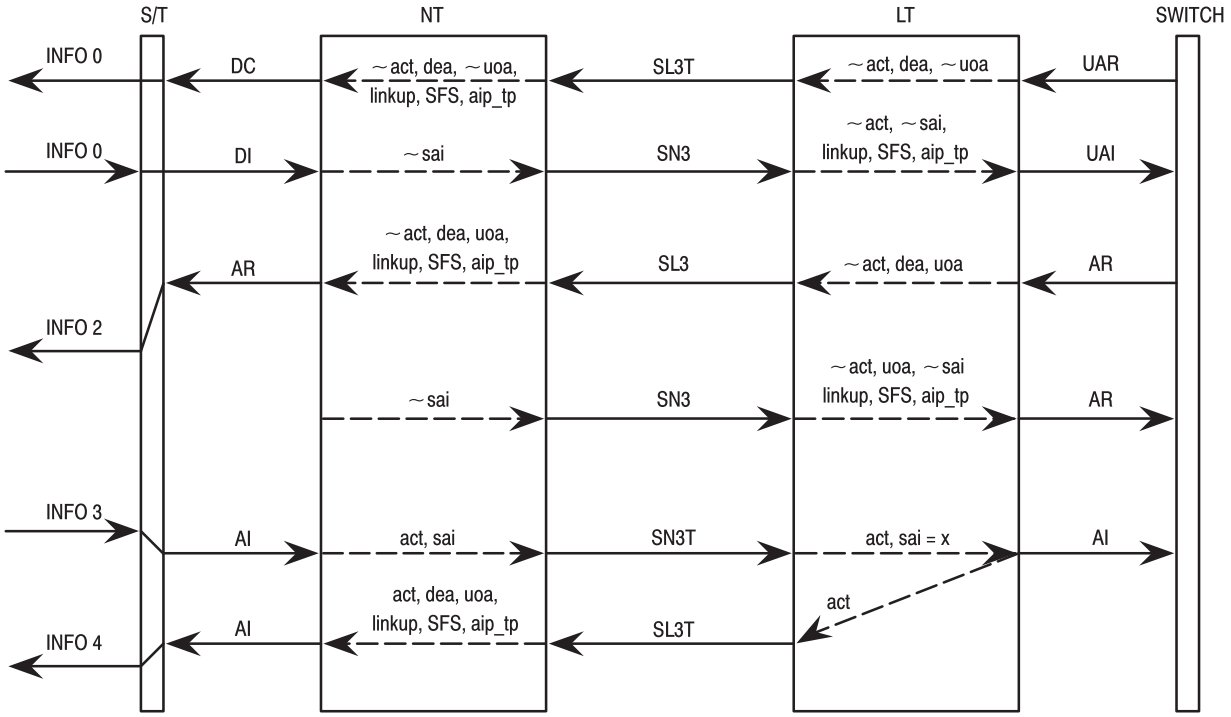


Figure 8–13. Time Diagram for a Transition from DSL–Only Activation to Total Activation Initiated by the Network

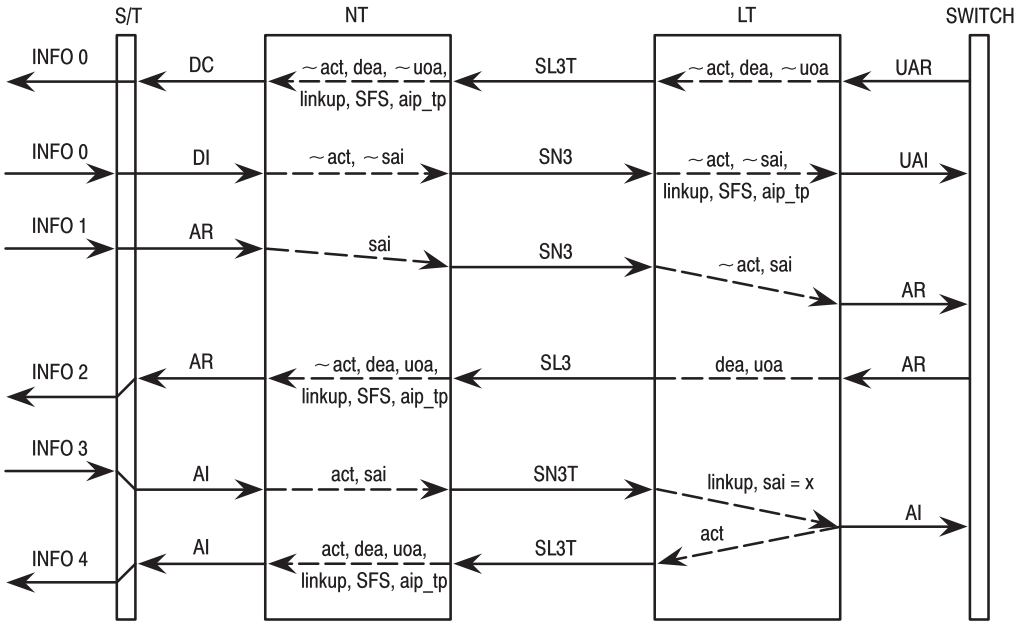
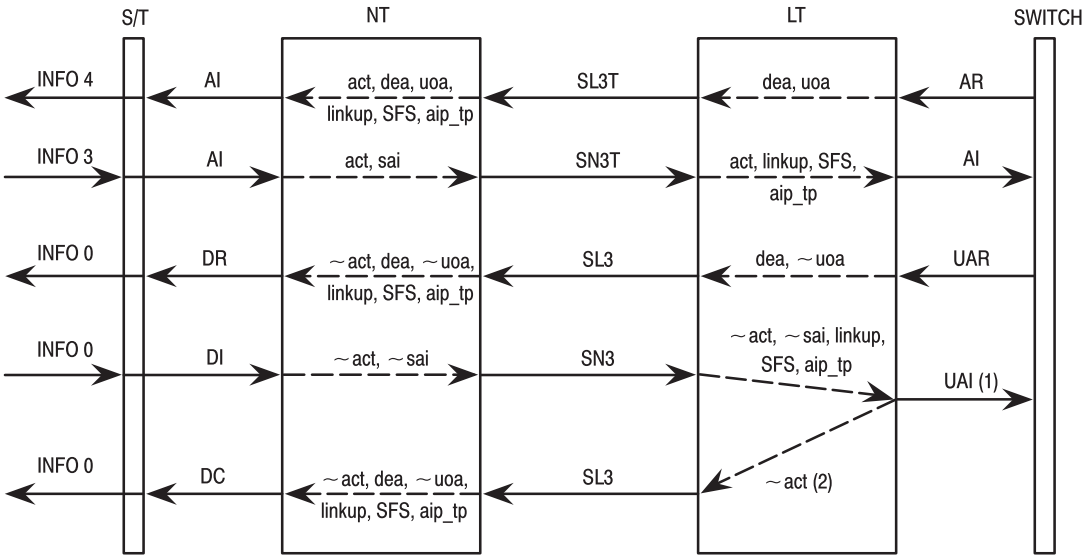


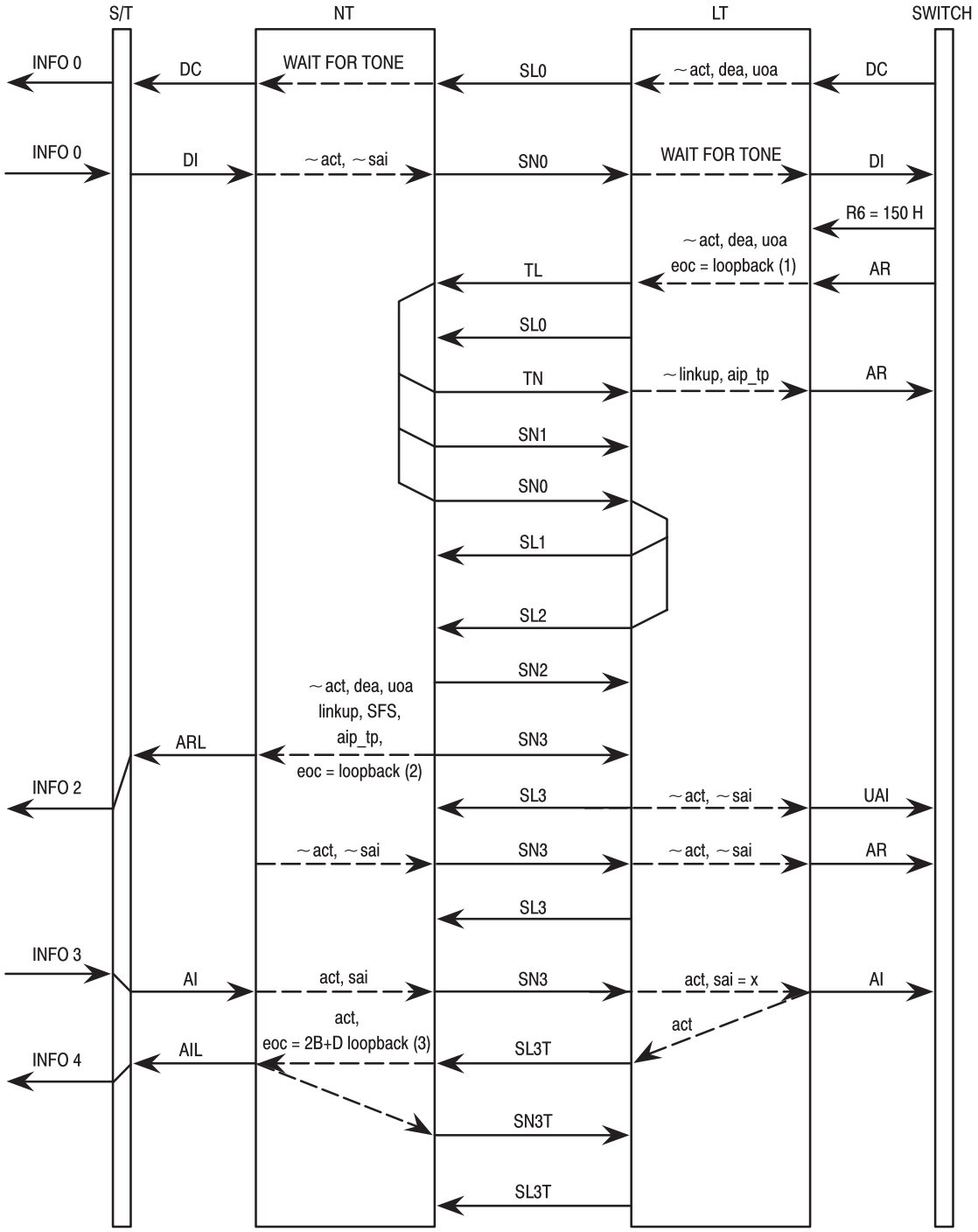
Figure 8–14. Time Diagram for a Transition from DSL–Only Activation to Total Activation Initiated by the Terminal Equipment



NOTES:

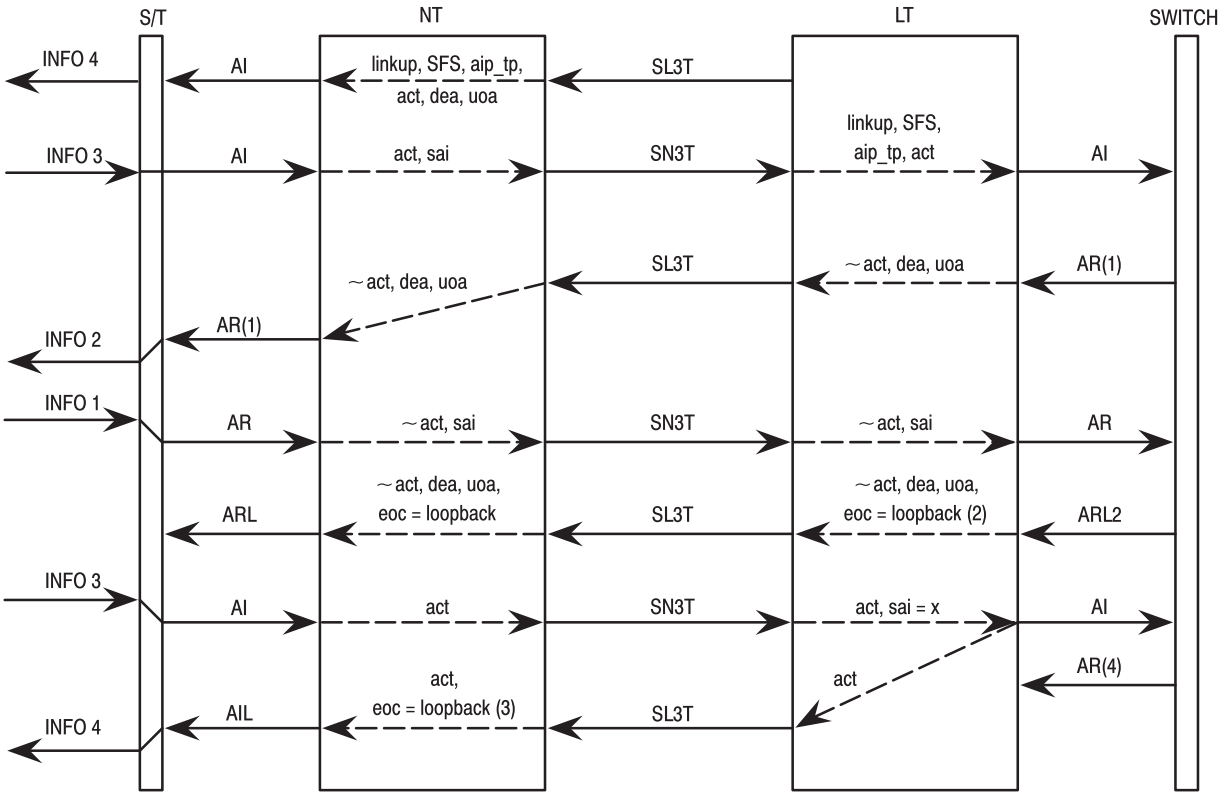
1. In the event that received act = 0 and sai = 0 do not occur at the same time in LT, it is possible that prior to the UAI indication, AR will be issued by LT, until the moment in which both maintenance bits are 0 in LT. Then, UAI will be issued, as shown.
2. The state of the act bit is automatically reset by the MC145572, without the need to issue a special command to do this.

Figure 8–15. Time Diagram for a Transition from Total Activation to DSL–Only Activation (Always Initiated by the Network)



NOTES:
1. Monitor channel is used to write eoc 2B+D loopback command to R6 prior to activation.
2. In NT mode, the MC145572 may detect the trinal–checked eoc message about the same time it validates the first set of received maintenance bits. Then, it shall issue an ARL indication instead of an AR.
3. The MC145572 issues an AIL indication for as long as loopback is active.

Figure 8–16. Time Diagram for Activation with Loopback 2 (Always Initiated by the Network)



NOTES:
1. According to recommendation T1E1.4/92–194, LT initiates request by lowering act bit.
2. LT requests loopback by means of eoc message.
3. Part will issue an AIL indication for as long as loopback is active.
4. LT will hold sending the downstream act bit until the eoc loopback message is acknowledged.

Figure 8–17. Time Diagram for Execution of Loopback 2 Once Link is Active (Always Initiated by the Network)

8.5 GCI MASTER AND SLAVE MODE OPERATION

The MC145572 can be configured for GCI master or GCI slave operation independently of LT or NT configuration. When the pin M/$\overline{S}$ is pulled low to V_{SS}, GCI slave operation is selected. When the pin M/$\overline{S}$ is pulled high to V_{DD}, GCI master operation is selected. When configured as a slave, FSC is an input driven by external circuitry. FSC must be synchronized to the clock applied to DCL. When configured as a master, the MC145572 drives FSC as an output.

8.6 U-INTERFACE SUPERFRAME ALIGNMENT

The MC145572 uses the FSC signal to indicate superframe alignment. In LT mode as a GCI slave, the FSC pin is used to force alignment of the transmitted U–interface superframe. Normally, the FSC pulse is two DCL clocks in duration. Alignment of the transmitted superframe can be forced by driving FSC with a one DCL clock wide pulse, once every 96 GCI frames. The 2B+D data read into the D_{in} pin following the single clock wide FSC, corresponds to the first 2B+D transmitted onto the U–interface. If superframe alignment is not input to FSC, the MC145572 aligns the outgoing U–interface superframe.

When configured for master mode and either LT or NT operation, reception of the first 2B+D data from the U–interface superframe is indicated by the MC145572 outputting a FSC pulse that is one DCL clock wide. This happens once every 96 GCI frames.

In NT mode, IDL2 slave operation, any superframe alignment information that may be present on FSC is ignored. ANSI T1.601 defines when the NT transmitted superframe occurs with respect to the received superframe.

WARNING

If FSC is to be used to set the alignment of the transmitted superframe in LT mode, it must be stable prior to activating the MC145572.

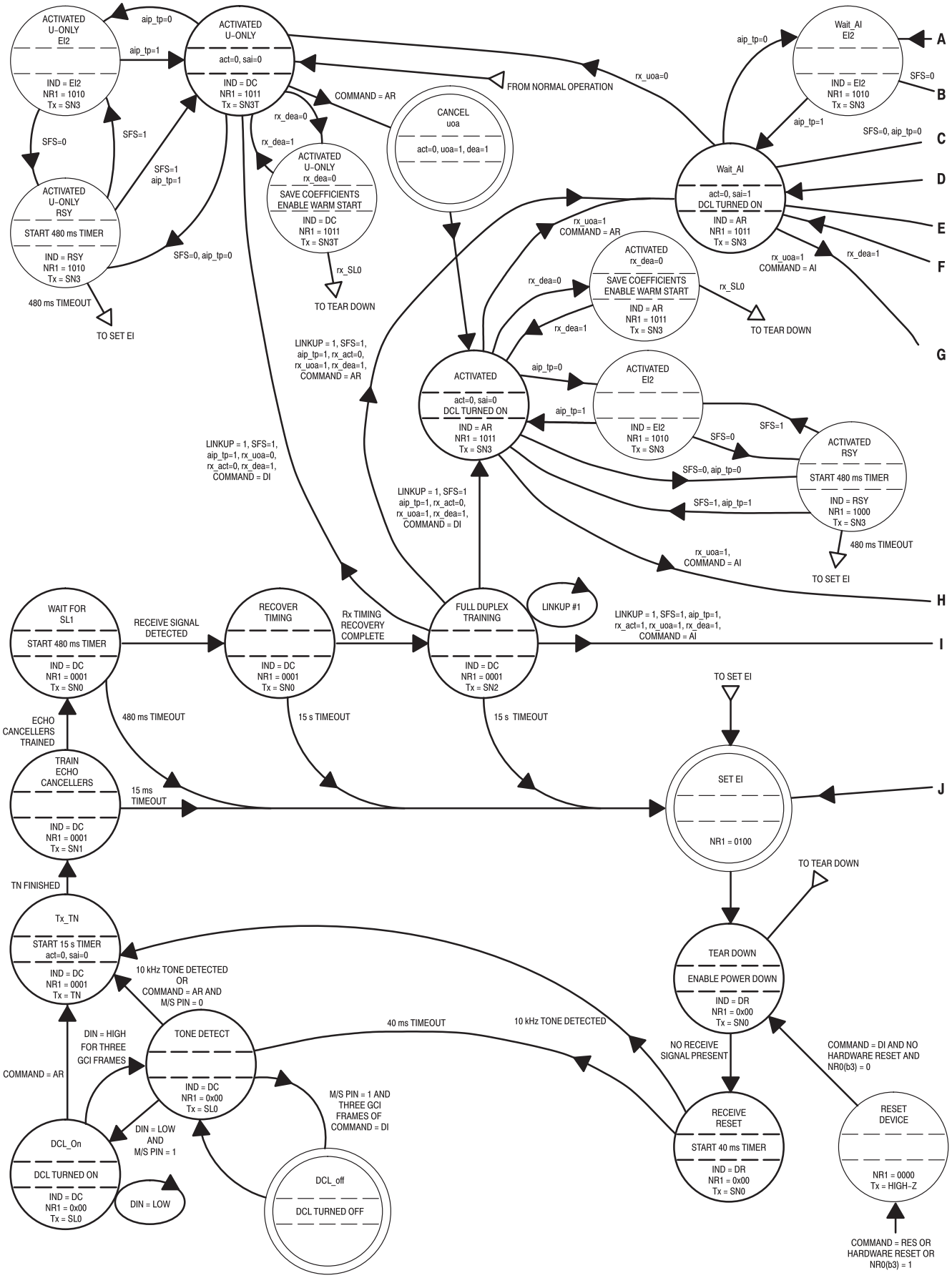
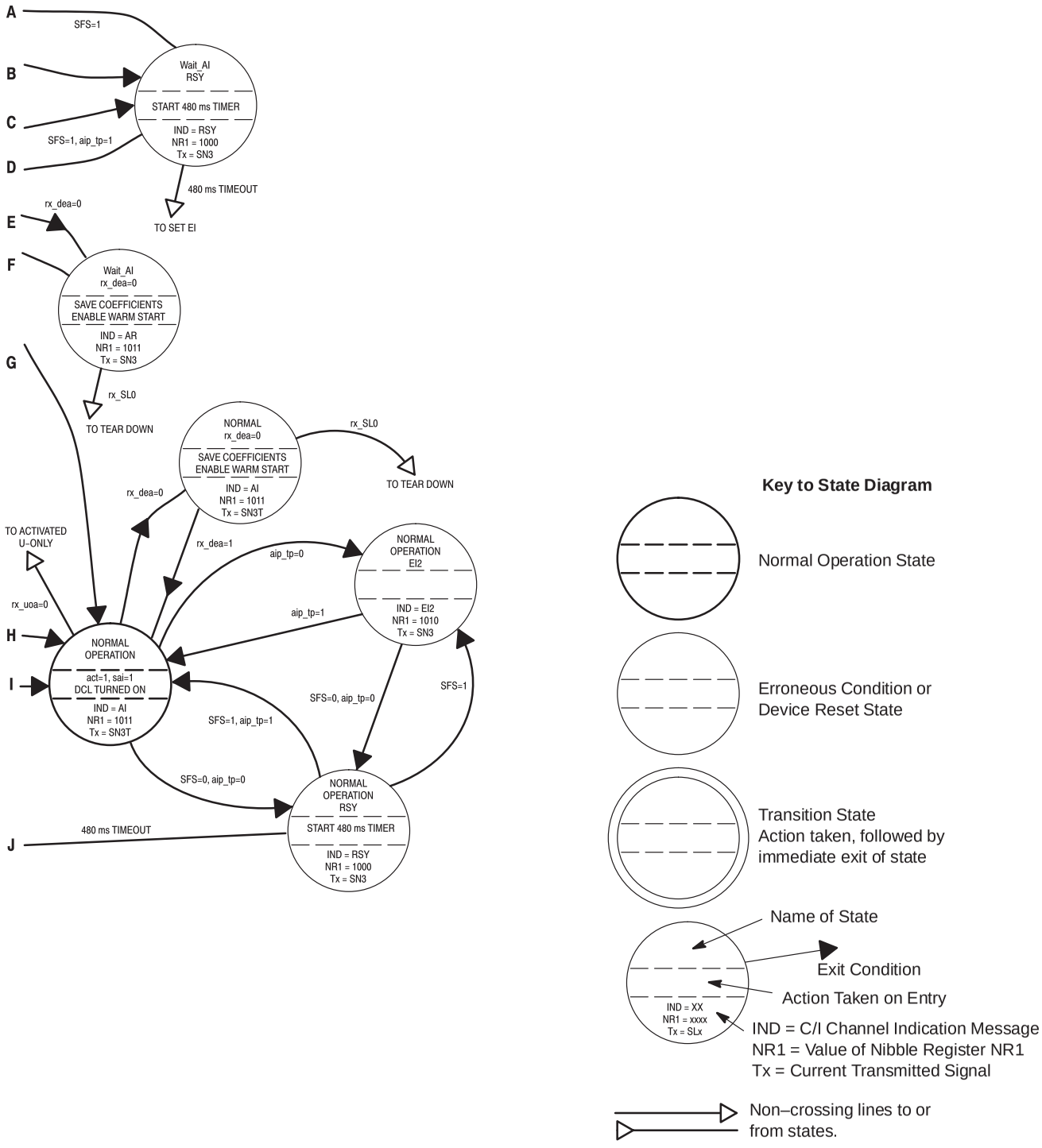


Figure 8–18. NT Mode GCI State Diagram (Sheet 1 of 2)



NOTES:
1. An “x” in the NR1 bit means that the bit remains unchanged from its value in a previous state.
2. The transmitted M4 channel bits remain unchanged between states unless a change is explicitly indicated.
3. SL3T is SL3 with transparent data transmission.
4. The state “Normal Operation” is the state in which the MC145572 operates when it is fully activated, transmitting 2B+D with transparency enabled.
5. Linkup = NR1(b3), SFS = NR1(b1), aip_tp = NR1(b0).
6. Warm start is only enabled when the MC145572 transitions from the four states that enable warm start directly to the “Tear Down” state. Any other transition disables warm start.

Figure 8–18. NT Mode GCI State Diagram (Sheet 2 of 2)

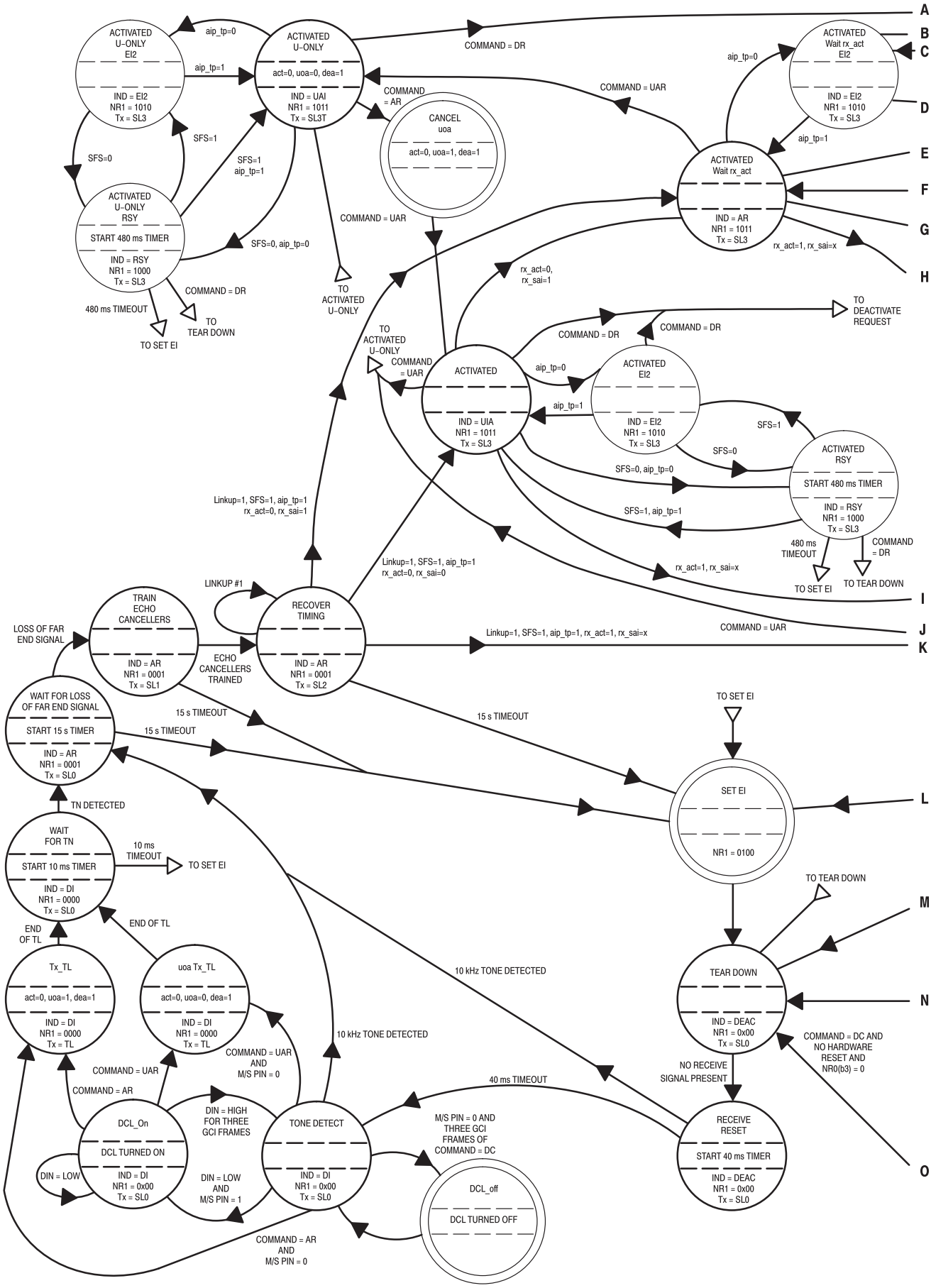
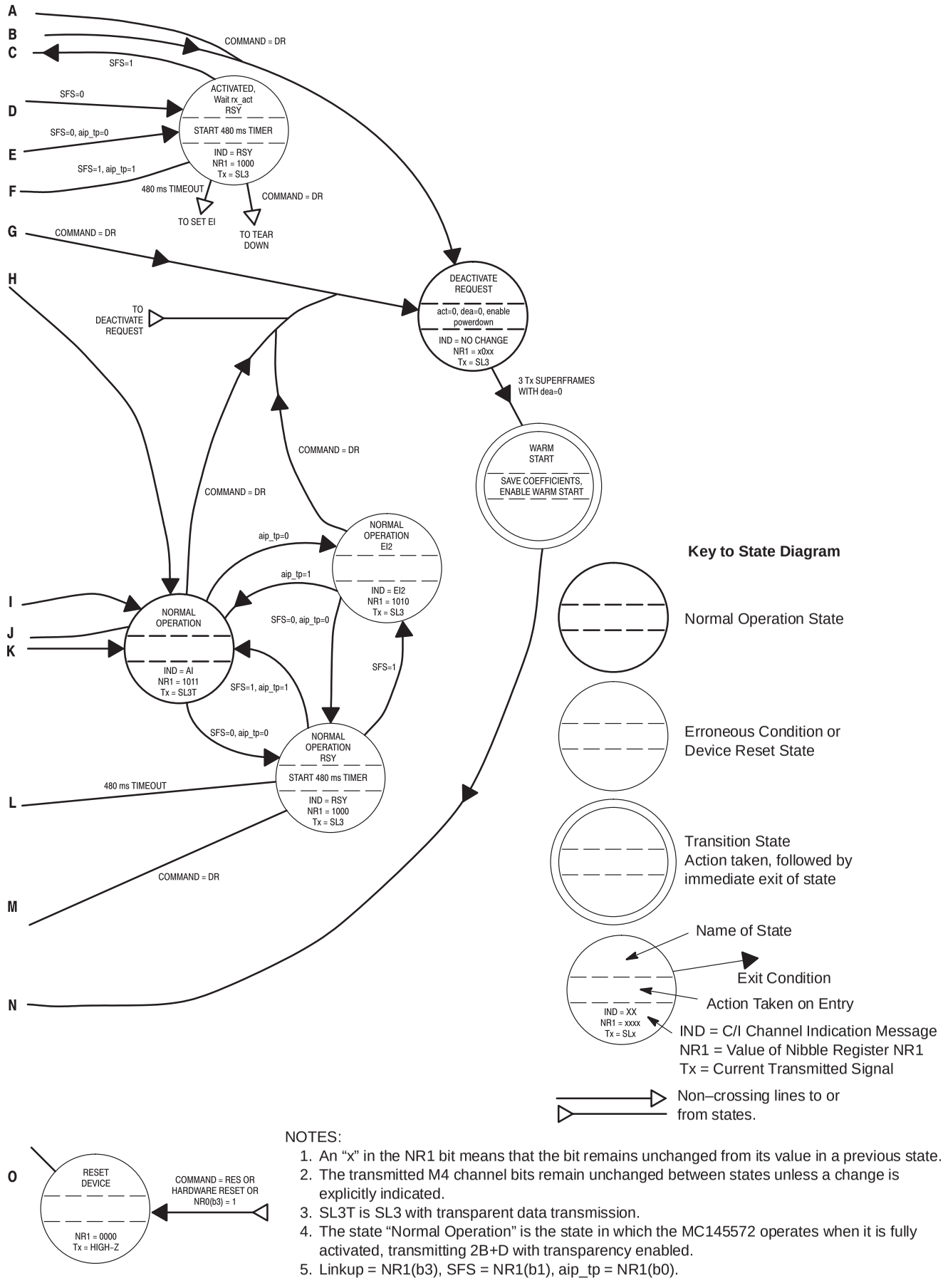


Figure 8–19. LT Mode GCI State Diagram (Sheet 1 of 2)



NOTES:

1. An “x” in the NR1 bit means that the bit remains unchanged from its value in a previous state.
2. The transmitted M4 channel bits remain unchanged between states unless a change is explicitly indicated.
3. SL3T is SL3 with transparent data transmission.
4. The state “Normal Operation” is the state in which the MC145572 operates when it is fully activated, transmitting 2B+D with transparency enabled.
5. Linkup = NR1(b3), SFS = NR1(b1), aip_tp = NR1(b0).

Figure 8–19. LT Mode GCI State Diagram (Sheet 2 of 2)

9

MCU MODE PROGRAMMING SUGGESTIONS

9.1 INTRODUCTION

This chapter is a guide for writing software for the MC145572. It provides several pseudo–code examples on how to initialize and activate the MC145572 U–interface transceiver. NT and LT initiated activation procedures are given, using both the automatic and non–automatic eoc modes. This chapter also contains sample initialization routines for IDL–2 timeslot assignment procedures, GCI electrical mode timeslot assignment, block error rate calculation, and non–ISDN D channel communications.

9.2 ACTIVATION AND INITIALIZATION

The MC145572 provides easy microcontroller read and write access to the Maintenance channel via the SCP or PCP interface. This permits the Maintenance channel to be easily updated and changes in ANSI T1.601–1992 defined default values to be implemented simply by modifying software. Note that there are many proprietary applications where the Maintenance channel can be used in any manner whatsoever. For a discussion of the Maintenance channel, see **Chapters 5 and 7**.

The MC145572 should be initialized before Activation Request, NR2(b2), is set to a 1, when Activation in Progress (NR1(b0)) is first detected set to a 1, or when deactivation has been confirmed. This ensures that the correct data appears on the maintenance channels when linkup is achieved and the U–interface is activated.

The Software Reset bit (NR0(b3)), need only be set to a 1, then reset to a 0, as part of the power–up initialization routines.

The MC145572 should be initialized so that when it activates, the correct data is present on all of the maintenance channels at the time activation occurs. The ANSI T1.601–1992 specification indicates the default and operational data that should appear on these channels. A microcontroller write to the specified register puts maintenance data onto the indicated U–interface maintenance channel. A microcontroller read of the specified register obtains maintenance data from the indicated U–interface maintenance channel. These channels are:

- **eoc Channel:** This channel is accessed via register R6. It is used to convey eoc messages from the LT to the NT. The NT conveys its acknowledgment of eoc messages back to the LT on this channel. Typically, this channel is used by the LT to send loopback and other maintenance messages to the NT. See ANSI T1.601–1992 for currently defined eoc messages and other eoc procedures.
- **M4 Maintenance Channel:** Data is put on this channel by writing to BR0. Data is read from this channel by reading BR1. This channel is used by the LT to signal its activation status to the NT. The LT also uses this channel to tell the NT when it is intending to deactivate the U–interface. The NT uses this channel to send its activation status to the LT. The NT also uses this channel to send its power supply status, its warm start capability, and if it is in a test mode, back to the LT. There are several reserved bits which the ANSI T1.601–1992 specification indicates should be set to 1s.
- **M5 and M6 Maintenance Channels:** Data is put onto these channels by writing to BR2. Data is read from these channels by reading BR3. Currently all bits in these channels are defined by ANSI T1.601–1992 as reserved and should be set to 1s.

Sample initialization routines are provided on how to initialize the MC145572 when operated in the LT or NT modes. Procedure NTINIT1 in **Section 9.2.1** initializes the MC145572 for automatic eoc operation when configured as an NT. The corresponding sample high level embedded operations

channel interrupt service routine, NTISR1, is also provided in **Section 9.2.1**. Procedure NTINIT2 in **Section 9.2.2** initializes the MC145572 for non–automatic eoc operation when in the NT mode. The corresponding sample high level embedded operations channel interrupt service routine, NTISR2, is also provided in **Section 9.2.2**. Procedure LTINIT1 in **Section 9.3** initializes the MC145572 when it is operated in LT mode.

The sample initialization and operation examples given here are to be used as a guide only. All data written to or read from registers is in hexadecimal. User eoc, M channel, and activation handlers are implementation specific. In this example, M4 channel is initialized to $77 in NT mode and $7F in LT mode. The $77 in NT mode indicates act bit not asserted, ps1 and ps2 status normal, NT1 not in test mode, warm start capability, and all ANSI T1.601–1988 reserved bits set to 1s. The $7F in LT mode indicates the act bit is not asserted, the dea bit is not asserted, and all ANSI T1.601–1988 reserved bits set to 1s. The bits in the M5 and M6 channels are all initialized to 1s and R6 is initialized to $1FF (Return to Normal) when in the LT mode. It is not necessary to initialize R6 in the NT mode since the specific eoc handler used will respond to the incoming eoc messages from the LT.

When the U–interface transceiver first activates after a cold or warm start, the `febe` and `nebe` counters, BR4 and BR5, should be cleared by the software. Provision must be made so these two registers are not cleared if there has been a temporary dropout of data transparency or loss of frame sync; i.e., only clear these counters upon initial activation. When a temporary loss of frame sync or signal occurs without the U–interface transceiver going to the full reset state, it is important that the `febe` and `nebe` count values accurately reflect CRC errors during this time. A reasonable time to clear the `febe` and `nebe` counters is when the M4 channel `act` bits are first exchanged after initial activation from warm or cold start. If the `febe` and `nebe` counters in the NT are cleared when linkup occurs, it is possible to get `febe` counts due to the LT transceiver not having completed its activation sequence.

9.2.1 NT Automatic eoc Mode Initialization and Activation

The MC145572 provides a mode for trinal checking and automatic invoking of NT1 eoc functions as defined in ANSI T1.601–1992. In this mode, the external microcontroller does not need to perform trinal checking, decoding, and implementation of eoc messages. The M4 trinal consecutive check mode is used in this example. Note that only the `act`, `dea`, and `uoa` M4 bits are verified three consecutive times. The following three code segments: NTACT1(), NTINIT1(), and NTISR1() configure the MC145572 in the above modes and are an example implementation of an NT initiated full activation in an NT1. The NT1 initiates activation of the U–interface only when requested to do so by the terminal equipment (TE) or upon cycling of NT1 power.

An initialization and activation procedure for an NT1 follows. A suggested interrupt service routine outline, NTISR1, is also given.

```
Procedure NTACT1();

/*
PURPOSE:
The activation procedure NTACT1 resets the U–interface transceiver, calls the initializa-
tion routine NTINIT1, sets activate request, and waits for interrupts.
*/
BEGIN
NR0(b3) <–      1;          /*  Assert software reset. Only required
                                at power–up initialization/
NR0(b3) <–      0;          /*  De–assert software reset. Only required at power–up
                                initialization/
CALL NTINIT1();
NR2(b3) <–      1;          /*  Set activation request bit.*/
Wait for interrupt;         /*  Wait for result of Activation */
Other code;
END;
```

Procedure NTINIT1()

```
/*
PURPOSE:
The initialization procedure NTINIT1 puts the NT configured U-interface transceiver into
automatic eoc mode and selects the M4 channel trinal consecutive check mode of operation.
It also sets default values for the M4, M5, and M6 channels. Activation interrupts are also
enabled. This routine should always be executed just prior to setting Activation Request
NR2(b3) = 1 or when the activation in progress interrupt occurs in response to the MC145572
detecting a wakeup tone.
*/
BEGIN
BR0      <-   77;  /*  M4 transmit: act = 0, power normal, normal mode (ntm = 1), warm start
                       capable, unused bits = 1 */
BR1      <-   7F;  /*  Set initial conditions on M4 channel receive. This (BR0 = 7F) will
                       force an M channel interrupt to occur when the M4 act bit from the LT
                       changes from a 0 to a 1, signifying Layer 2 communication readiness/
BR2      <-   F0;  /*  M5 and M6 channels set to ANSI T1.605-1992 reserved condition. febe
                       input = 1.*/
BR9      <-   1C;  /*  Select automatic eoc mode, M4 dual consecutive check, M5/M6 update on
                       every frame and transmitted febe is computed nebe. */
BR10(b0) <-   1;   /*  Select init group registers. */
OR7(b0)  <-   1;   /*  Enable trinal checking of M4 act, dea, and uoa bits. The remaining M4
                       bits are dual consecutive checked as defined in BR9(b4:b5) */
BR10(b0) <-   0;   /*  Return to normal byte register operation. */
NR4      <-   A;   /*  Enable IRQ3, activation/D channel interrupt and IRQ2 - M4 Channel
                       interrupt. */
END;
```

Procedure NTISR1()

```
/*
PURPOSE:
The interrupt service routine NTISR1 handles activation and checks for Linkup with Super
frame Sync or for an Error Indication. If linkup is achieved, the febe and nebe counters
are cleared and the M4 act bit is set to a 1 if a check of the S/T-interface indicates that
it is active. If the Error Indication status bit, NR1(b2), is set to 1, appropriate mea-
sures can be taken. Also, when act = 1 from the LT, NTISR1 will enable data transparency.
*/
BEGIN
       IF NR3(b3) = 1 THEN    /* Test for activation interrupt */
       BEGIN
              IF NR1 = A or B AND
              initial activation THEN       /* Test for successful initial activation */
              BEGIN
                     BR4 <- 00;             /* Clear febe counter */
                     BR5 <- 00;             /* Clear nebe counter */
                     IF S/T interface is
                     active THEN
                            BR0 <- F7;      /* Send M4 act status to LT */
              END
              ELSE IF NR1 = 4 THEN          /* Test for error indication */
              BEGIN
                     Take appropriate measures:
                     * disable interrupts
                     * report unsuccessful
                       activation attempt
              END
       END
       IF NR3(b1) = 1 /* Test for M4 channel interrupt */
       BEGIN
              IF BR1(b7) = 1 AND    /* test for act bit 0 to 1 transition and */
              last received BR1(b7) = 0 AND /* dea = 1 from LT */
              BR1(b6) = 1 THEN
                            NR2(b0) <- 1;  /* Set Customer Enable bit for NT1 data
                                           transparency */
              ELSE
                     handle other M4
                     status changes here
       END
       return();
END
```

9.2.2 NT Non-Automatic eoc Mode Initialization and Activation

The MC145572 can be operated with eoc frame trinal checking and eoc interrupts enabled so an external microcontroller may handle all eoc commands in software. Note that the MC145572 still performs eoc frame trinal checking, thus relieving the external microcontroller of this task. The M4 channel dual consecutive check mode is enabled. The examples in this section configure an NT U–interface transceiver in these modes and activate it.

The eoc message processor, given as an example here, covers a very limited implementation of an eoc command set.

The activation procedure, NTACT2, resets the U–interface transceiver, calls the initialization routine NTINIT2, sets activate request, and waits for interrupts.

An initialization and activation procedure for an NT1 follows with numbers in hexadecimal. A suggested interrupt service routine outline, NTISR2, is also given.

Procedure NTACT2();

```
/*
PURPOSE:
The activation procedure NTACT2 resets the U–interface transceiver, calls the initializa-
tion routine NTINIT2, sets activate request, and waits for interrupts.
*/
BEGIN
NR0(b3)  <–   1;   /*  Assert software reset. Only required
                       at power–up initialization/
NR0(b3)  <–   0;   /*  De–assert software reset. Only required at power–up initialization/
CALL NTINIT2();
If NR1 = 0 then NR2 (b3) <– 1;    /*  Set activation request bit */
Wait for interrupt;   /*                                  Wait for result of Activation */
Other code;
END;
```

Procedure NTINIT2()

```
/*
PURPOSE:
The initialization procedure NTINIT2 puts the NT configured U–interface transceiver into
eoc trinal–check mode and selects the M4 channel trinal consecutive check mode of opera-
tion. It also sets default values for the M4, M5, and M6 channels. Activation interrupts
are also enabled. This routine should always be executed just prior to setting Activation
Request NR2(b3) = 1 or when the activation in progress interrupt occurs in response to the
MC145572 detecting a wakeup tone.
*/
BEGIN
BR0      <–   77;  /*  M4 transmit: act = 0, power normal, normal mode (ntm = 1), warm start
                       capable, unused bits = 1 */
BR1      <–   7F;  /*  Set initial conditions on M4 channel receive. This (BR0 = 7F) will
                       force an M channel interrupt to occur when the M4 act bit from the LT
                       changes from a 0 to a 1, signifying Layer 2 communication readiness/
BR2      <–   F0;  /*  M5 and M6 channels set to ANSI T1.605–1992 reserved condition. febe
                       input = 1.*/
BR9      <–   9C;  /*  Select non–automatic eoc mode, M4 dual consecutive check, M5/M6 up-
                       date on every frame and transmitted febe is computed nebe. */
BR10(b0) <–   1;   /*  select init group registers */
OR7(b0)  <–   1;   /*  enable trinal checking of M4 act, dea, and uoa bits. The remaining M4
                       bits are dual consecutive checked as defined in BR9(b4:b5) */
BR10(b0) <–   0;   /*  return to normal byte register operation */
NR4      <–   E;   /*  Enable activation/D channel, M4 channel and eoc interrupts */
END;
```

Procedure NTISR2()

```
/*
PURPOSE:
The interrupt service routine NTISR2 checks for Linkup with Super frame Sync or for an
Error Indication. If linkup is achieved, the febe and nebe counters are cleared and the M4
act bit is set to a 1 if a check of the S/T-interface indicates that it is active. If the
Error Indication status bit, NR1(b2), is set to 1, appropriate measures can be taken. A
sample outline of the ANSI complaint eoc message handler is also included. Note that if the
D channel SCP access (BR10(b1) = 1) and IRQ3 (NR4(b3) = 1) are enabled then NR1 must be
checked for the hex code F before any other IRQ3 interrupt is serviced.
*/
BEGIN
       IF NR3(b3) = 1 THEN   /* Test for activation interrupt */
       BEGIN
              IF NR1 = F THEN       /* Check for D channel interrupt.*/
              BEGIN
                     * read/write D channel
                       data from/to OR12
                     * clear D channel interrupt
              END
              ELSE IF NR1 = A or B AND
              initial activation THEN      /* Test for successful initial activation */
              BEGIN
                     BR4 <- 00;     /* Clear febe counter */
                     BR5 <- 00;     /* Clear nebe counter */
                     IF S/T interface is
                     active THEN
                            BR0 <- F7;     /* Send M4 act status to LT */
              END
              ELSE IF NR1 = 4 THEN  /* Test for error indication */
              BEGIN
                     Take appropriate measures:
                     * disable interrupts
                     * report unsuccessful
                       activation attempt
              END
       END
       IF NR3(b1) = 1 /* Test for M4 channel interrupt */
       BEGIN
              IF BR1(b7) = 1 AND    /* test for act bit 0 to 1 transition and */
              last received BR1(b7) = 0 AND /* dea = 1 from LT */
              BR1(b6) = 1 THEN
                            NR2(b0) <- 1;  /* Set Customer Enable bit for NT1 data
                                      transparency */
              ELSE
                     handle other M4
                     status changes here
       END

       IF NR3(b2) = 1 THEN   /* Test for eoc interrupt */
       BEGIN
              IF R6(B11:B9) = 1 OR 7 THEN   /* Test for eoc message, address = NT1 or
                                      broadcast, respectively. */
              BEGIN
                     IF (R6(B8)=1 AND R6(B7:B0) = a defined eoc message THEN
                     BEGIN
                            R6 <- R6;      /* Echo eoc message to LT (Time critical!) */
                            * take appropriate
                              actions depending on
                              message
                     END
                     ELSE
                            R6 <- 1AA;     /* Send Unable to Comply back to LT. */
              END
              ELSE
                     R6 <- 100;     /* eoc address not equal to 000 or 111. Send
                                      Hold state back to LT */
       END
       return();
END
```

9.2.3 LT Mode Initialization and Activation

LT initialization is very similar to NT initialization except that the automatic eoc mode is not available. Trinal checking of received eoc commands is enabled. When the U–interface transceiver is operated as an LT, the software initiates eoc messages by writing into R6. Correct operation of the eoc message at the NT1, as defined in ANSI T1.601–1992, is indicated by the LT receiving the echoed eoc message in R6. This is shown at a very high level in LTISR1.

An initialization and activation procedure for LT mode follows with numbers in hexadecimal:

Procedure LTACT1();

```
/*
PURPOSE:
The activation procedure LTACT1 resets the U–interface transceiver, calls the initializa-
tion routine LTINIT1, sets activate request, and waits for interrupts.
*/
BEGIN
NR0(b3)  <–   1;   /*  Assert software reset. Only required
                       at power–up initialization.*/
NR0(b3)  <–   0;   /*  De–assert software reset. Only required at power–up initialization.*/
CALL LTINIT1();
If NR1 = 0 then NR2 (b3) <– 1;    /*  Set activation request bit */
Wait for interrupt;   /*                                    Wait for result of Activation */
Other code;
END;
```

Procedure LTINIT1()

```
/*
PURPOSE:
The initialization procedure LTINIT1 puts the LT configured U–interface transceiver into
eoc trinal–check mode and selects the M4 channel trinal consecutive check mode of opera-
tion. It also sets default values for the M4, M5, and M6 channels. Activation interrupts
are also enabled. This routine should always be executed just prior to setting Activation
Request NR2(b3) = 1 or when the activation in progress interrupt occurs in response to the
MC145572 detecting a wakeup tone.
*/
BEGIN
BR0      =    7F;  /*  act = 0, dea = 1, other bits to ANSI T1.601–1992 reserved status. */
BR1      =    7F;  /*  Force an M4 channel interrupt to occur when received act changes to a
                       1 from a zero. */
BR2      =    F0;  /*  M5 and M6 channels to ANSI T1.601–1992 reserved condition. febe Input
                       = one. */
BR9      =    8C;  /*  Select eoc trinal check, M4 Verified act mode, M5/M6 update on every
                       frame, and transmited febe is Computed nebe. */
BR10(b0) =    1;   /*  Select Init Group of registers */
OR7(b0)  =    1;   /*  Enable trinal checking of M4 act and sai bits. */
BR10(b0) =    0;   /*  Deselect Init Group. */
R6       =    1FF; /*  Eoc defaults to Return to Normal message with NT1 addressed and d/m
                       bit set to one. */
NR4      =    E;   /*  Enable eoc, M4 and activation interrupts. */
return ( ) ;
END;
```

Procedure LTISR1()

```
/*
PURPOSE:
The interrupt service routine LTISR1 checks for Linkup with Super frame Sync or for an
Error Indication. If linkup is achieved, the febe and nebe counters are cleared and the M4
act bit is set to a 1. A check is made for correct reception of the eoc message by the NT1.
Correct reception is indicated when the received eoc message in R6 is the same as the eoc
message originally written to R6. This is per ANSI T1.601–1992. Note that this is one of
many possible implementations. Note that the M4 channel act bit towards the NT is set to a
1 only if the LT is receiving M4 act bit equal to 1 from the NT. This is per ANSI
T1.601–1992 section 6.4.6.4. If the Error Indication status bit, NR1(b2), is set to 1,
appropriate measures can be taken.
It is not necessary to reset the MC145572 after an activation failure occurs. A reset only
needs to be applied after initial power up.
*/
BEGIN
       IF NR3(b3) = 1 THEN   /* Test for activation interrupt */
       BEGIN
              IF NR1 = B THEN       /* Test for successful activation */
                     Notify central office
                     processor;
              ELSE IF NR1 = 4 THEN  /* Test for failed activation (Error
              BEGIN          /* Indication) */
                     NR4 <– 0;      /* Disable interrupts. */
                     * report failed
                       activation attempt
              END
       END
       IF NR3(b1) = 1 /* Test for M4 Channel Interrupt */
       BEGIN
              IF BR1(b7) = 1 AND    /* test for act bit 0 to 1 transition */
              last received BR1(b7) = 0 THEN
              BEGIN
                     BR4 <– 00;     /* Clear febe Counter */
                     BR5 <– 00;     /* Clear nebe Counter */
                     BR0(b7) <– 1;  /* Send M4 act = 1 status to NT */
                     NR2(b0) <– 1;  /* Enable data transparency at LT */
              END
              ELSE          /* handle other M4 status changes */
                     handle other M4 channel
                     status changes here
       END
       IF NR3(b2) = 1 THEN   /* Test for eoc channel interrupt */
       BEGIN
              If the value read from R6
              is the same as the last value
              written to R6 then the NT1
              executed the eoc message
              correctly. Take appropriate
              measures

              If the value read from R6 is
              not the same as the last value
              written to R6 then the NT1 did
              not execute the eoc message
              correctly. Take appropriate
              measures
       END
       return();
END
```

9.3 TIMESLOT ASSIGNER PROGRAMMING EXAMPLE

In modern Central Office Switches (COS) or Private Branch Exchanges (PBXs), a Time Division Multiplex (TDM) bus may carry data from several different U–interfaces. The MC145572 is designed with a flexible Timeslot Assigner (TSAC), allowing it to transmit and receive 2B+D data in any timeslot on a TDM bus.

With the MC145572s TSAC, B, and D channel timeslots can be assigned an any 2–bit boundary. Figure 9–1 shows an 8 kHz TDM frame divided into 2–bit timeslots labeled TS0 through TSn–1. ‘n’ is the maximum number of 2–bit timeslots. Programming the MC145572s TSAC is accomplished by writing the 2–bit timeslot number that corresponds to the first two bits of a B or D channel timeslot to one of the TSAC registers (OR0 through OR5).

A typical arrangement of timeslots for four U–interface devices is shown in Figure 9–2. The procedure `TSACinit()` shows how to configure the MC145572 as if it occupies the timeslots highlighted in Figure 9–2.

Procedure TSACinit();

```
/*
PURPOSE:
   select IDL format and timeslots for B1, B2, and D channels
INITIAL CONDITIONS:
   MC145572 configured for IDL–2 slave mode
   DCL clock rate = 4.096 MHz
TIMESLOT assignment
B1 channel transmit –> TS8 through TS11
B1 channel receive  –> TS8 through TS11
B2 channel transmit –> TS12 through TS15
B2 channel receive  –> TS12 through TS15
D channel transmit  –> TS33
D channel receive   –> TS33
The transmit and receive starting timeslot for each channel is programmed into registers
OR0 through OR5.
*/
Begin
NR0(b3)  <–   1;   /*  Assert software reset. Only required
                       at power–up initialization.*/
NR0(b3)  <–   0;   /*  De–assert software reset. Only required at power–up initialization.*/
BR10(b0) <–   1;   /*  Select Init Group Overlay registers.*/
OR0      <–   08;  /*  B1 transmit starts in TS8 */
OR1      <–   0C;  /*  B2 transmit starts in TS12 */
OR2      <–   11;  /*  D transmit is in TS33 */
OR3      <–   08;  /*  B1 receive starts in TS8 */
OR4      <–   0C;  /*  B2 receive starts in TS12 */
OR4      <–   11;  /*  D receive is in TS33 */
OR6      <–   E0;  /*  Enable B1, B2, and D timeslots.*/
OR10(b0) <–   0;   /*  Timeslot initialization over. Deselect overlay registers and return
                       to normal byte register operation */
End;
```

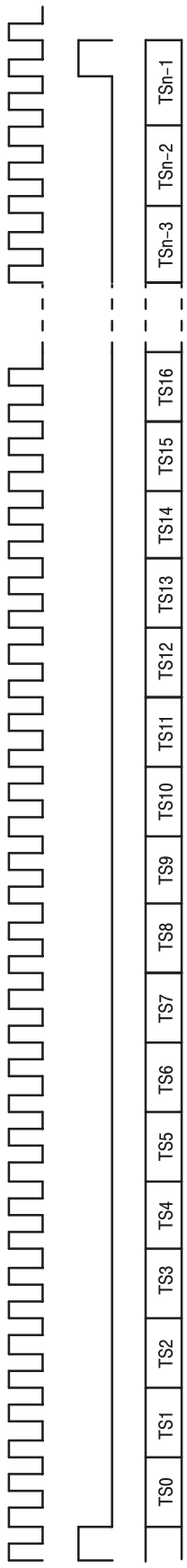


Figure 9–1.

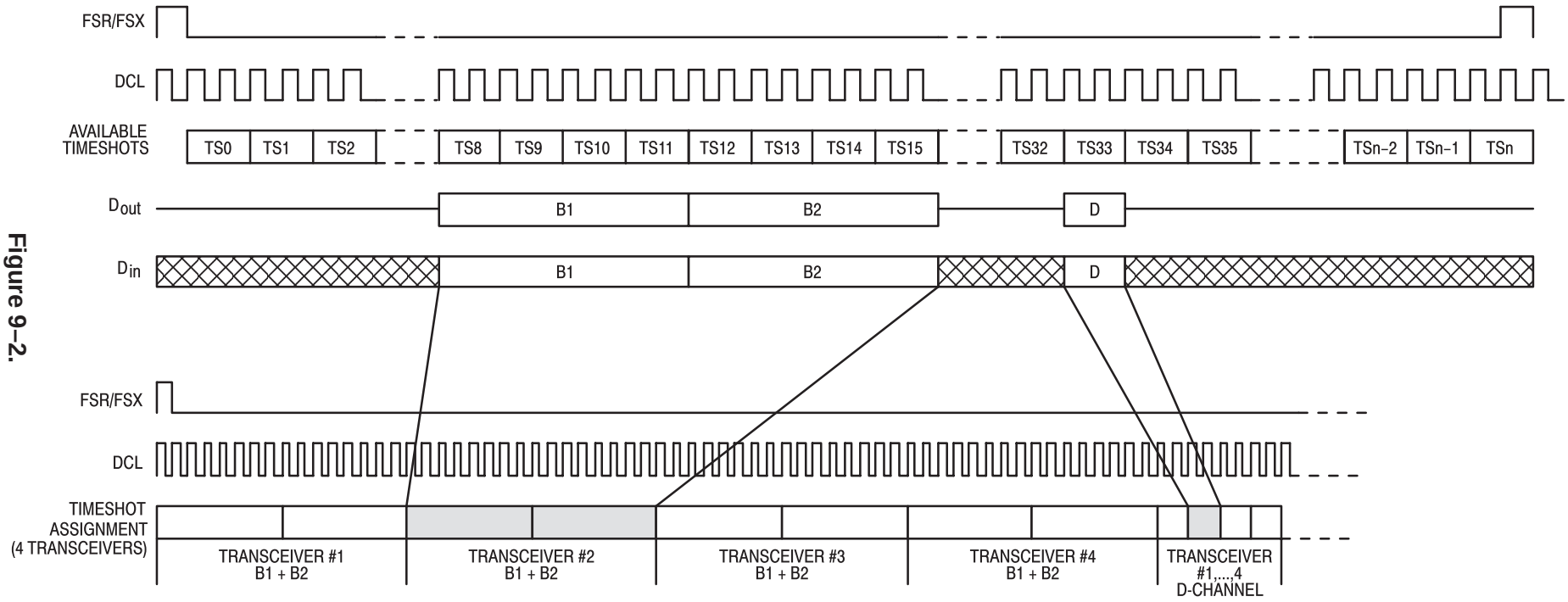


Figure 9–2.

9.4 GCI 2B+D MODE PROGRAMMING EXAMPLE

This example shows how to program the MC145572 when the GCI 2B+D format is selected instead of IDL 8– and 10–bit modes. See **Section 5.4.3** for a description of the GCI 2B+D mode.

```
Procedure GCI2B+Dinit();

/*
PURPOSE:
   Program GCI timeslot in IDL–2 GCI 2B+D data format
INITIAL CONDITIONS:
   MC145572 configured for IDL–2 slave mode
   DCL clock rate = 4.096 MHz
Timeslot assignment:
When the DCL clock frequency = 4.096MHz there are 8 possible 32–bit GCI timeslots. In this
example we will program the MC145572 to transmit and receive in the 4th GCI timeslot.
*/
BEGIN
NR0(b3)  <–   1;   /*  Assert software reset. Only required at power–up initialization.*/
NR0(b3)  <–   0;   /*  De–assert software reset. Only required at power–up initialization.*/
BR10(b0) <–   1;   /*  Select Init Group Overlay registers.*/
OR5      <–   03;  /*  Select the 4th GCI timeslot */
OR6(3)   <–   1;   /*  Enable 4th GCI timeslot */
OR10(b0) <–   0;   /*  Timeslot initialization over. Deselect overlay registers and return
                       to normal byte register operation */
END;
```

9.5 BLOCK ERROR RATIO CALCULATION USING febe/nebe COUNTERS

This example shows how to use the MC145572 febe and nebe counters to calculate a BLock Error Ratio (BLER). The BLER is a useful measure of the channel quality as well as a measure of the far–end and near–end receiver's performance. Using a timed interrupt, the procedures BLER_init and BLER_ISR determine the BLER by calculating the number of far–end and near–end block errors that occurred in the last 100 superframes. By subtracting the value of the febe/nebe counters read during an interrupt from the value read in the previous interrupt, the error count over a specific time interval can easily be determined.

The MC145572 has febe and nebe status bits, as well as febe and nebe counters. BR3 contains the status bits, BR4 is the febe counter and BR5 is the nebe counter. When a febe or nebe is detected, the status bit is set and the counters are incremented. **Section 7.5** describes the operation of the febe/nebe bits in detail. The MC145572 adds a febe/nebe counter rollover feature which was not available in the MC145472. When this feature is enabled, the febe/nebe counters will rollover from $FF to 00 instead of saturating at $FF. The interrupt period of this example has been set to 1.2 seconds to guarantee that the febe/nebe counters do not roll over more than once between interrupts.

Since the superframe period is 12 ms, 100 superframes will be transmitted or received in 1.2 seconds. The 1.2–second interrupt can easily be implemented using the timer function on any Motorola MC68HC05 series microcontroller. For greater accuracy, the BLER generated at each interrupt can be summed over longer periods of time.

By reading BR4 and BR5 once per second it is easy to modify the above procedure to calculate error seconds and error free seconds.

Procedure BLER_init

```
/*
PURPOSE: BLER_init initializes the febe/nebe counters, enables febe/nebe rollover, and en-
ables the 1.2 second interrupt. Initialization of the febe/nebe registers should be done
upon activation as shown in the NT and TE activation examples previously mentioned in this
section.
*/
BEGIN
       BR4 <- 00;         /* Clear febe counter.*/
       BR5 <- 00;         /* Clear nebe counter */
       BR10(b0) <- 1;     /* Enable init group registers */
       OR7(b1) <- 1;      /* Enable febe/nebe rollover */
       BR10(b0) <- 0;     /* Disable init group registers */
       * program timer for 1.2 sec interrupt
       * enable timer interrupt
END
```

Procedure BLER_ISR

```
/*
PURPOSE: BLER_ISR handles the 1.2 second timer interrupt. It calculates the current far end
and near end block error rates and stores them in the memory locations: FE_BLER and
NE_BLER. The febe/nebe values from the last interrupt are stored in the memory locations:
last_febe and last_nebe. These memory locations should be initialized prior to enabling the
interrupt. If the result of subtracting the last febe/nebe from the current febe/nebe is
negative then the result is adjusted module 256.
OUTPUT:
FE_BLER        : far end block error rate in errors/100 blocks
NE_BLER        : near end block error rate in errors/100 blocks
last_febe      : BR4 value recorded from previous interrupt
last_nebe      : BR5 value recorded from previous interrupt
*/
BEGIN
       IF BLER_timer_int THEN
       BEGIN
              febe <- BR4;   /* store current febe */
              FE_BLER <- febe - last_febe   /* calculate far end BLER of last 1.2 sec */
              IF FE_BLER <= 0 THEN  /* test for febe counter rollover */
                     FE_BLER <- 256 - FE_BLER      /* adjust far end BLER for counter
                                                      rollover */
              last_febe <- BR4      /* update last_febe */
              nebe <- BR5;   /* store current nebe */
              NE_BLER <- nebe - last_nebe   /* calculate near end BLER of last 1.2 sec */
              IF NE_BLER <= 0 THEN  /* test for nebe counter rollover */
                     NE_BLER <- 256 - NE_BLER      /* adjust near end BLER for counter
                                                      rollover */
              last_nebe <- BR5      /* update last_nebe */
       END
END
```

9.6 D CHANNEL COMMUNICATION VIA THE SERIAL OR PARALLEL CONTROL PORT

In non–ISDN applications, such as pair–gain multiplexing, it is often necessary to communicate low–speed status information. The MC145572 provides a simple means to transmit this type of status information over the D channel of the U–interface.

In pair–gain applications, the off–hook status is transmitted from the Remote Terminal (RT) to the Central Office Terminal (COT) and the ring detect status is transmitted from the COT to the RT (see Figure 9–3).

In MCU mode, the MC145572 provides a means to transmit and receive D channel information through the SCP or PCP. This allows an MCU to access the D channel without using the D channel port or the IDL interface. Once activation is achieved, transparent data is enabled and BR10(b1) is set, D channel data is accessible through Overlay register OR12. If $\overline{IRQ3}$ is enabled and BR10(b1) = 1, a special code is loaded into NR1 (NR1 = 1111) to indicate that a new byte of D channel data was received. This interrupt occurs every 500 μs. When an activation interrupt (also $\overline{IRQ3}$) occurs at the same time as a D channel interrupt, it is latched and generates an interrupt to the MCU after D Channel register OR12 has been read. This must be taken into account when writing the interrupt service routine.

The following two procedures are a basic example of how to communicate over the D channel using the PCP/SCP registers. DCH_init is used to enable $\overline{IRQ3}$ and initiate activation. The interrupt service routine, DCH_ISR, then enables customer data when activation is achieved and handles the D channel communications through Overlay register OR12.

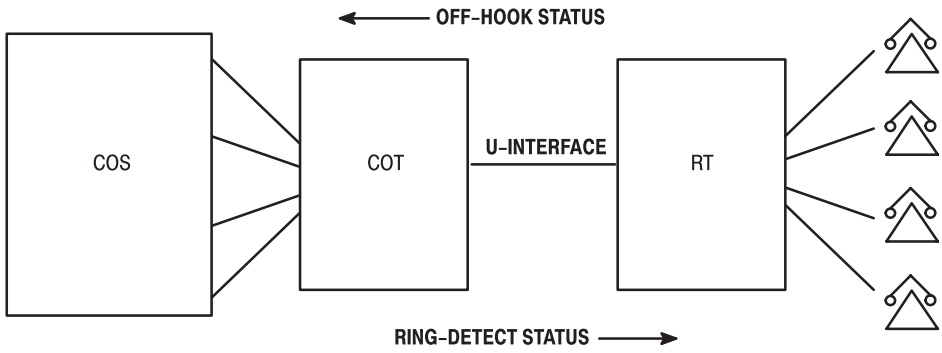


Figure 9–3. Status Information Flow in a 4:1 Pair–Gain Application

procedure DCH_init

```
/* PURPOSE: DCH_init initializes the D channel SCP/PCP communications and also activates
the MC145572.
BEGIN
NR0(b3)  <-   1;   /*  Assert software reset. Only required
                       at power-up initialization.*/
NR0(b3)  <-   0;   /*  De-assert software reset. Only required at power-up initialization.*/
BR10(b1) <-   1;   /*  Enable SCP/PCP D channel read/write access through OR12 */
NR4      <-   8;   /*  Enable IRQ3, activation/D channel interrupt */
NR2(b3)  <-   1;   /*  Set activation request bit.*/
Wait for interrupt;   /*                                  Wait for result of Activation */
Other code;
END
```

procedure DCH_ISR

```
BEGIN
       IF NR3(b3) = 1 THEN   /* Test for activation interrupt */
       BEGIN
              IF NR1 = F THEN       /* Check for D channel interrupt.*/
              BEGIN
                     * get OFF HOOK (RT) or RING DETECT (COT)
                       status from hardware and write
                       to OR12
                     * read OR12 and initiate
                       OFF HOOK to central office (from COT)
                       or RING DETECT to end phone (from RT)
                       if necessary
              END
              ELSE IF NR1 = A or B AND initial activation THEN
                                   /* Test for successful initial activation */
                     NR2(b0) <- 1;  /* set customer enable bit */
              ELSE IF NR1 = 4 THEN  /* Test for error indication */
              BEGIN
                     Take appropriate measures:
                     * disable interrupts
                     * report unsuccessful
                       activation attempt
              END
       END
END
```

10 ELECTRICAL SPECIFICATIONS

10.1 ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to 7.0	V
Voltage, Any Pin to V_{SS}	V_{in}	– 0.3 to V_{DD} + 0.3	V
DC Current, Any Pin (see Note)	I_{in}	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

NOTE: Except for V_{DD}, V_{SS}, TxP, and TxN.

10.2 RECOMMENDED OPERATING CONDITIONS

(Voltages Referenced to V_{SS}, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Current Sourced from CAP3V pin @ 2.7 V		—	—	5	mA

10.3 POWER CONSUMPTION

(Voltages Referenced to V_{SS}, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Power Consumption, Activated		—	225	275	mW
Power Consumption, Absolute Power Down		—	—	10	mW
Power Consumption, Deactivated		—	135	—	mW

10.4 PERFORMANCE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C)

Parameter	Min	Typ	Max	Unit
Cold Start Time, LT Mode	—	9	—	s
Cold Start Time, NT Mode	—	4	—	s
Warm Start Time, LT and NT Modes	—	75	—	ms
Transmit Linearity	45	—	—	dB
Bit Error Rate, 16,500 ft of 26 AWG, 1500 ft of 24 AWG, +1 dB NEXT Margin, ANSI T1.601–1992 (see Note)	—	—	10^{-7}	
Differential Receiver Sensitivity	—	15	20	mV

NOTE: Bit error rate performance depends significantly on the characteristics of the line interface circuit used to couple the MC145572 to the transmission line. This parameter is provided for informational purposes only.

10.5 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 V + 5%, T_A = – 40 to + 85°C)

Parameter	Test Conditions	Symbol	Min	Max	Unit
High–Level Input Voltage, Except FREQREF and $\overline{RESET}$		V_{IH}	2.0	—	V
Low–Level Input Voltage, Except FREQREF and $\overline{RESET}$		V_{IL}	– 0.3	0.8	V
High–Level Input Voltage, FREQREF and $\overline{RESET}$		V_{IH}	3.75	—	V
Low–Level Input Voltage, FREQREF and $\overline{RESET}$		V_{IL}	—	1.25	V
High–Level Output Voltage (I_{OH} = – 400 μA)		V_{OH}	2.4	—	V
Low–Level Output Voltage (I_{OL} = 5 mA)		V_{OL}		0.5	V
High–Level Input Current		I_{IH}	– 1	1	μA
Low–Level Input Current		I_{IL}	– 1	1	μA
High–Level Output Current	$V_{OH} = V_{DD} – 0.5$ V	I_{OH}	– 4	—	mA
Low–Level Output Current	V_{OL} = 0.4 V	I_{OL}	—	2.5	mA
$\overline{IRQ}$ Output Current	V_{OL} = 0.4 V	I_{IRQ}	—	2	mA
$\overline{IRQ}$ High Impedance		$R_{IRQ\ off}$	100	—	kΩ
Input Capacitance, Digital Pins		C_{in}	—	10	pF
$XTAL_{in}$, $XTAL_{out}$ Input Capacitance	FREQREF Connected to V_{SS} or V_{DD}		—	100	pF
$XTAL_{in}$ High–Level Input			3.5	—	V
$XTAL_{in}$ Low–Level Input			—	1.5	V
$XTAL_{out}$ Output Current	V_{OH},V_{OL} = 2.5 V		– 6.5	6.5	mA

NOTES:
1. All digital outputs except $XTAL_{out}$ are three–stateable regardless of their normal operating condition.
2. All digital outputs are specified at a load capacitance of 80 pF.

10.6 2B1Q INTERFACE ELECTRICAL CHARACTERISTICS

10.6.1 Pins TxP and TxN (V_{DD} = 5 V + 5%, T_A = – 40 to + 85°C, R_L = 60 Ω from TxP to TxN)

Parameter	Min	Typ	Max	Unit
Output Resistance — Full Power Mode	—	—	0.05	Ω
Output Resistance — Power Down Mode	—	10	30	Ω
Output Resistance — Absolute Power Down Mode	—	10	30	Ω
Output Peak Voltage From TxP to TxN	—	± 4.0	—	V_{pk} –V_{pk}
Output Load Capacitance	—	—	47	nF
Power Supply Rejection	—	60	—	dB
Peak Current	—	75	—	mA

10.6.2 Pins RxP and RxN (V_{DD} = 5 V + 5%, T_A = – 40 to + 85°C)

Parameter	Min	Max	Unit
Input Resistance — Full Power Mode	1	—	MΩ
Input Resistance — Power Down Mode	1	—	MΩ
Input Resistance — Absolute Power Down Mode	1	—	MΩ
Input Capacitance	—	10	pF
Input Voltage Range for RxP or RxN	$((V_{DD} – V_{SS})/2) – 0.5$	$((V_{DD} – V_{SS})/2) + 0.5$	V

10.7 IDL2 TIMING

10.7.1 IDL2 Master Short Frame Sync Timing, 8- and 10-Bit and TSAC Formats

Ref. No.	Parameter		Min	Typ	Max	Unit	Note
1	FSR or FSX Period		125	125	—	µs	1
2	Delay From the Rising Edge of DCL to the Rising Edge of FSX or FSR		—	—	30	ns	
3	Delay From the Rising Edge of DCL to the Falling Edge of FSX or FSR		—	—	30	ns	
4	DCL Clock Period		391	—	1953	ns	2
5	DCL Pulse Width High, Nominal	512 kHz	878	—	1074	ns	3
		2.048 MHz	210	—	265		
		2.56 MHz	170	—	215		
	DCL Clock 249 Pulse Width High	2.048 MHz	160	—	315		
		2.56 MHz	120	—	265		
	DCL Clock 59 Pulse Width High	512 kHz	825	—	1120		
6	DCL Pulse Width Low		45	—	55	% of DCL Period	4
7	Delay From Rising Edge of DCL to Low–Z and Valid Data on D_{out}		—	—	30	ns	
8	Delay From Rising Edge of DCL to Data Valid on D_{out}		5	—	30	ns	
9	Delay From Rising Edge of DCL to High–Z on D_{out}		—	—	30	ns	
10	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)		25	—	—	ns	
11	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)		25	—	—	ns	
12	Delay From Rising Edge of DCL to $\overline{TSEN}$ Low		—	—	30	ns	5
13	Delay From Falling Edge of DCL to $\overline{TSEN}$ High		—	—	30	ns	

NOTES:

1. FSR or FSX occurs on average every 125 µs.
2. The DCL frequency may be 512 kHz, 2.048 MHz, or 2.56 MHz.
3. The duty cycle of DCL is between 45% and 55% when operated in Master Timing mode. This duty cycle is guaranteed for all DCL clocks, except the clock that is used for making timing adjustments, in order to maintain synchronization with the received signal when operating in NT mode. In NT Master mode, the MC145572 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive IDL frames, once per U–interface basic frame. The total adjustment is 96 ns distributed over the two IDL frames. When DCL is configured for 2.048 MHz or 2.56 MHz, the adjustment occurs during clock pulse number 249 after FSX/FSR. The count starts at clock pulse 0 for the DCL clock immediately following FSX/FSR. When DCL is configured for 512 kHz, the adjustment occurs during DCL pulse number 59. It is important to remember this when using the timeslot assigner, since it is possible to program it to transfer 2B or D data during the clock period where the timing adjustment is being made and this may effect setup and hold times for other components in a system.
4. The pulse width during the low phase of the clock varies between 45% and 55% of the nominal frequency. Timing adjustments are not made during the low phase of DCL.
5. In IDL 8– and 10–bit formats, $\overline{TSEN}$ can be valid during the B1, B2, and D channel timeslots.

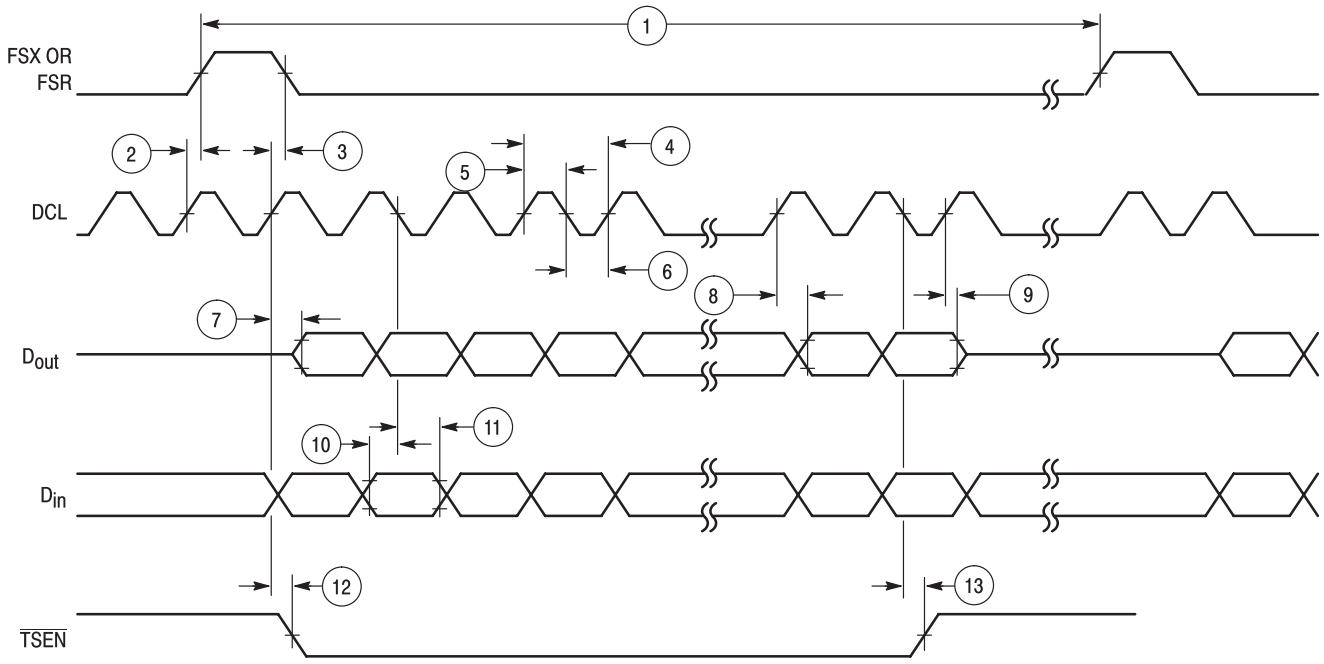


Figure 10–1. IDL Short Frame Sync Master Timing, 8– and 10–Bit Formats and TSAC Formats

10.7.2 IDL2 Slave Short Frame Sync Timing, 8- and 10-Bit Formats

Ref. No.	Parameter	Min	Max	Unit	Note
14	FSR or FSX Period	125	—	µs	1
15	FSR or FSX High Before the Falling Edge of DCL (FSR or FSX Setup Time)	25	—	ns	
16	FSR or FSX High After the Falling Edge of DCL (FSR or FSX Hold Time)	25	—	ns	
17	Delay From Rising Edge of DCL to Low–Z and Valid Data on D_{out}	—	30	ns	
18	Delay From Rising Edge of DCL to Data Valid on D_{out}	—	30	ns	
19	Delay From Rising Edge of DCL to High–Z on D_{out}	5	30	ns	
20	Delay From Rising Edge of DCL to $\overline{TSEN}$ Low	—	30	ns	2
21	Delay From Rising Edge of DCL to $\overline{TSEN}$ High	—	30	ns	
22	DCL Clock Period	244	1953	ns	3
23	DCL Pulse Width High	45	55	% of DCL Period	
24	DCL Pulse Width Low	45	55	% of DCL Period	
25	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)	25	—	ns	
26	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)	25	—	ns	

NOTES:
1. FSR or FSX occurs on average every 125 µs. FSX and FSR/FSC must occur every 125 µs with a maximum instantaneous phase titter of ± 30 µs.
2. In IDL2 8– and 10–bit formats, $\overline{TSEN}$ is valid during the B1, B2, and D channel timeslots. $\overline{TSEN}$ will be aligned with data on the D_{out} pin.
3. In IDL2 Slave mode, DCL may be any frequency multiple of 8 kHz between 256 kHz and 4.096 MHz inclusive.

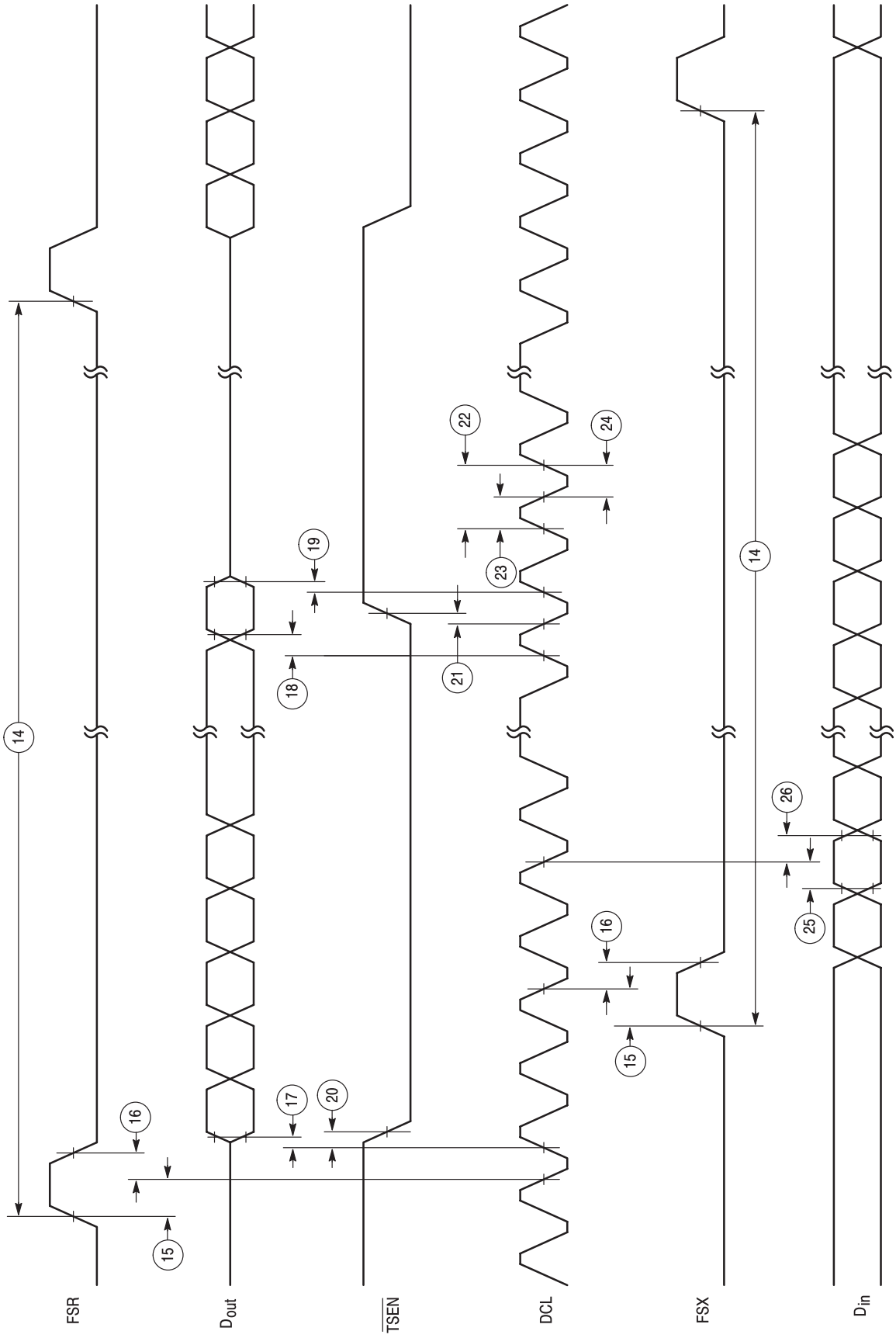


Figure 10–2. IDL Short Frame Sync Slave Timing, 8– and 10–Bit Formats

10.7.3 IDL2 Master Long Frame Sync, 8- and 10-Bit Formats

Ref. No.	Parameter	Min	Max	Unit	Note
27	FSR or FSX Period	125	—	µs	1
28	Delay From Rising Edge of DCL to Rising Edge of FSR or FSX	—	30	ns	
29	Delay From Rising Edge of DCL to Falling Edge of FSR or FSX	—	30	ns	2
30	Delay From Rising Edge of FSR to Low–Z and Valid Data on D_{out}	—	30	ns	
31	Delay From Rising Edge of DCL to Data Valid on D_{out}	—	30	ns	
32	Delay From Rising Edge of DCL to High–Z on D_{out}	5	30	ns	
33	DCL Clock Period	391	1953	ns	3
34	DCL Pulse Width High	45	55	% of DCL Period	
35	DCL Pulse Width Low	45	55	% of DCL Period	
36	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)	25	—	ns	
37	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)	25	—	ns	
38	Delay From Rising Edge of FSR to $\overline{TSEN}$ Low	—	30	ns	4
39	Delay From Falling Edge of DCL to $\overline{TSEN}$ High	—	30	ns	

NOTES:
1. FSR or FSX occurs on average every 125 µs.
2. The duty cycle of DCL is between 45% and 55% when operated in Master Timing mode. This duty cycle is guaranteed for all DCL clocks, except the clock that is used for making timing adjustments, in order to maintain synchronization with the received signal when operating in NT mode. This timing adjustment does not occur during the 2B+D data transfer. The timing adjustment is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive IDL frames, once per U–Interface basic frame. The total adjustment is 96 ns distributed over the two IDL frames.
3. In IDL Master Long Frame Sync mode, the FSR or FSX pulse is eight DCL clock periods long.
4. The DCL frequency may be 512 kHz, 2.048 MHz, or 2.56 MHz.
5. In IDL 8– and 10–bit formats, $\overline{TSEN}$ can be valid during the B1, B2, and D channel timeslots.

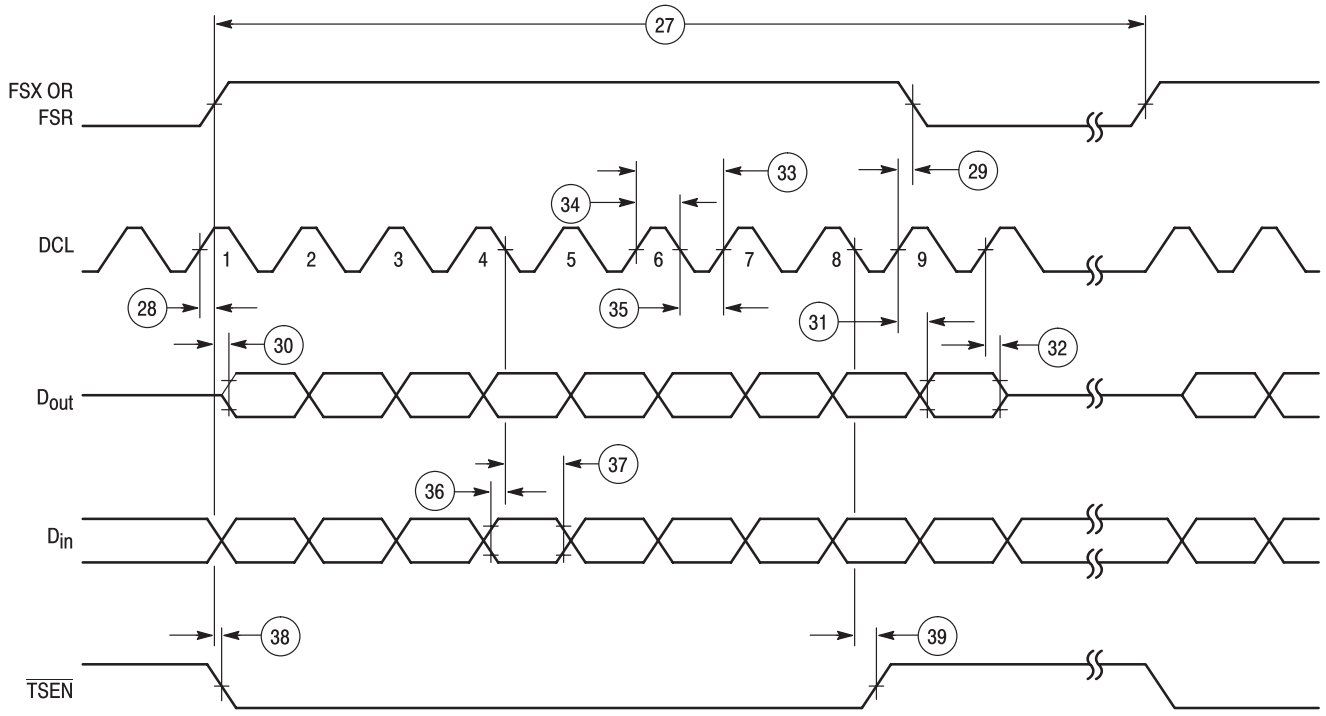


Figure 10–3. Long Frame Sync Master Timing, 8– and 10–Bit Formats

10.7.4 IDL2 Slave Long Frame Sync, 8- and 10-Bit Formats

Ref. No.	Parameter	Min	Max	Unit	Note
40	FSR or FSX Period	125	—	µs	1
41	FSR or FSX High Before the Falling Edge of DCL (FSR or FSX Setup Time)	25	—	ns	2
42	FSR or FSX High After the Falling Edge of DCL (FSR or FSX Hold Time)	25	—	ns	2
43	FSR or FSX Low Before the Falling Edge of DCL	25	—	ns	2
44	Delay From Rising Edge of FSR to Low–Z and Valid Data on D_{out}	—	30	ns	
45	Delay From Rising Edge of DCL to Data Valid on D_{out}	—	30	ns	
46	Delay From Rising Edge of DCL to High–Z on D_{out}	5	30	ns	
47	Delay From Rising Edge of FSR to $\overline{TSEN}$ Low	—	30	ns	3
48	Delay From Falling Edge of DCL to $\overline{TSEN}$ High	—	30	ns	
49	DCL Clock Period	244	1953	ns	4
50	DCL Pulse Width High	45	55	% of DCL Period	
51	DCL Pulse Width Low	45	55	% of DCL Period	
52	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)	25	—	ns	
53	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)	25	—	ns	

NOTES:
1. FSR or FSX occurs on average every 125 µs. FSX and FSR/FSC must occur every 125 µs with a maximum instantaneous phase titter of ± 30 µs.
2. FSR or FSX should be asserted for at least two DCL clock cycles and at most eight DCL clock cycles.
3. In IDL 8– and 10–bit formats, $\overline{TSEN}$ is valid during the B1, B2, and D channel timeslots. $\overline{TSEN}$ will be aligned with data on the D_{out} pin.
4. In IDL Slave mode, DCL may be any frequency that is a multiple of 8 kHz and is between 256 kHz and 4.096 MHz inclusive.

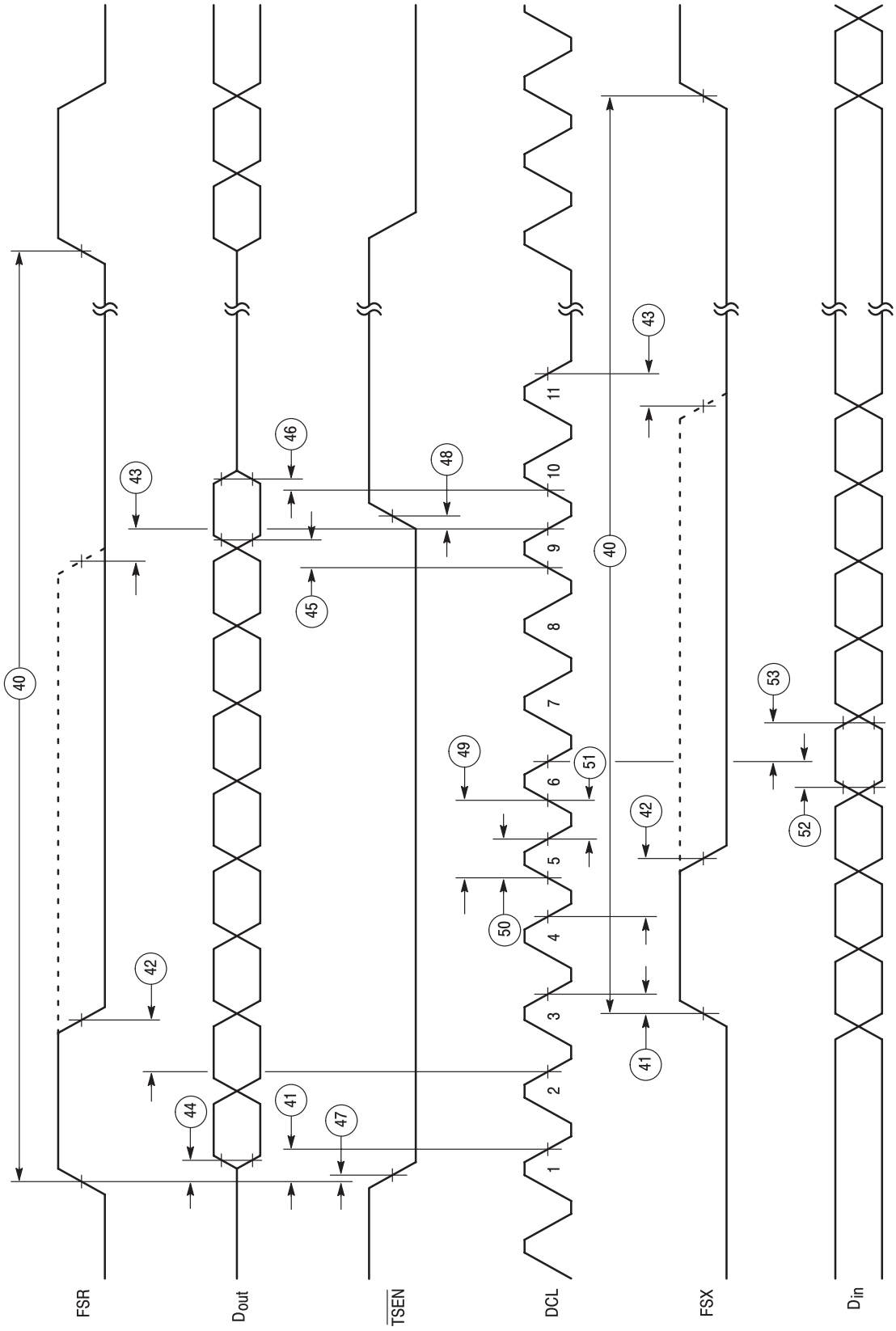


Figure 10–4. Long Frame Sync Slave Timing, 8– and 10–Bit Formats

10.8 GCI TIMING

Ref. No.	Parameter		Min	Max	Unit	Note
53	Delay From Rising Edge of DCL to FSC Output High		—	30	ns	
54	Delay From Rising Edge of DCL to FSC Output Low (Normal Frame)		—	30	ns	1
55	Delay From Rising Edge of DCL to FSC Output Low (Superframe Marker)		—	30	ns	2
56	FSC Input High Before the Falling Edge of DCL (FSC Setup Time)		25	—	ns	
57	FSC Input High After the Falling Edge of DCL (FSC Hold Time — Superframe Marker)		25	—	ns	1
58	FSC Input High After the Falling Edge of FSC (FSC Hold Time — Normal Frame)		25	—	ns	3
59a	DCL Clock Period Master Mode		488	1953	ns	4
59b	DCL Clock Period Slave Mode		122	1953	ns	5
60	DCL Pulse Width High DCL Clock 249 Pulse Width High DCL Clock 59 Pulse Width High	512 kHz 2.048 kHz 2.048 MHz 512 kHz	878 210 160 825	1074 265 315 1120	ns	6
61	DCL Pulse Width Low		45	55	% of DCL Period	
62	DCL Fall Time		5	15	ns	
63	DCL Rise Time		5	15	ns	
64	Delay From Rising Edge of FSC to Low–Z and Valid Data on D_{out}		—	30	ns	
65	Delay From Rising Edge of DCL to Data Valid on D_{out}		—	30	ns	
66	Delay From Rising Edge of DCL High–Z on D_{out}		5	30	ns	
67	Data Valid on D_{in} Before Rising Edge of DCL		25	—	ns	
68	Data Valid on D_{in} After Rising Edge of DCL		25	—	ns	
69	Delay From Rising Edge of FSC to $\overline{TSEN}$ Low		—	30	ns	
70	Delay From Rising Edge of DCL to $\overline{TSEN}$ High		—	30	ns	

NOTES:

1. The FSC pulse is normally two DCL clock periods wide.
2. The FSC pulse is only one DCL clock period wide at the start of a superframe. Every 96th FSC pulse marks the start of a superframe.
3. To mark the beginning of a superframe (i.e., to flag the 2B+D data of the current frame as the first data in the transmitted superframe) the FSC pulse should be only one DCL clock period wide. If the FSC pulse is not modulated as such the MC145572 will randomly chose an FSC frame as the first to be transmitted.
4. In GCI Master mode, the MC145572 will output a 512 kHz or 2.048 MHz clock as selected by CLKSEL.
5. In GCI Slave mode, DCL may be any frequency that is a multiple of 512 kHz and is between 512 kHz and 8.192 MHz.
6. The duty cycle of DCL is between 45% and 55% when operated in Master Timing mode. This duty cycle is guaranteed for all DCL clocks, except the clock that is used for making timing adjustments, in order to maintain synchronization with the received signal when operating in NT mode. In NT Master mode, the MC145572 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive GCI frames, once per U–interface basic frame. The total adjustment is 96 ns distributed over the two frames. When DCL is configured for 2.048 MHz, the adjustment occurs during clock pulse number 249 after FSC. The count starts at clock pulse 0 for the DCL clock immediately coincident with FSC being driven high. When DCL is configured for 512 kHz the adjustment occurs during DCL pulse number 59. It is important to remember this when programming the GCI timeslot, since it is possible for data to be transferred during the clock period where the timing adjustment is being made and this may effect setup and hold times for other components in a system.

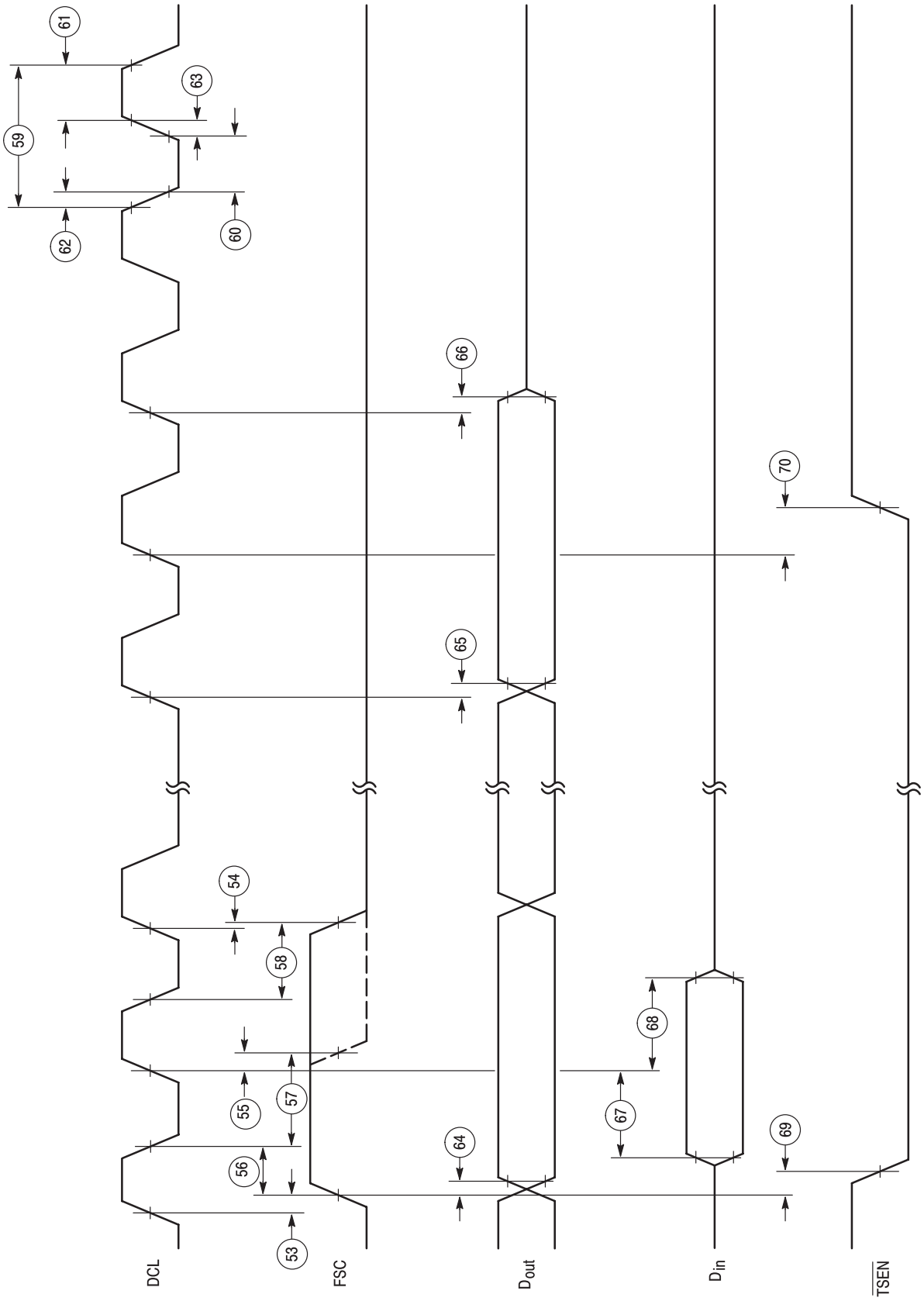


Figure 10–5. GCI Timing

10.9 D-CHANNEL PORT TIMING

10.9.1 IDL2 (Master or Slave) Short Frame Sync 8-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
71	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
72	Delay From DCHCLK Rising Edge to Data Valid on DCH_{out}	—	30	ns	
73	Data Valid on DCH_{in} Before Falling Edge of DCHCLK (DCH_{in} Setup Time)	25	—	ns	
74	Data Valid on DCH_{in} After Falling Edge of DCHCLK (DCH_{in} Hold Time)	25	—	ns	

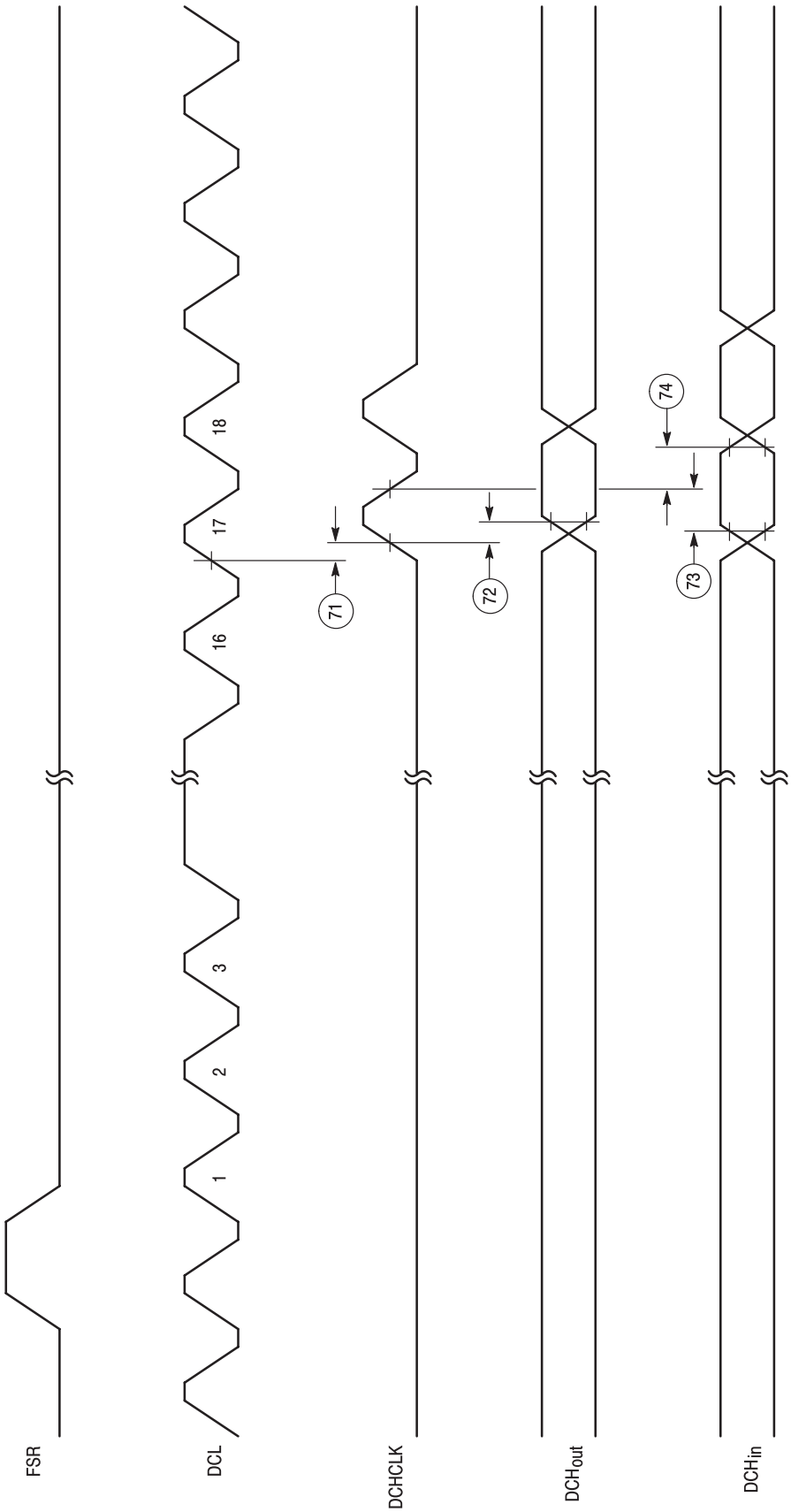


Figure 10–6. IDL2 (Master or Slave) Short Frame Sync 8–Bit Format, D Channel Port Timing

10.9.2 IDL2 (Master or Slave) Short Frame Sync 10-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
75	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
76	Delay From DCHCLK Rising Edge to Data Valid on DCH_{out}	—	30	ns	
77	Data Valid on DCH_{in} Before Falling Edge of DCHCLK (DCH_{in} Setup Time)	25	—	ns	
78	Data Valid on DCH_{in} After Falling Edge of DCHCLK (DCH_{in} Hold Time)	25	—	ns	

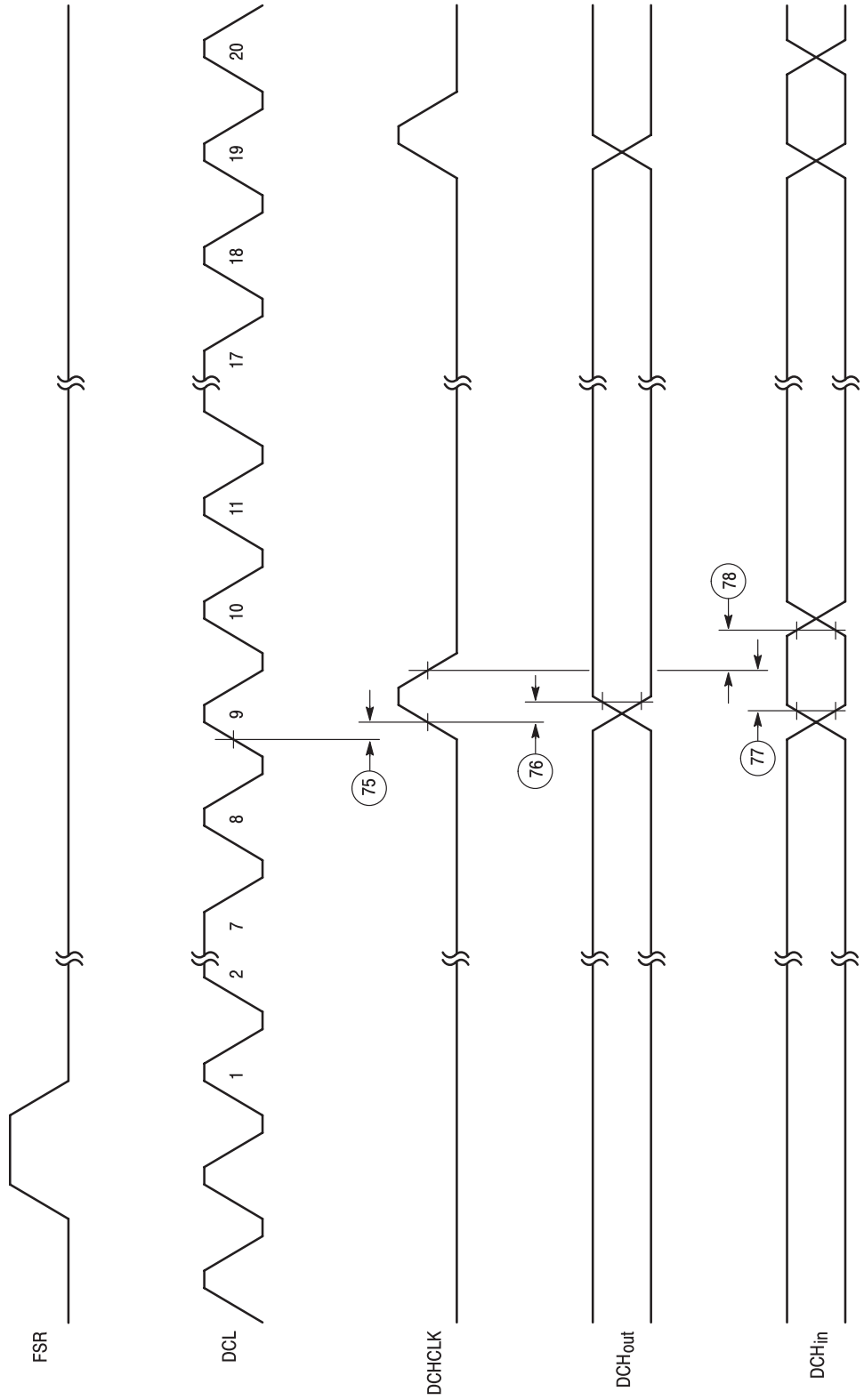


Figure 10–7. IDL2 (Master or Slave) Short Frame Sync 10–Bit Format, D Channel Port Timing

10.9.3 IDL2 (Master or Slave) Long Frame Sync 8-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
79	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
80	Delay From DCHCLK Rising Edge to Data Valid on DCH_{out}	—	30	ns	
81	Data Valid on DCH_{in} Before Falling Edge of DCHCLK (DCH_{in} Setup Time)	25	—	ns	
82	Data Valid on DCH_{in} After Falling Edge of DCHCLK (DCH_{in} Hold Time)	25	—	ns	

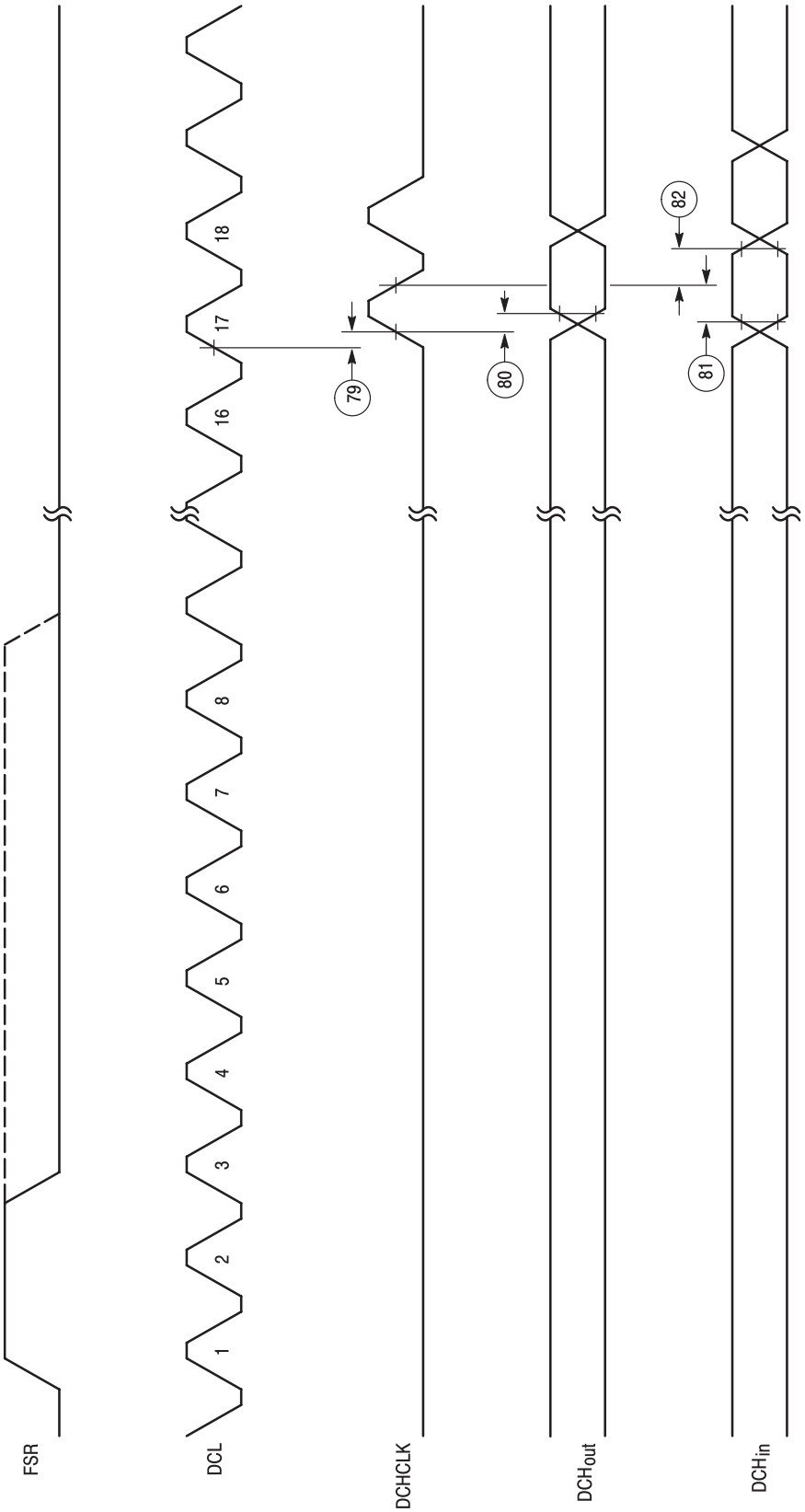


Figure 10–8. IDL2 (Master or Slave) Long Frame Sync 8–Bit Format, D Channel Port Timing

10.9.4 IDL2 (Master or Slave) Long Frame Sync 10-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
83	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
84	Delay From DCHCLK Rising Edge to Data Valid on DCH_{out}	—	30	ns	
85	Data Valid on DCH_{in} Before Falling Edge of DCHCLK (DCH_{in} Setup Time)	25	—	ns	
86	Data Valid on DCH_{in} After Falling Edge of DCHCLK (DCH_{in} Hold Time)	25	—	ns	

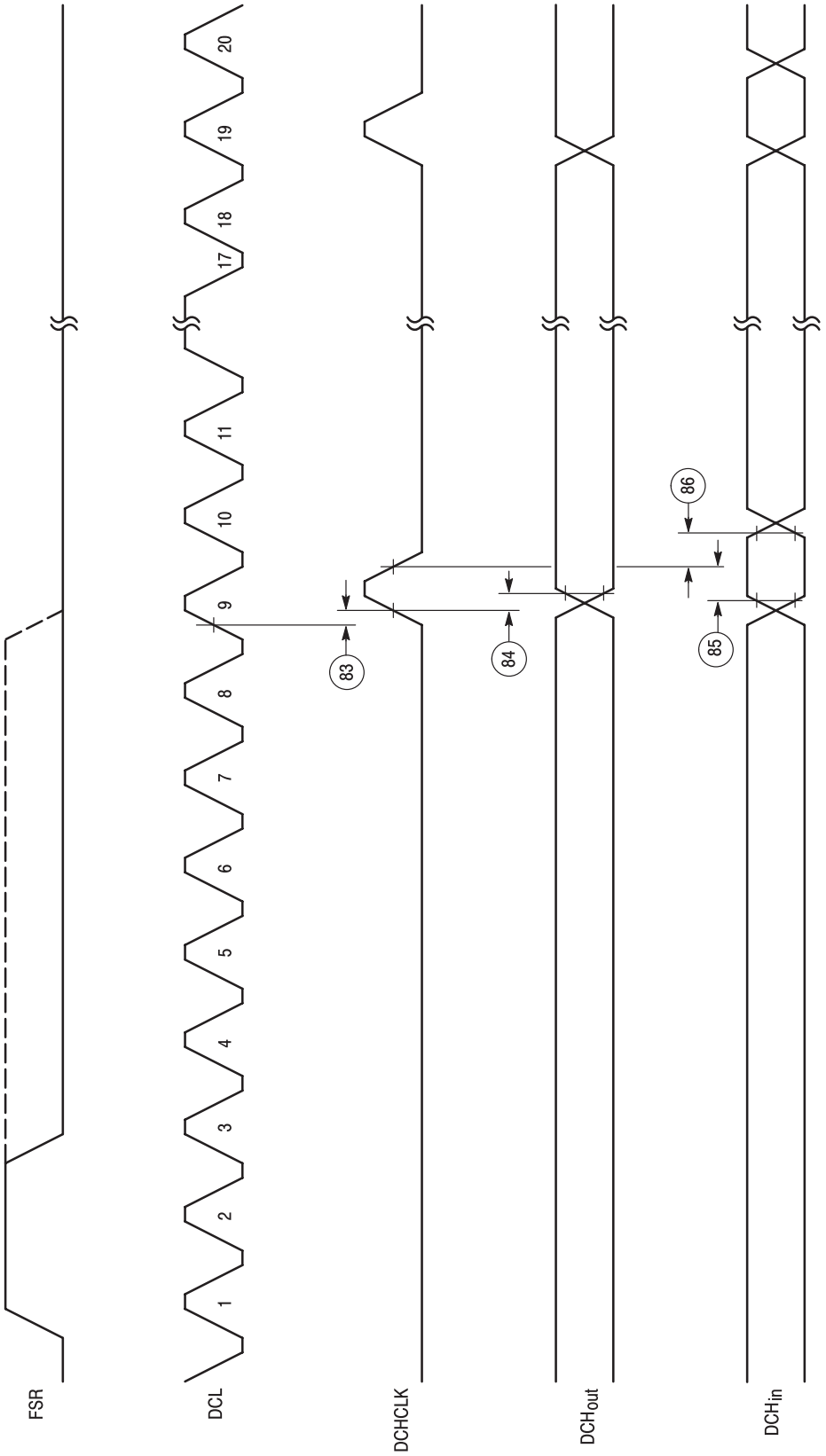


Figure 10–9. IDL2 (Master or Slave) Long Frame Sync 10–Bit Format, D Channel Port Timing

10.10 SUPERFRAME TRANSMIT AND RECEIVE (SFAX/SFAR) TIMING

10.10.1 SFAX Input Timing in IDL2 (Master or Slave) Short Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
91	FSX Period	125	—	µs	1
92	SFAX Period	12.0	—	ms	2
93	SFAX Input High Before Falling Edge of DCL (SFAX Setup Time)	25	—	ns	3
94	SFAX Input High After Falling Edge of DCL (SFAX Hold Time)	25	—	ns	

NOTES:
1. See **Section 10.7** for FSX jitter requirements and specifications.
2. SFAX must occur every 96 FSX 8 kHz frames.
3. SFAX is sampled on the next DCL falling edge after FSX is asserted.

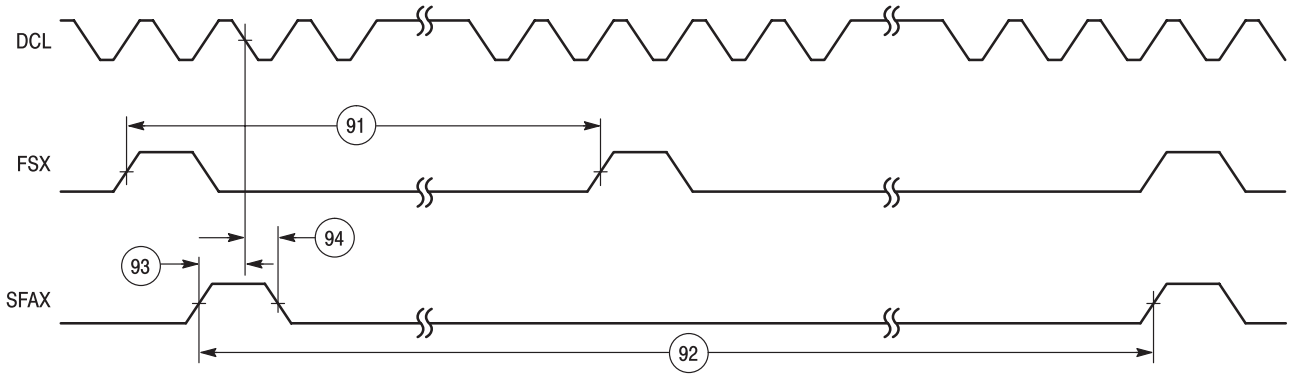


Figure 10–10. SFAX Input Timing in IDL2 (Master or Slave) Short Frame Mode

10.10.2 SFAX Input Timing in IDL2 (Master or Slave) Long Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
95	Delay From Rising Edge of DCL to Rising Edge of FSR or FSX	—	30	ns	
96	FSR or FSX High Before the Falling Edge of DCL (FSR or FSX Setup Time)	25	—	ns	
97	FSR or FSX High After the Falling Edge of DCL (FSR or FSX Hold Time)	25	—	ns	
98	FSX Period	125	—	µs	1
99	SFAX Period	12.0	—	ms	2
100	SFAX Input High Before Rising Edge of FSX (SFAX Setup Time)	25	—	ns	3
101	SFAX Input High After Rising Edge of FSX (SFAX Hold Time)	25	—	ns	

NOTES:
1. See **Section 10.**7 for FSX jitter requirements and specifications.
2. SFAX must occur every 96 FSX 8 kHz frames.
3. SFAX is sampled on the rising edge of FSX.

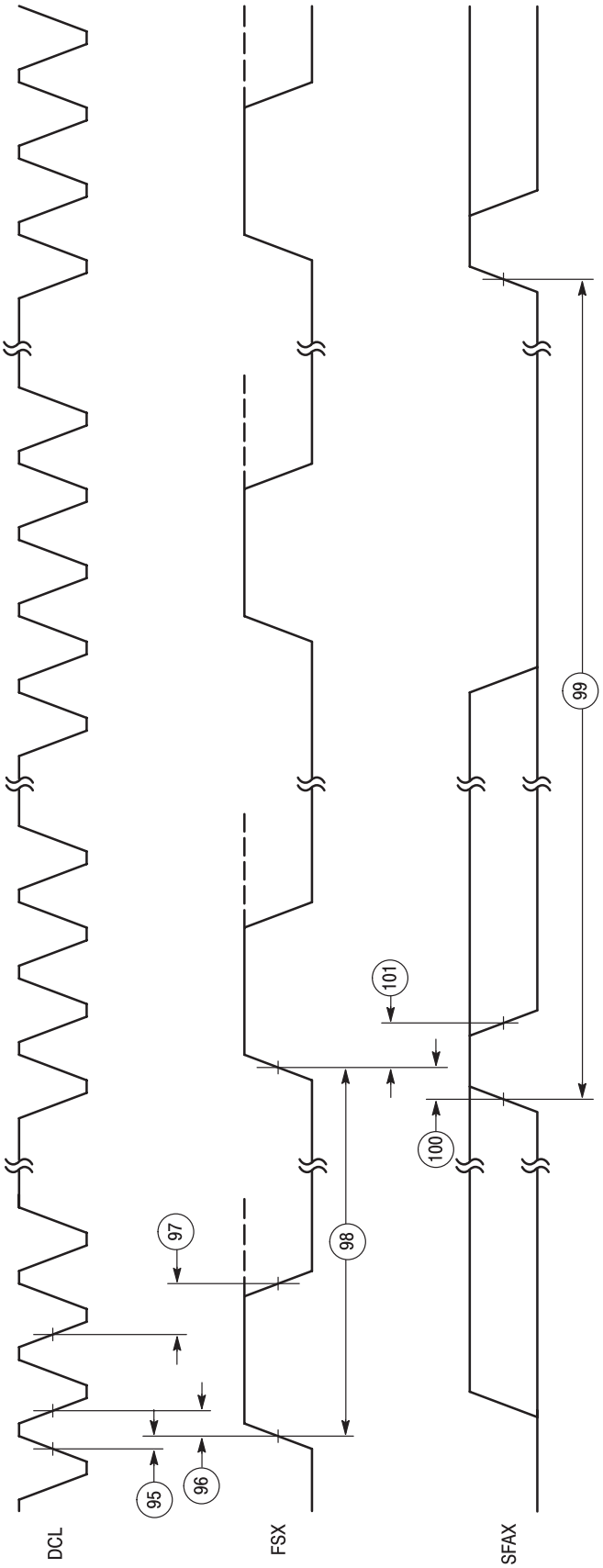


Figure 10–11. SFAX Input Timing in IDL2 (Master or Slave) Long Frame Mode

10.10.3 SFAX/SFAR Output Timing in IDL2 (Master or Slave) Short Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
102	FSX Period	125	—	µs	1
103	SFAX Period	12.0	—	ms	2
104	Delay From the Rising Edge of DCL to the Rising Edge of FSAR or FSAX	—	30	ns	3
105	Delay From the Rising Edge of DCL to the Rising Edge of FSAR or FSAX	—	30	ns	

NOTES:
1. See **Section 10.7** for FSX jitter requirements and specifications.
2. SFAX and SFAR must occur every 96 FSX 8 kHz frames.
3. FAX and SFAR are one DCL clock pulse wide and occur on the next DCL clock pulse after FSX or FSR is asserted.

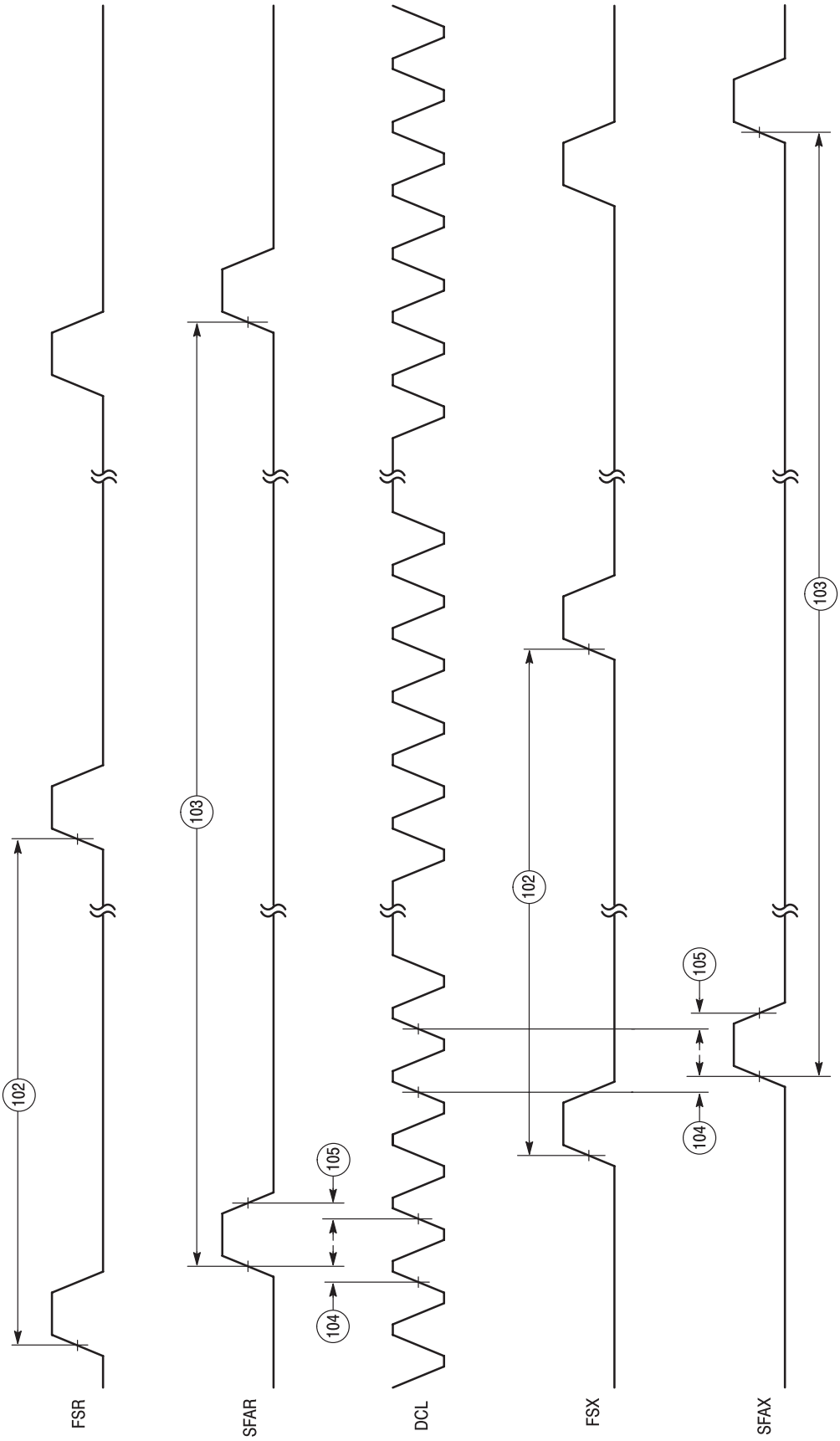


Figure 10–12. SFAX/SFAR Output Timing in IDL2 Short Frame Mode (Master or Slave)

10.10.4 SFAX/SFAR Output Timing in IDL2 (Master or Slave) Long Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
106	FSX or FSR Period	125	—	µs	1
107	SFAX or SFAR Period	12.0	—	ms	2
108	Delay From the Rising Edge of FSR or FSX to the Rising Edge of SFAR or SFAX	—	30	ns	3

NOTES:
1. See **Section 10.7** for FSX jitter requirements and specifications.
2. SFAX and SFAR must occur every 96 FSX 8 kHz frames.
3. SFAX and SFAR occur coincident with FSX and FSR, respectively.

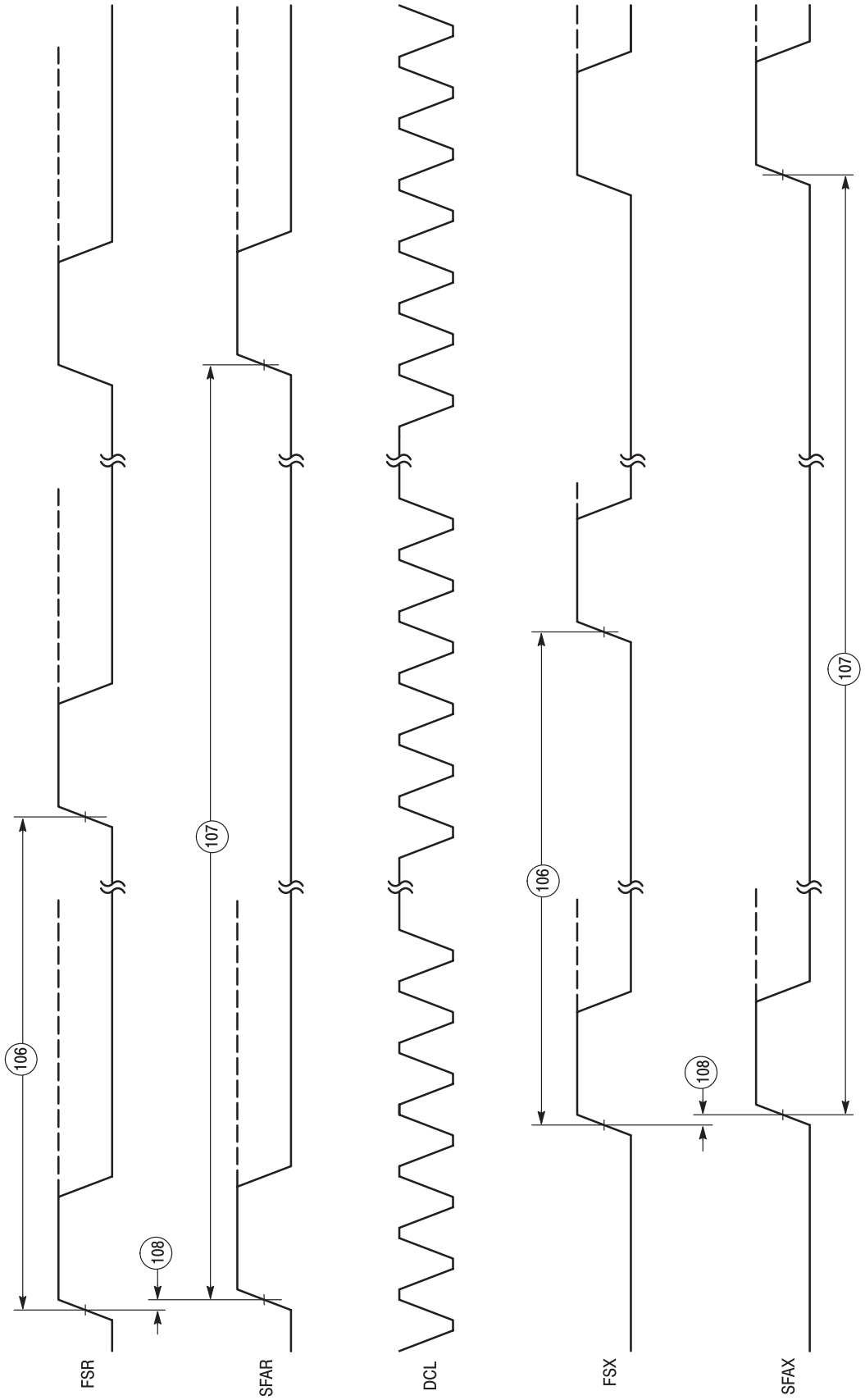


Figure 10–13. SFAX/SFAR Output Timing in IDL2 Long Frame Mode (Master or Slave)

10.11 PARALLEL CONTROL PORT TIMING

10.11.1 Parallel Control Port Write Timing

Ref. No.	Parameter	Min	Max	Unit	Note
109	$\overline{CS}$ Low	110	—	ns	
110	$\overline{CS}$ High	440	—	ns	
111	R/$\overline{W}$ Low Before $\overline{CS}$ Rising Edge (R/$\overline{W}$ Setup Time)	50	—	ns	
112	R/$\overline{W}$ Low After $\overline{CS}$ Rising Edge (R/$\overline{W}$ Hold Time)	30	—	ns	
113	D0 – D7 Valid Before the Rising Edge of $\overline{CS}$ (Data Setup Time)	20	—	ns	
114	D0 – D7 Valid After the Rising Edge of $\overline{CS}$ (Data Hold Time)	20	—	ns	

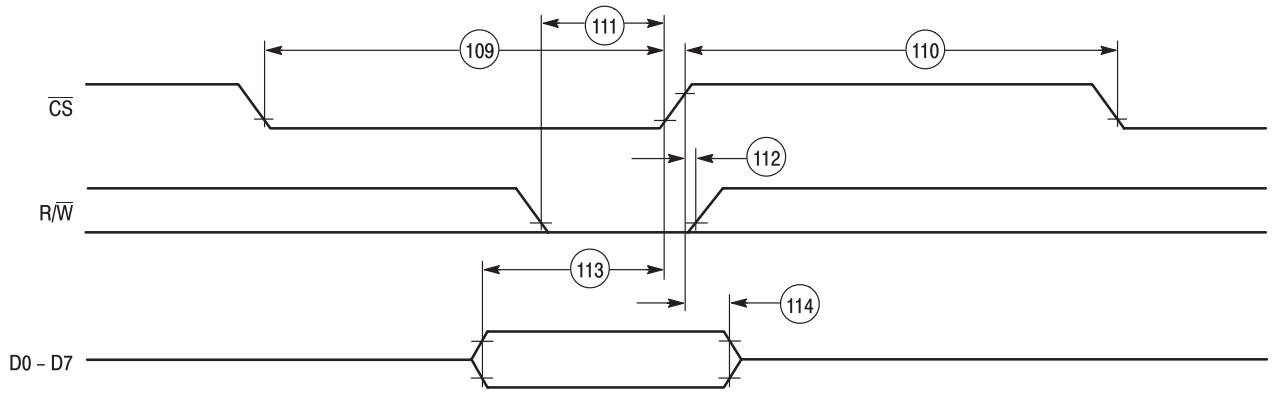


Figure 10–14. Parallel Control Port Write Timing

10.11.2 Parallel Control Port Read Timing

Ref. No.	Parameter	Min	Max	Unit	Note
115	$\overline{CS}$ Low	110	—	ns	
116	$\overline{CS}$ High	440	—	ns	
117	R/$\overline{W}$ High Before $\overline{CS}$ Falling Edge (R/$\overline{W}$ Setup Time)	0	—	ns	
118	R/$\overline{W}$ High After $\overline{CS}$ Rising Edge (R/$\overline{W}$ Hold Time)	20	—	ns	
119	D0 – D7 Valid After the Falling Edge of $\overline{CS}$ (Read Access Time)	—	30	ns	
120	D0 – D7 Valid After the Rising Edge of $\overline{CS}$ (Data Hold Time)	20	50	ns	

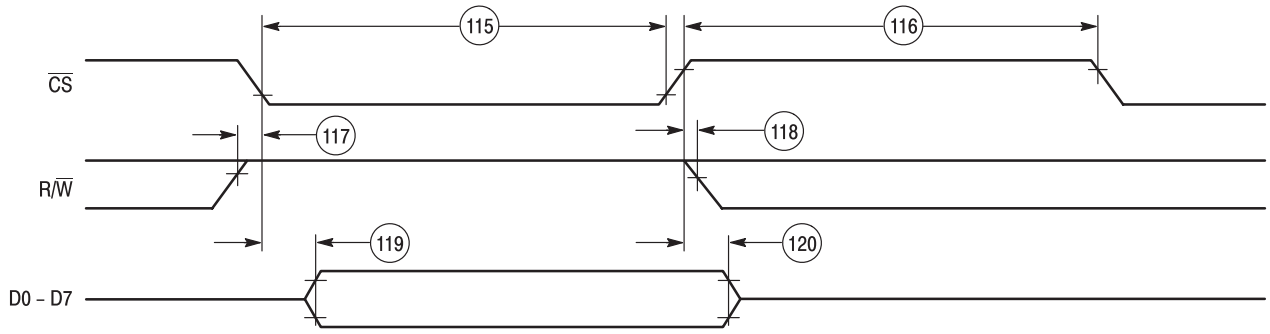


Figure 10–15. Parallel Control Port Read Timing

10.12 SWITCHING CHARACTERISTICS FOR SCP INTERFACE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–2)

Ref. No.	Parameter	Min	Max	Unit
121	SCPCLK Rising Edge Before $\overline{\text{SCPEN}}$(L) Falling Edge	40	—	ns
122	$\overline{\text{SCPEN}}$ Falling Edge Before SCPCLK Rising Edge	40	—	ns
123	SCPRx Data Valid Before SCPCLK Rising Edge (Setup Time)	20	—	ns
124	SCPRx Data Valid After Rising Edge of SCPCLK (Hold Time)	20	—	ns
125	SCPCLK Frequency	—	4.1	MHz
126	SCPCLK Width Low	50	—	ns
127	SCPCLK Width High	50	—	ns
128	SCPCLK Rising Edge Before $\overline{\text{SCPEN}}$(L) Rising Edge (See Note 2)	40	—	ns
129	$\overline{\text{SCPEN}}$ Rising Before SCPCLK Rising Edge (See Note 2)	40	—	ns
130	SCPCLK Falling Edge to SCPTx Low–Z	—	40	ns
131	SCPCLK Falling Edge (While $\overline{\text{SCPEN}}$(L) is Low) to SCPTx Data Valid	—	40	ns
132	$\overline{\text{SCPEN}}$ Rising Edge to SCPTx High–Z	—	30	ns
133	$\overline{\text{SCPEN}}$ Falling Edge to SCPTx Active (Byte Mode)	0	40	ns

NOTES:
1. Measurements are made from the point at which they achieve their guaranteed minimum or maximum logic levels.
2. $\overline{\text{SCPEN}}$ must rise between the rising edge of the eighth SCPCLK and the rising edge of the ninth SCPCLK for an 8–bit access or the access will be ignored. For a 16–bit access, $\overline{\text{SCPEN}}$ must rise between the rising edge of the sixteenth SCPCLK and the rising edge of the seventeenth SCPCLK or the access will be ignored.

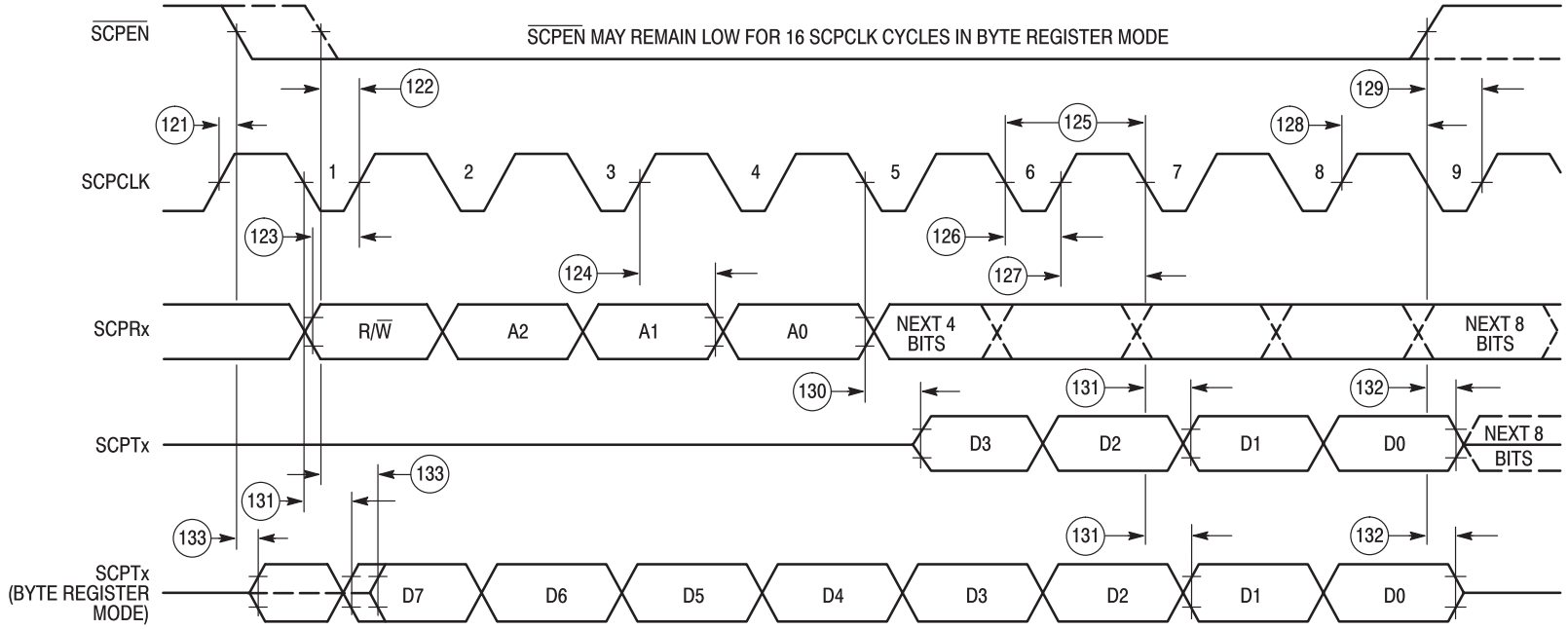


Figure 10–16. SCP Interface Timing

NOTE: In byte mode read operations, the SCPTx pin is enabled when SCPCLK goes low and $\overline{\text{SCPEN}}$ has gone low.
If SCPCLK is low prior to $\overline{\text{SCPEN}}$ going low, then SCPTx remains in a high impedance state until $\overline{\text{SCPEN}}$ goes low.

10.13 SWITCHING CHARACTERISTICS FOR SYSCLK AND EYEDATA

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–13)

Ref. No.	Parameter	Min	Max	Unit
134	SYSCLK Rising Edge to EYEDATA Valid	– 35	35	ns

NOTE: Measurements are made from the point at which they achieve their guaranteed minimum or maximum logic levels.

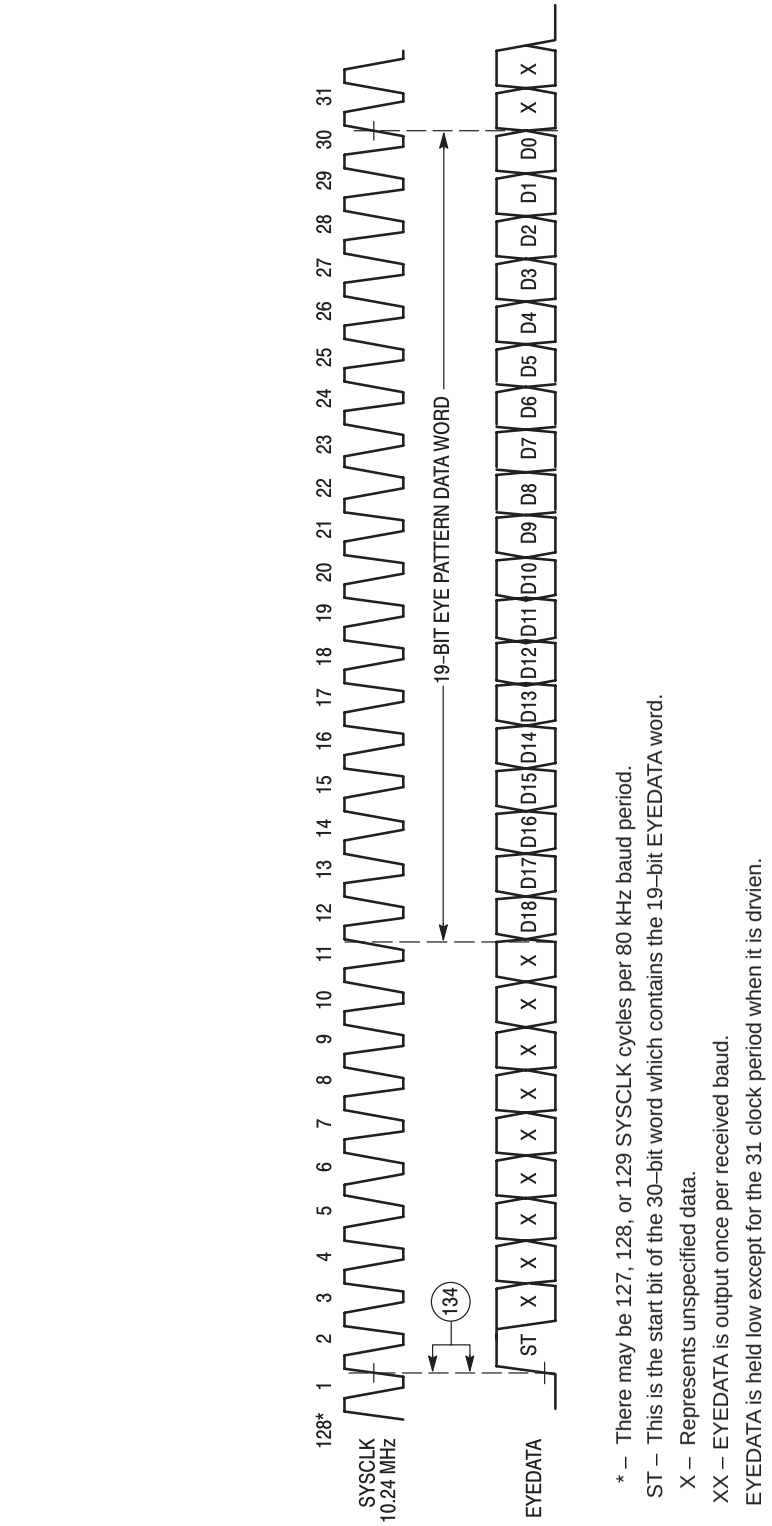


Figure 10–17. SYSCLK and EYEDATA Timing

10.14 SWITCHING CHARACTERISTICS FOR CRYSTAL INPUT, CLKOUT, BUFXTAL, AND FREQREF

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–14)

Ref. No.	Parameter	Min	Typ	Max	Unit
135a	FREQREF Minimum Pulse Width Low (LT Mode Only)	20	—	—	ns
135b	FREQREF Minimum Pulse Width High (LT Mode Only)	20	—	—	ns
136	BUFXTAL Duty Cycle at 20.48 MHz	45	50	55	%
137	BUFXTAL Output High to IDL Clock Output High (IDL Master Mode)	—	—	35	ns
138	BUFXTAL Output High to IDL Clock Output Low (IDL Master Mode)	—	—	35	ns
139	BUFXTAL Output Low to 4096 kHz Clock Output Low	—	—	35	ns
140	$XTAL_{in}$ Duty Cycle, for External Clock Source	45	—	55	%
141	LT Mode $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance, FREQREF Connected to Either V_{DD} or V_{SS}	—	—	45	pF
142	LT Mode $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance, FREQREF Much Greater Than 8 kHz	15	—	—	pF
143	NT Mode $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance	15	—	45	pF
144	NT Mode Deactivated Condition $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance	—	24	—	pF
145	$XTAL_{out}$ Drive Level	—	1	—	mW

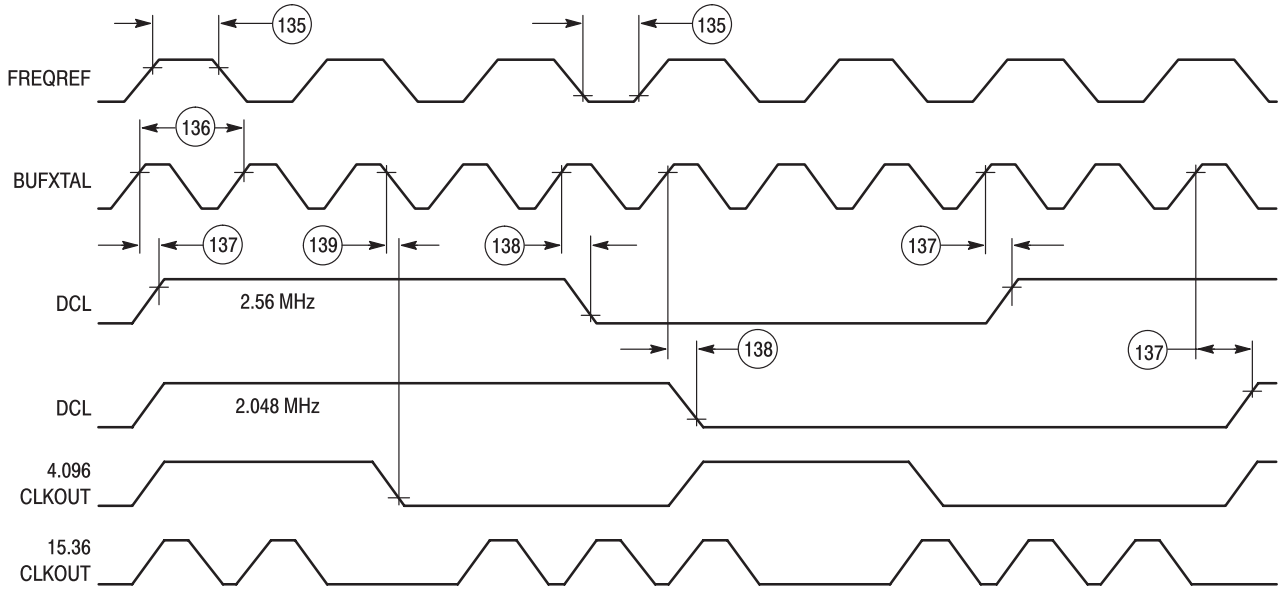


Figure 10–18. Clock Timing

10.15 SWITCHING CHARACTERISTICS FOR BAUD CLOCKS

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–15)

Ref. No.	Parameter	Min	Typ	Max	Unit
147	2B1Q Baud Period	—	12.5	—	µs
148	Start of 2B1Q Baud to Tx Baud Clock Rising Edge	—	9	—	µs
149	Tx Baud Clock Width High, Rx Baud Clock TxSFS	75	90	100	ns
150	Superframe Period	—	12	—	ms

NOTE: Measurements are made from the point at which they achieve their guaranteed minimum or maximum logic levels.

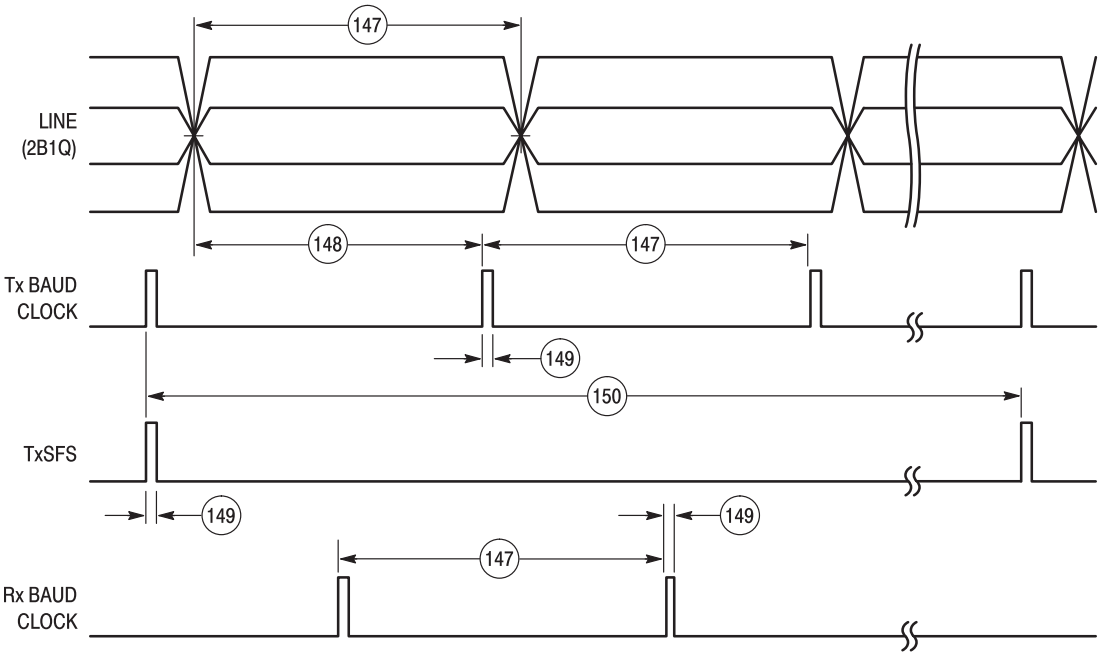


Figure 10–19. Baud Clock Timing

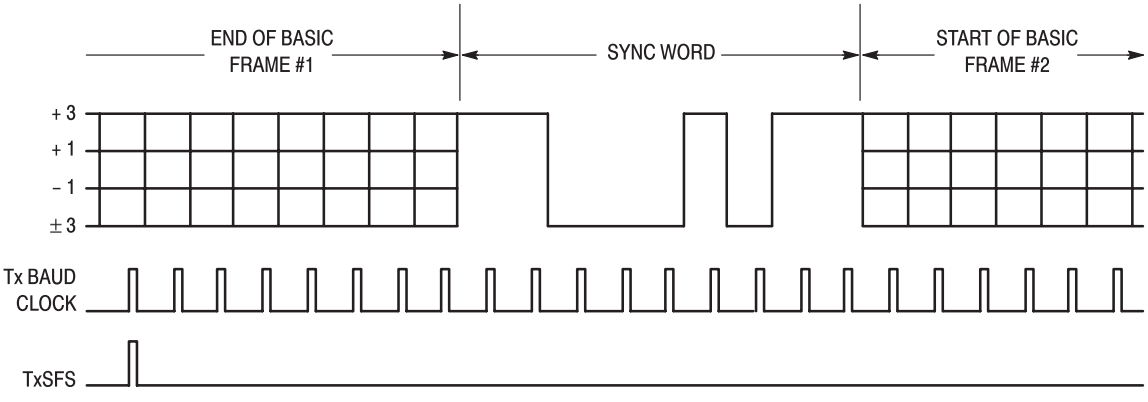


Figure 10–20. Tx Superframe Sync Pulse Alignment

11
MECHANICAL DATA

11.1 PIN ASSIGNMENTS

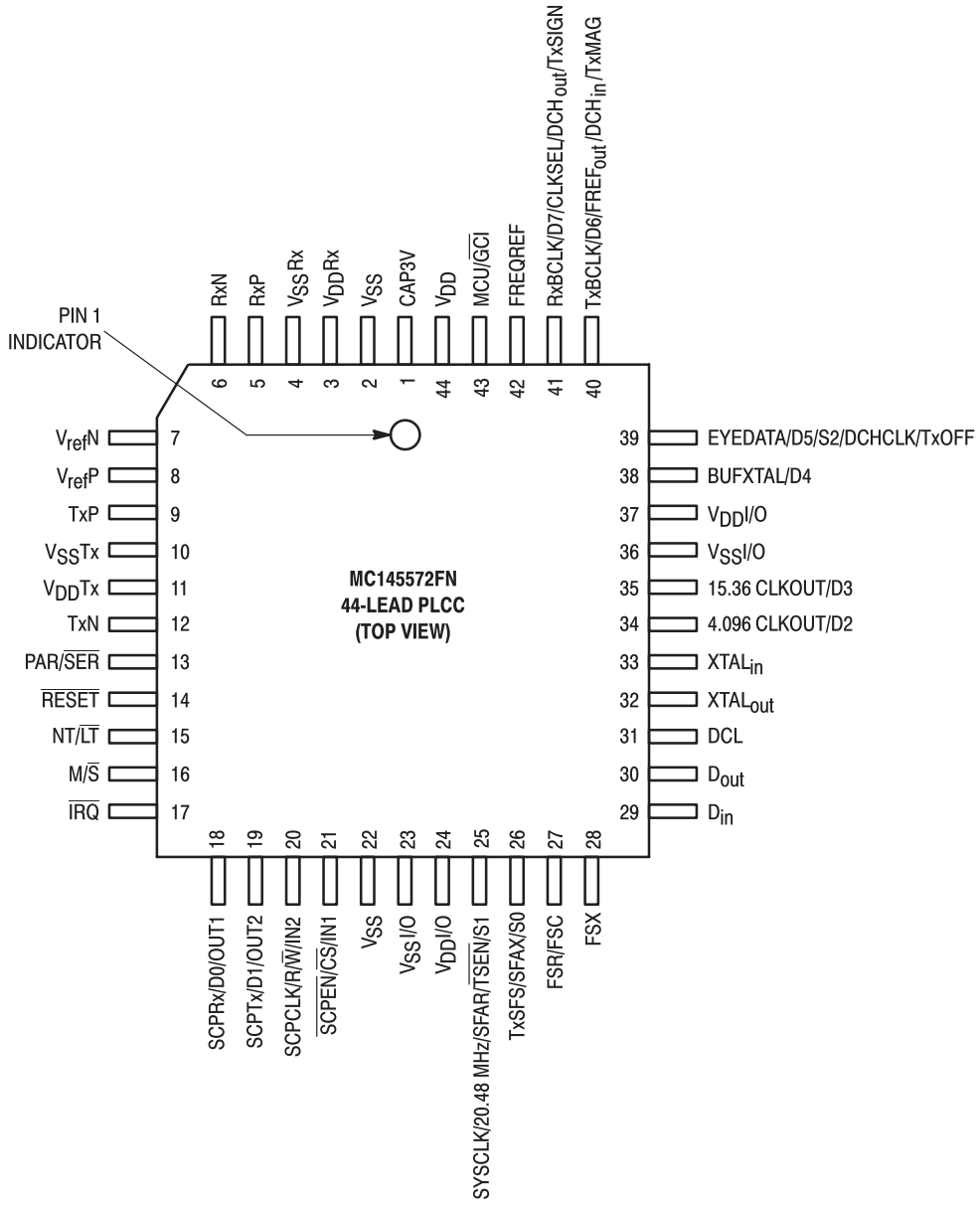


Figure 11–1. MC145572FN Pin Assignment

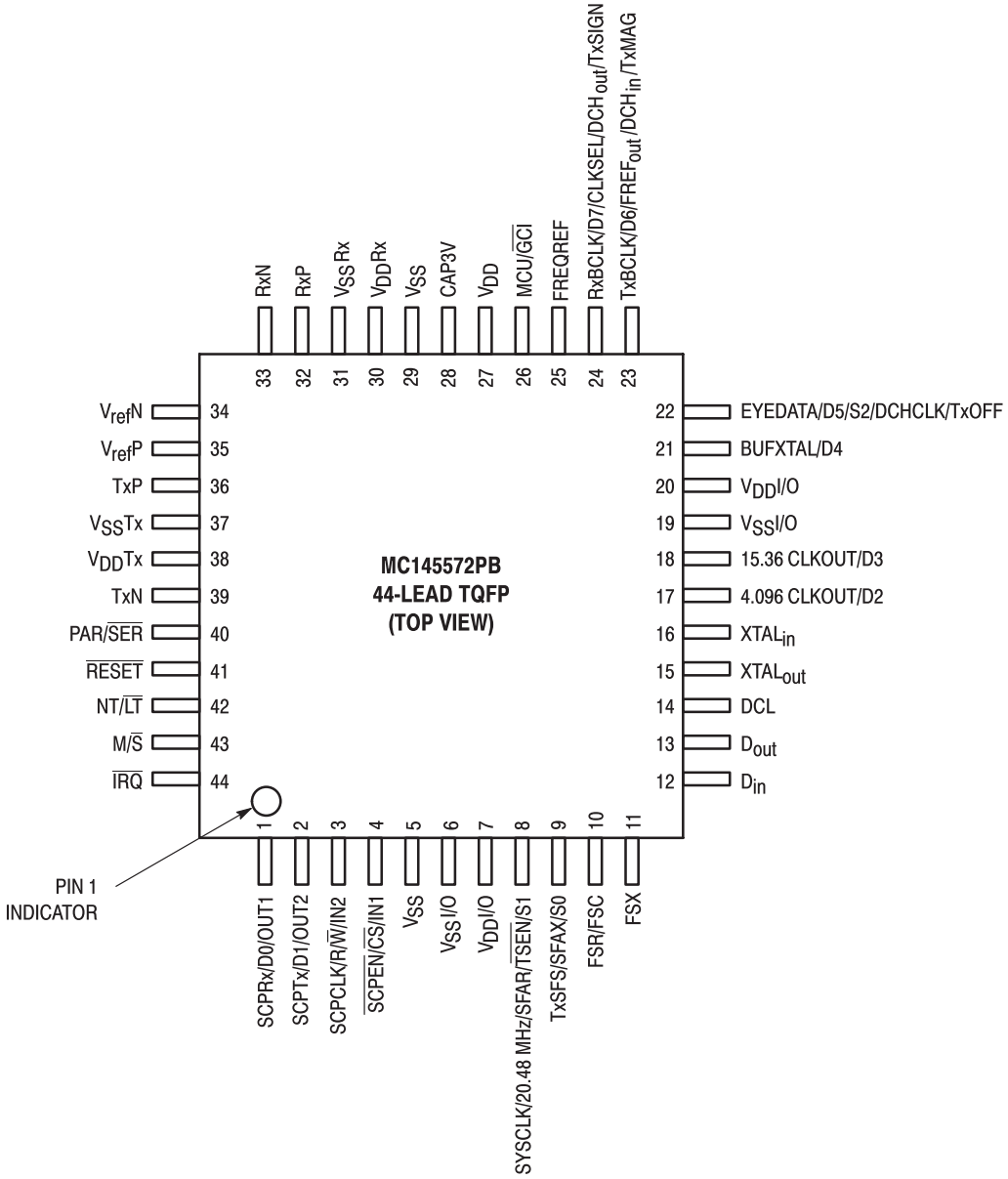
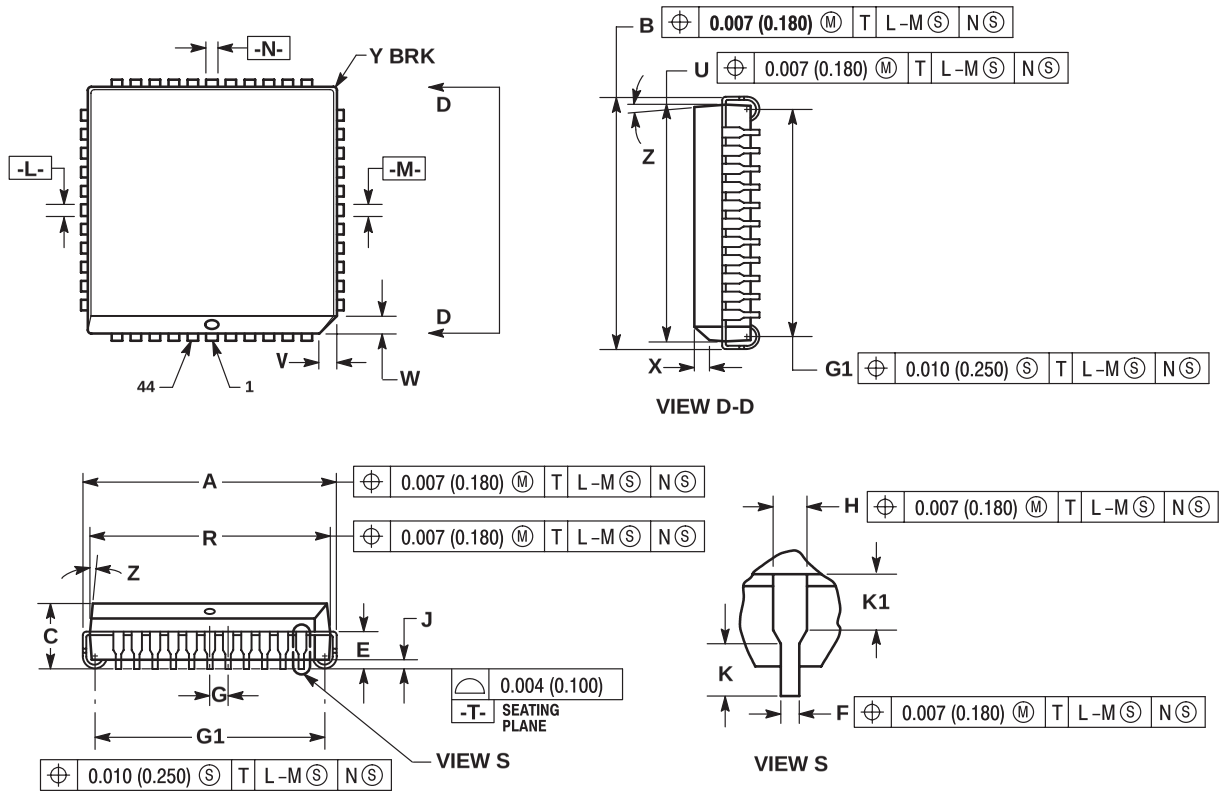


Figure 11–2. MC145572PB Pin Assignment

11.2 PACKAGE DIMENSIONS

PLCC PACKAGE
CASE 777-02

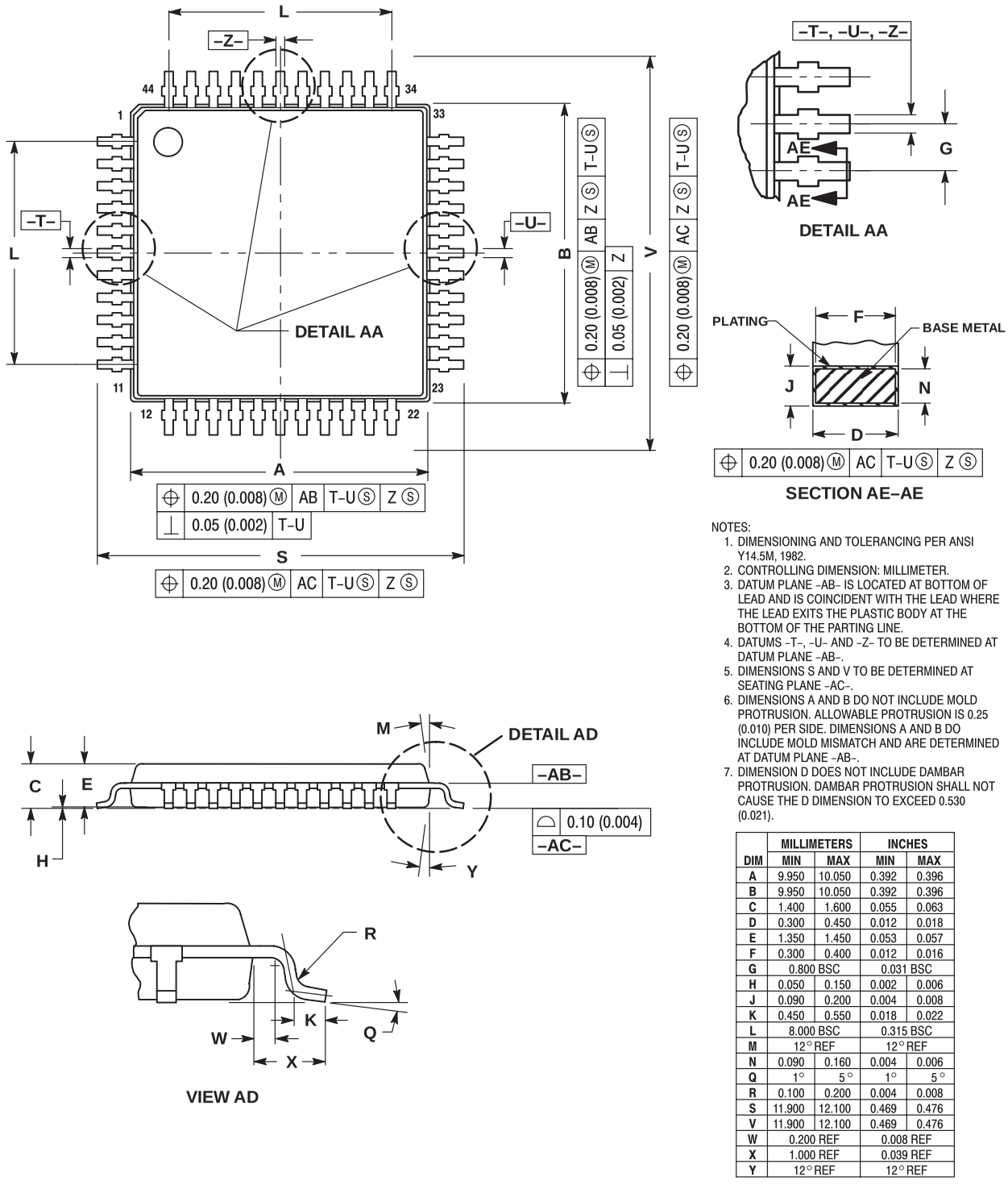


NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS (0.010) 0.25 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

Figure 11–3. MC145572FN Mechanical Outline

TQFP PACKAGE
CASE 824D–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U– AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	8.000 BSC		0.315 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

Figure 11–4. MC145572PB Mechanical Outline

A

MC145572EVK ISDN U-INTERFACE TRANSCEIVER EVALUATION KIT

A.1 INTRODUCTION

The MC145572EVK ISDN U–Interface Transceiver Evaluation Kit provides Motorola ISDN customers a convenient and efficient vehicle for evaluating the MC145572 ISDN U–interface transceiver. The approach taken to demonstrate the MC145572 ISDN U–interface transceiver is to provide the user with a fully functional NT1 connected to an LT. An NT1 provides transparent 2B+D data transfer between the U– and S/T–interfaces. In addition, it must also provide for network–initiated maintenance procedures. It does not, however, provide any interface to higher level protocols — this functionality is left to entities such as the NT2.

The MC145572EVK ISDN U–Interface Evaluation Kit can be physically and functionally separated into two “halves”. The left side of the card is the NT1, while the right side of the card is the LT. Alternatively, it can be thought of as having both ends of the two wire U–interface, extending from the customer premise (NT1) to the digital switch line card (LT), on a single standalone evaluation board.

The kit provides the ability to interactively manipulate status registers in the MC145572 ISDN U–interface transceiver as well as in the MC145474/75 S/T–interface transceiver with the aid of an external terminal or PC. A unique combination of hardware and software features allows for standalone or terminal activation of the U–interface and as such provides an excellent platform for NT1 and LT hardware/software development.

The MC145572EVK ISDN U–Interface Evaluation Kit can be interfaced directly to the MC68302 Integrated Multiprotocol Processor Development System to aid in the hardware and software development of S/T– and U–interface terminal equipment.

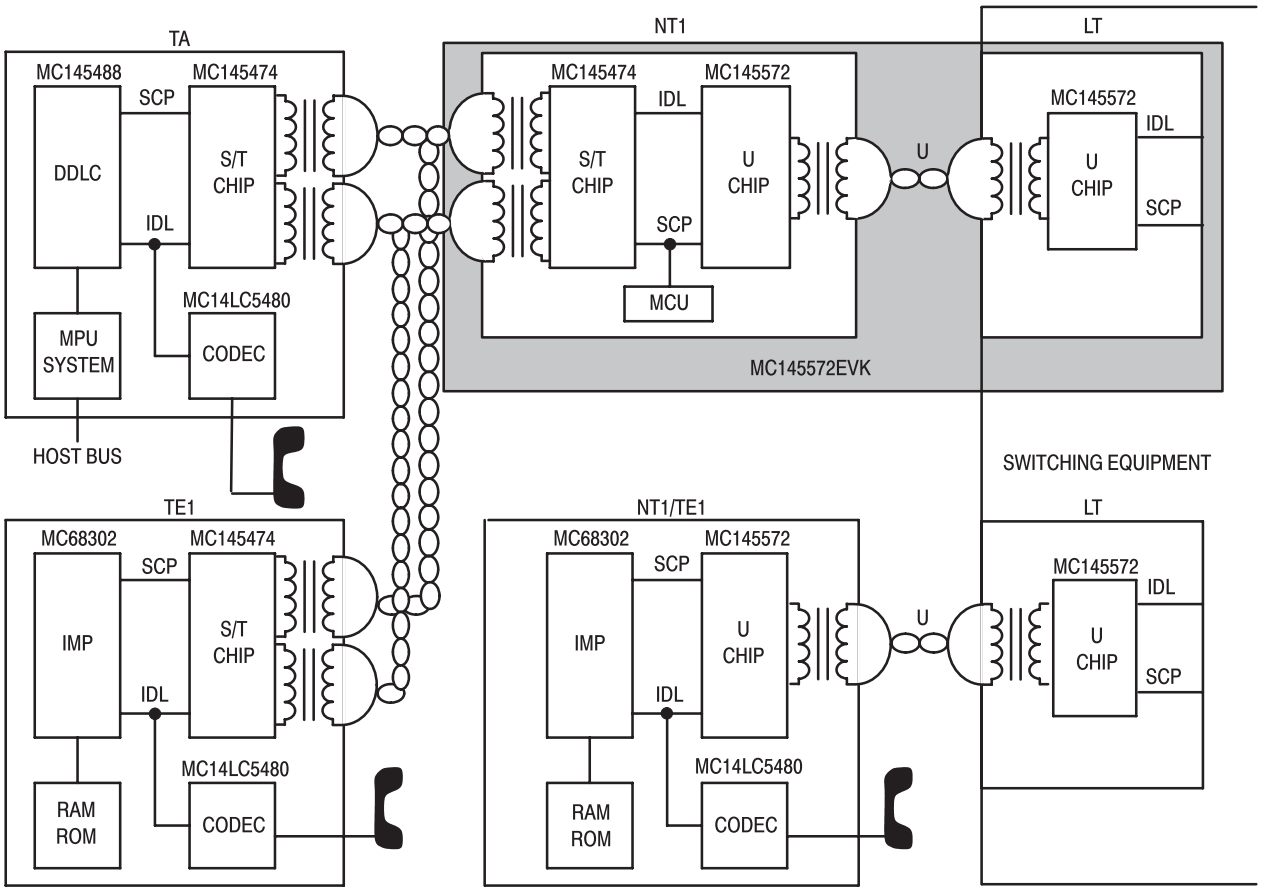


Figure A–1. Motorola Silicon Applications and the MC145572EVK

A.2 FEATURES

A.2.1 General

- Provides Standalone LT and NT1 on Single Board
- Board Can Be Broken Apart Providing Separate LT and NT1
- On–Board Microcontrollers with Resident Monitor Software
- Convenient Access to Key Signals
- Generous Prototype Area for Application Development
- LT and NT1 Software Development Platform
- Extensive User Manual

A.2.2 Hardware

- + 5 V Only Power Supply
- “Push Button” Activation of U–Interface from LT or NT1
- Standalone Operation for Bit Error Rate Testing
- Gated Data Clocks Provided for Bit Error Rate Testing
- Interfaces Directly to ADS302 IMP Evaluation Board
- Can Be Used as U– or S/T–Interface Terminal Development Tool
- On–Board 5 ppm LT Frequency Reference
- EIA–232 (V.28) Serial Port(s) for Terminal Interface
- Configurable for IDL2 and GCI Operation

A.2.3 Software

- Standalone or Terminal Operation
- Resident Firmware Monitor for User Control of Board
- Device Driver for Serial Control Port Interface
- Microcontroller Controlled or Automatic Activation/Deactivation
- Access to All Maintenance Channels
- MC68HC05 Assembly Language Source Code Available
- Enhanced Command Set from the MC145494EVK

A.3 BLOCK DIAGRAM

Figure A–2 is a basic functional block diagram of the MC145572EVK ISDN U–Interface Evaluation Kit. Note that the dashed line represents the physical and logical separation between the LT and the NT1 sides of the evaluation board. While the board is capable of activating “standalone”, the user may decide to use a single ASCII terminal to gain total control of the MC145572EVK capabilities. Or the user may choose to split the board, allowing the LT and NT1 portions to be physically located in separate areas.

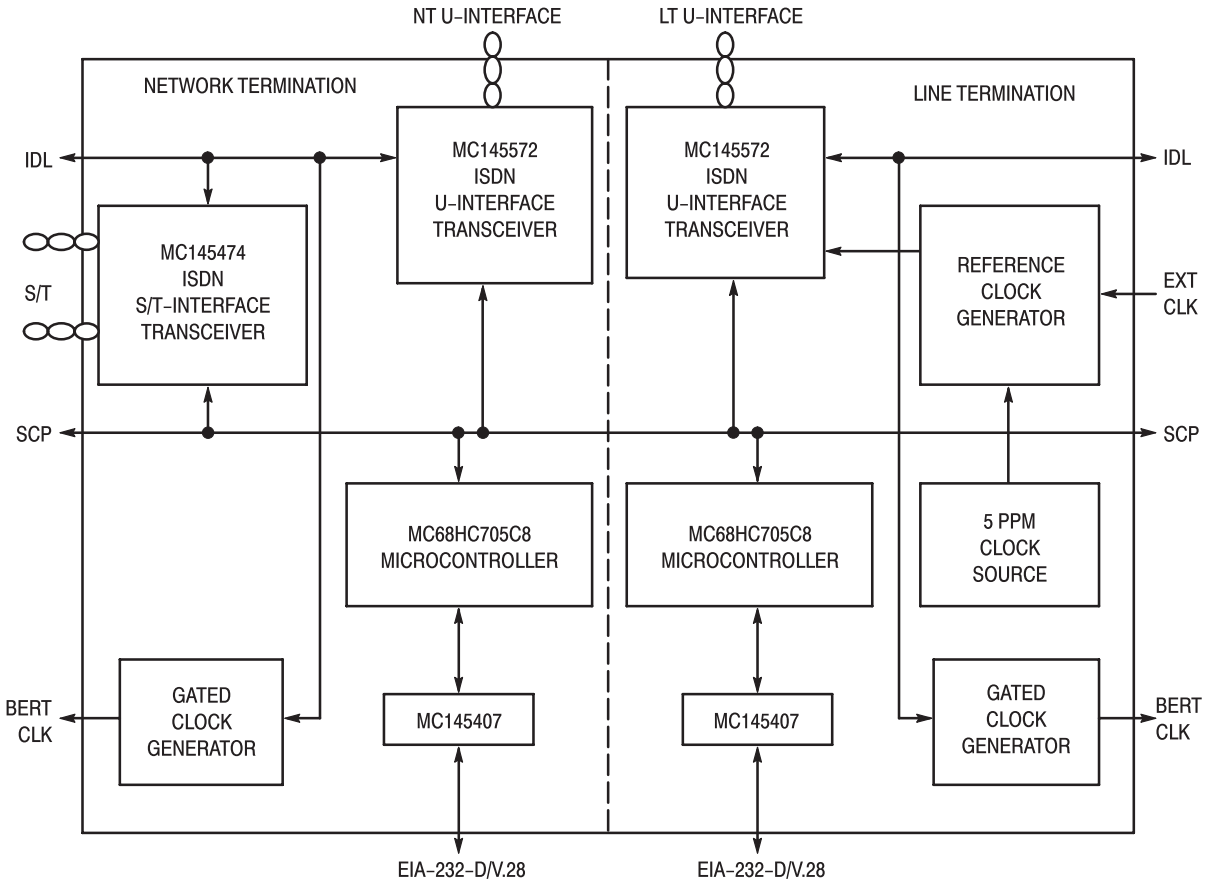


Figure A–2. MC145572EVK Functional Block Diagram

B

COMPONENT SOURCING

This information is provided to assist in sourcing the various parts used in the application of the MC145572 U–interface transceiver. The detailed specifications for these parts are available from the manufacturer and information presented here is only as current as the printing of this document. Contact your local Motorola representative or the Motorola factory applications staff for the latest updates on this information.

CAUTION

Motorola has conducted limited evaluation of third party components for use with the MC145572. This limited review suggests that the components included here appear to be suitable for applications using the MC145572. However, the evaluation did not include all specifications or parameters that may be applicable to particular designs, and the vendors included here represent only a partial list of component manufacturers. Motorola does not guarantee that these third party components will work in all applications. It is the responsibility of the equipment designer to verify that these components are suitable for their intended application.

B.1 TRANSFORMER SOURCES

Table B–1 lists sourcing information for the transformers used in the MC145572 line interface circuit.

Table B–1. U–Interface Transformer Vendors

Manufacturer	Part No.	Package Dimensions L x W x H	Fax No.	Contact/Phone No.
Midcom	671–7308	1.05″ x 0.92″ x 0.45″	(605) 886–4486	(605) 886–4385
Schott Corporation	671 46720	1.05″ x 0.92″ x 0.45″	(615) 885–0834	(615) 889–8800
APC	41018	19.6 mm x 25.1 mm x 13.2 mm	USA: (201) 368–1704 UK: (44) 1634–290–591	USA: (201) 368–1750 UK: (44) 1634–290–588
Pulse Engineering	PE 68628	1.05″ x 0.92″ x 0.45″	(619) 674–8262	(619) 674–8100
Valor Electronics	PT5062	0.82″ x 0.82″ x 0.675″	(619) 537–2525	(619) 537–2500

NOTES:
1. See Caution note above.
2. Part numbers subject to change.
3. APC also manufactures line interface modules.

B.2 2B1Q INTERFACE TRANSFORMER SPECIFICATION

A list of third party vendors and current qualification status appear in Table B–1. The transformer reference schematic appears in Figure B–1. The specifications in Table B–2 apply to the design of the U–interface transformer.

Any transformer manufactured to this specification must be verified for compliant transmission performance. It is also suggested that transformers manufactured for use in loop powered systems be required to remain within specification up to the maximum loop current which may be as high as 60 mA.

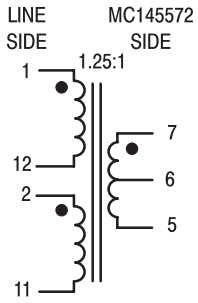


Figure B–1. Schematic Reference for U–Interface Transformer

Table B–2. Electrical Specification for the U–Interface Transformer, North American ISDN

Parameter	Pins Under Test	Min	Max	Unit	Notes
Operating Temperature		– 40	+ 85	°C	
Breakdown Voltage Vac (t = 1 s)	Each winding to all others and core	1500	—	Vac	1
Surge Voltage per Bellcore TR–NWT–001089 Issue 1, Table 4–2	Each winding to all others and core	2500	—	Vdc	1
DC Insulation Resistance (500 Vdc)	Each winding to all others and core	500	—	MΩ	
DC Resistance (T = 25°C) (Valhalla 4100)	(1 – 12) (2 – 11) (7 – 5)	1 1 1	6 6 9	Ω	2
Transformation Ratio (0.1 Vac, 20 kHz) (Waynekerr 3245)	(1 – 12):(2 – 11) (1 – 12:7 – 5)	0.99 0.615	1.01 0.635	—	
Inductance at 0.1 Vac, 10 kHz, and 0.0 Adc or 0.08 Adc (Waynekerr 3245)	(1 – 11) strap (2 – 12)	26.5	29.5	mH	3
Leakage Inductance at 0.01 Vac, 100 kHz	(7 – 5) strap (1 – 12) (2 – 11)	—	20.0	µH	
Total Harmonic Distortion at 80 mA Winding Current, 4 V pk–pk (Measured Between 500 Hz and 100 kHz)	(7 – 5):(1 – 11) strap (12 – 2)	—	– 55	dB	
Peak Winding Current	(1 – 11) strap (2 – 12)	20	—	mA dc	4

NOTES:
1. European countries may have significantly higher requirements.
2. DC winding resistance should be kept as low as possible since it can change by ± 25% over the temperature range of – 40 to + 85°C. If the dc winding resistance is low with respect to the value of the series resistors connected between the Tx pins and the transformer, a change in temperature will have a lower effect on the output pulse amplitude than if the transformer dc winding resistance is a relatively high value and the series resistors have a lower value.
3. Operating point on B–H curve should be well below the 'knee', i.e., no saturation.
4. Since European ISDN power feeding and pair gain currents are greater, the value should be increased to 60 mA for such applications.

B.3 MC145572 CRYSTAL SPECIFICATION

The MC145572 requires a pullable crystal because it has an on–chip VCXO. The same specification can be used for both the NT and LT mode. The specification assumes network timing tolerance of ± 5 ppm. The total pullability has been reduced from 360 ppm to 200 ppm.

The 200 ppm pullability spec has the following components:

2 x 50 ppm, total crystal tolerance	=	100 ppm
2 x 5 ppm, reference signal	=	10 ppm
Compensation for PCB and device capacitance	=	90 ppm
Total	=	200 ppm

B.3.1 Pullable Crystal Specification for ISDN and Network Applications

1. Operating frequency: 20.48 MHz
2. Crystal shunt capacitance: C_O = 7.0 pF
3. Uncertainty at rated C_L: ± 50 ppm over temperature, calibration, and 10–year aging
4. Equivalent series resistance: R_S ≤ 20 ohms @ 1 mW drive
5. Crystal pull range:
   a. ± 5 ppm signal — 200 ppm minimum pullability over a C_L range of 15 to 45 pF
   b. ± 32 ppm signal — 260 ppm minimum pullability over a C_L range of 15 to 45 pF
   c. ± 50 ppm signal — 300 ppm minimum pullability over a C_L range of 15 to 45 pF
6. Calibration load capacitance: 24 pF

NOTES:
1. – 40 to + 85°C required for transmission applications.
2. For room temperature, use 0 to 70°C.
3. Explanation of item 5, crystal pull range. Crystal pullability must be specified to allow the MC145572 to lock to either a received signal when operating in NT mode or lock to the 8 kHz FREQREF when operating in LT mode. The appropriate crystal pullability specification is dependent of the maximum expected signal or FREQREF tolerance in ppm. This will vary depending on national network and application requirements. For example in North America, receive signals from the network are expected to have a tolerance of less than 5 ppm. Hence, a crystal with either 200 or 260 ppm total pullability may be used. The ultimate choice is up to the equipment designer.

B.4 CRYSTAL SOURCES

Table B–3 lists sourcing information for the crystals used in the MC145572.

Table B–3. Crystal Vendors

Manufacturer	Contact Phone No.	Contact Fax No.
ECLIPTEK	(714) 433–1200	(714) 433–1234
Hy–Q International	(606) 283–5000	(606) 283–0883
SaRonix	(415) 856–6900	(415) 856–4732
Connor–Winfield	(708) 851–4722	(708) 851–5040
Precision Devices	(608) 831–4445	(608) 831–3343

NOTE: See Caution note on page B–1.

B.5 ISDN CALL CONTROL SOURCE CODE SUPPLIERS

The following vendors provide ISDN call control and applications source code. These suppliers support most of the various national and regional ISDN call control specifications on a world–wide basis. This list may not be complete.

Table B–4. ISDN Call Control Source Code Suppliers

Manufacturer	Street Address	Contact Phone No.	Contact Fax No.
telenetworks	625 Second Street Petaluma, CA 94952 U.S.A. e–mail: info@tn.com	(707) 773–4000	(707) 773–4099
Trillium Digital Systems, Inc.	2001 S. Barrington Ave., Suite 215 Los Angeles, CA 90025 U.S.A.	(310) 575–0172	(310) 575–0172
TeleSoft International, Inc.	4029 S. Capital of Texas Hwy. S., Suite 220 Austin, TX 78704 U.S.A. e–mail: sales@telesoft–intl.com	(512) 373–4224	(512) 447–1024
OMNITEL	31 rue Jean Rostand 91893 ORSAY CEDEX France	(331) 69 85 50 44	(331) 69 85 54 26
OMNITEL	3880 S. Bascom Ave., Suite 116 San Jose, CA 95124 U.S.A. e–mail: 102766.2525@compuserve.com	(408) 369–7733	(408) 369–7722
Link Technology	23 Crescent Drive Holland, PA 18966 e–mail: linkisdn@interramp.com	(215) 357–3354	(215) 357–1670
Co Systems	1263 Oakmead Parkway Sunnyvale, CA 94086 U.S.A. e–mail: info@cosystems.com	(408) 522–0505	(408) 790–9114

C
PRINTED CIRCUIT BOARD LAYOUT

C.1 INTRODUCTION

The MC145572 is manufactured using high speed CMOS VLSI process technology to implement the mixed signal processing functions required in the device. The U–interface transceiver has a high resolution sigma–delta ADC and a precision DAC, in addition to three high speed digital signal coprocessors. The fully differential analog circuit design techniques used for this device result in superior performance for the ADC, DAC, and Tx Driver sections. Special attention was given to the design of the MC145572 to reduce sensitivity to noise, including power supply rejection and susceptibility to radio frequency noise. This special attention to circuit design, results in an ADC with greater than 84 dB dynamic range on the same monolithic chip as the digital signal coprocessors clocking at 10.24 MHz, all of which operates on a single 5–V power supply. This device was designed to ease the task of PCB layout, but due to the wide analog dynamic range and high digital clock rate, special care should be taken during PCB layout to assure optimum transmission performance.

NOTE

When laying out the PCB, do not run any digital signals through the line interface region of the board. Switching noise from the digital signals can be coupled into the line interface and reduce performance, especially on long loops. Wire wrap is not recommended for prototyping.

C.2 PRINTED CIRCUIT BOARD MOUNTING

The device should be soldered to the PC board for production manufacturing. If the device is to be used in a socket, it should be placed in a low parasitic pin capacitance socket of 1.5 pF or less.

C.3 POWER SUPPLY, GROUND, AND NOISE CONSIDERATIONS

This device is often used in digital switching equipment applications which require plugging the PC board into a rack with power applied. This is referred to as “hot–rack insertion”. In these applications, care should be taken to limit the voltage on any pin from going positive relative to the V_{DD} pins, or negative relative to the V_{SS} pins. One method to accomplish this is to extend the ground and power contacts of the PCB connector so that power is applied prior to any other pins having voltage applied. The device has input protection on all pins and may source or sink a limited amount of current without damage. See Section 10.1, **Absolute Maximum Ratings,** for more information concerning the current into or out of the device pins. Current limiting may be accomplished by series resistors between the signal pins and the connector contacts.

The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and coupling digital signals into the analog signals. The best PCB layout methods to prevent noise–induced problems are:

1. Keep digital signals as far away from analog signals as possible.
2. Use short, low inductance traces for the analog circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
3. Use short, low inductance traces for digital circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
4. Bypass capacitors should be connected between the V_{DD} and V_{SS} pairs with minimal trace length. These capacitors help supply the instantaneous currents of the digital circuitry, in addition to decoupling the noise that may be generated by other sections of the device or other circuitry on the power supply.

5. Use short, wide, low inductance traces to connect all of the V_{SS} ground pins together and, with one trace, connect all of the V_{SS} ground pins to the power supply ground. Depending on the application, a double sided PCB with a V_{SS} ground plane under the device connecting all of the digital and analog V_{SS} pins together would be a good grounding method. A multi–layer PCB with a ground plane connecting all of the digital and analog V_{SS} pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high speed digital current spikes. Suppressing these voltage spikes on the integrated circuit is the reason for multiple V_{SS} ground leads.
6. Use short, wide, low inductance traces to connect all of the V_{DD} power supply pins together and, with one trace, connect all of the V_{DD} power supply pins to the 5–V power supply. Depending on the application, a double sided PCB with V_{DD} bypass capacitors to the V_{SS} ground plane under the device, as described in item 5 above, may complete the low impedance coupling for the power supply. For a multi–layer PCB with a power plane, connecting all of the digital and analog V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5–V V_{DD} power circuit are essentially the same as for the ground circuit.
7. Motorola recommends that a four layer board be used. It is possible to use a two layer board but special care must be taken. See Figure C–1.
8. The 20.48 MHz crystal must be located as close as possible to the MC145572 package. This is required to minimize parasitic capacitances between crystal traces and ground.

Figure C–1 shows a suggested board layout for a two layer board. This drawing is not done to scale. Trace vias are shown. Depending on the application, other pins may need to be connected to V_{DD} or V_{SS}. All bypass capacitors should be located as close as possible to the V_{SS}/V_{DD} pins. The suggested layout shows the power feed to the MC145572 coming from a common point. This is important in a two layer implementation. The 10 μF electrolytic capacitor is recommended to filter out any ripple or noise that may be on the board in a two layer application. Even though the MC145572 has very high power supply rejection, good power supply decoupling is recommended.

If a four layer board with full power and ground planes is used, the V_{DD} and V_{SS} pins can be connected directly to the appropriate plane by vias.

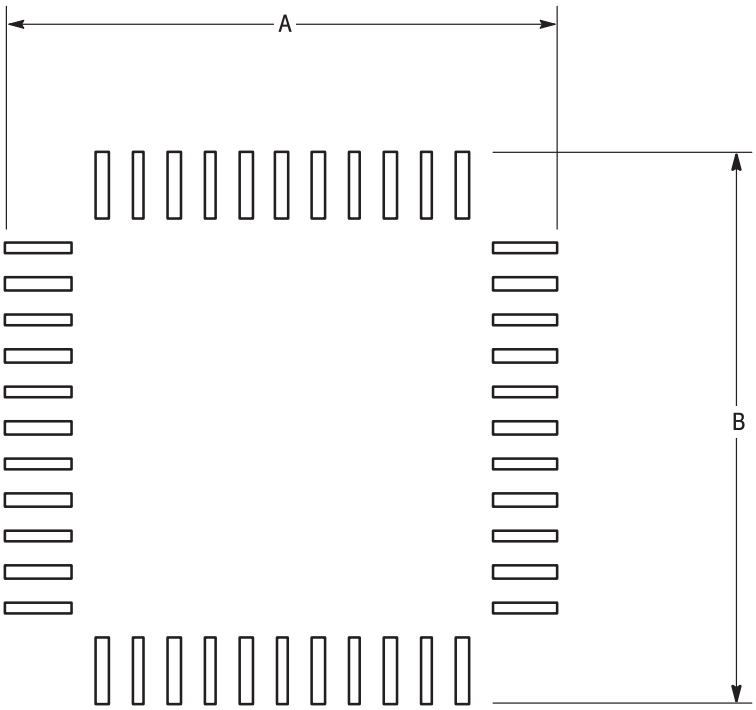
C.4 OSCILLATOR LAYOUT GUIDELINES

All traces must be as short as possible to reduce stray capacitance and inductance. The traces to $XTAL_{in}$ and $XTAL_{out}$ must be kept as short as possible with minimal width to keep stray capacitance less than 1 pF. Other digital signals should not be routed near the crystal traces. Any passive components for the oscillator or PLL should have short leads and should be soldered to the PC board. Wherever possible the layout should be symmetrical, so the stray capacitances from each pin of the crystal to ground are equal.

When a four layer board is used, do not route ground or power plane material underneath the 20.48 MHz crystal oscillator circuitry. This is to minimize parasitic capacitances between the 20.480 MHz oscillator traces and the power or ground plane. Excessive parasitic capacitance between the traces and power/ground planes decreases the pull range of the 20.48 MHz oscillator.

C.5 2B1Q INTERFACE GUIDELINES

The line interface into and out of the device is differential, implying symmetry. It is recommended that the layout of the 2B1Q interface be as symmetrical as possible to avoid any imbalances to this circuit. Do not run any digital traces through the line interface region of the printed circuit board.



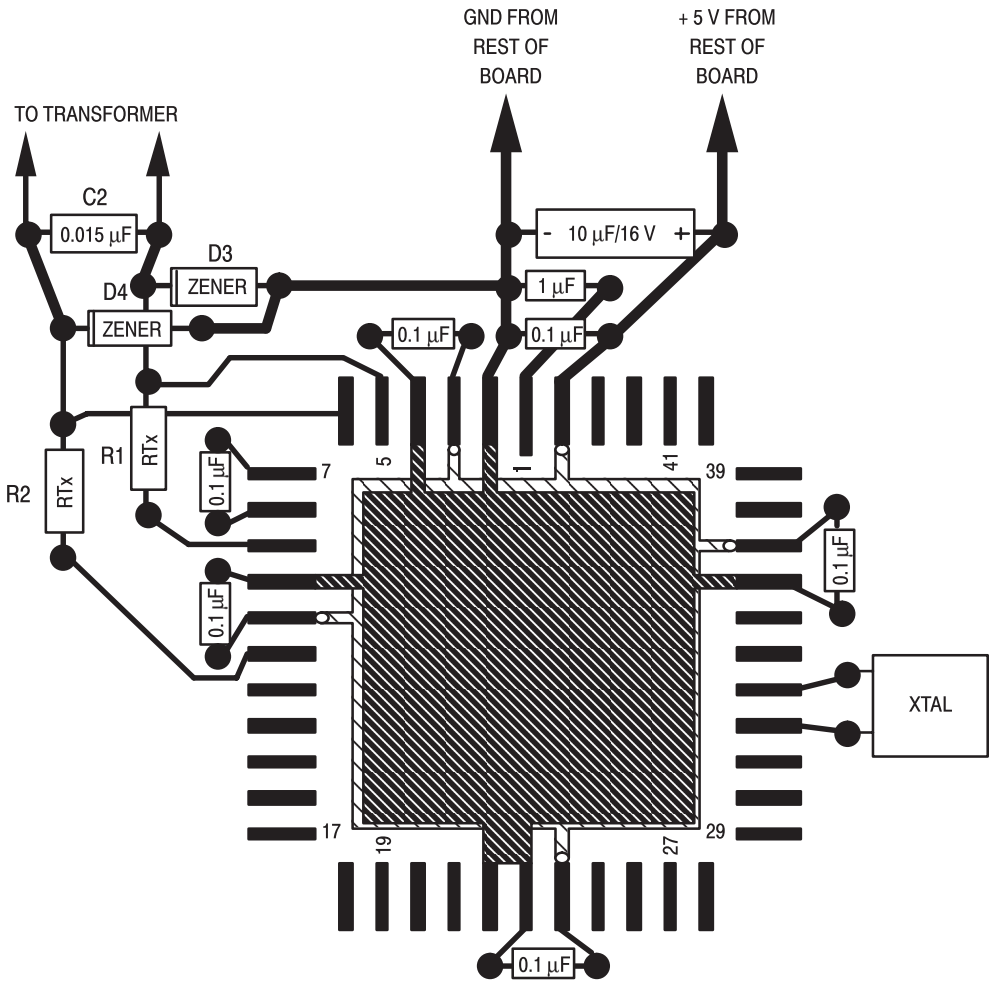
NOTE: Dimensions given in millimeters are hard metric numbers and PCB pad designs must be done in metric. Likewise, dimensions given in inches must be designed in inches. This is especially important on conversions involving lead pitch where a small fractional error, repeated many times across the width of a package, will make it impossible to align all leads to pads.

Package	Lead Pitch	Pad Size	Dimension A	Dimension B	Device	Units
44 PLCC	0.050	0.025 x 0.075	0.705	0.705	MC145572FN	inches
44 TQFP	0.8	0.5 x 1.6	13	13	MC145572PB	mm

Figure C–1. MC145572 Printed Circuit Board Footprint Dimensions

C.6 PACKAGE FOOTPRINTS FOR PRINTED CIRCUIT BOARDS

Figure C–2 gives suggestions for a two layer printed circuit board layout of surface mount packages used for the MC145572FN package.



NOTES:
1. Figure is shown for a 44–lead PLCC package.
2. Figures 5–38(a) and 5–38(b) are used for reference.

Figure C–2. MC145572 Suggested PCB Layout

D

EYE PATTERN GENERATOR

D.1 INTRODUCTION

The MC145572 can provide the recovered eye pattern on a received baud–by–baud basis as a serial digital word once every 12.5 μs. Some applications may use this feature for monitoring performance. This appendix describes a circuit to receive the eye pattern word and convert it to an analog voltage for display on an oscilloscope.

This appendix includes the schematics and PALASM™ 2 programmable logic equations to implement two versions of an eye pattern generator. One design requires manual scaling to the magnitude of the eye pattern data, while the other design automatically scales to optimize the limited dynamic range of the DAC. The eye pattern generator takes the data available on the EYEDATA pin and the clocking from the SYSCLK pin and generates an analog eye pattern for display purposes. Note that BR14(b0) must be set to a 1 to enable the EYEDATA and SYSCLK outputs.

D.2 DISCUSSION

The eye pattern data output from the MC145572 consists of the received 2B1Q quats after the echo cancelling and DFE functions have been performed on the signal available at the RxP and RxN pins. The eye pattern data is output in digital form on the EYEDATA pin and is 19 bits long. It is in sign extended two's complement form. The eye pattern data generators described here use an 8–bit DAC (this is sufficient for acceptable display on an oscilloscope) to display the most significant 8 bits of data including the first sign bit, but not extended sign bits or less significant bits. The 8 bits are shifted into an 8–bit serial–to–parallel converter and are then latched into an Analog Device's AD557 DAC. When the resulting 8–bit window is correctly placed over the 19–bit eye data word, a full scale (approximately 1 or 2 V peak–to–peak) eye pattern signal is output from the AD557 clearly showing the 2B1Q quats. See Figure D–1 for an example of the 8–bit window positioned over a portion of the 19–bit eye data word. In this example, D16 happens to be the sign bit.

Two circuits are shown for decoding the eye pattern data available on the EYEDATA pin. The first method provides for manual positioning of the 8–bit DAC data window over the 19–bit eye data word. The manual positioning schematic is shown in Figure D–2. The second method provides for automatic or manual positioning of the 8–bit DAC data window over the 19–bit eye data word. The automatic positioning schematic is shown in Figure D–3. Whenever the manual method is used, the DIP switches can be changed to correctly position the 8–bit data window. Manual positioning capability is provided with the automatic positioning circuit, since there may be some conditions in which the automatic positioner will not stabilize. DIP switches are shown but any convenient binary encoder may be used.

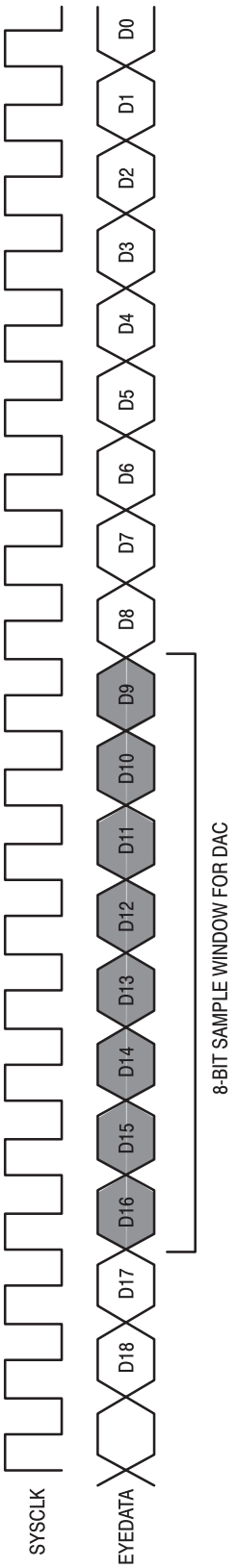


Figure D–1. 8–Bit Sample Window Positioned Over Bits D16:D9

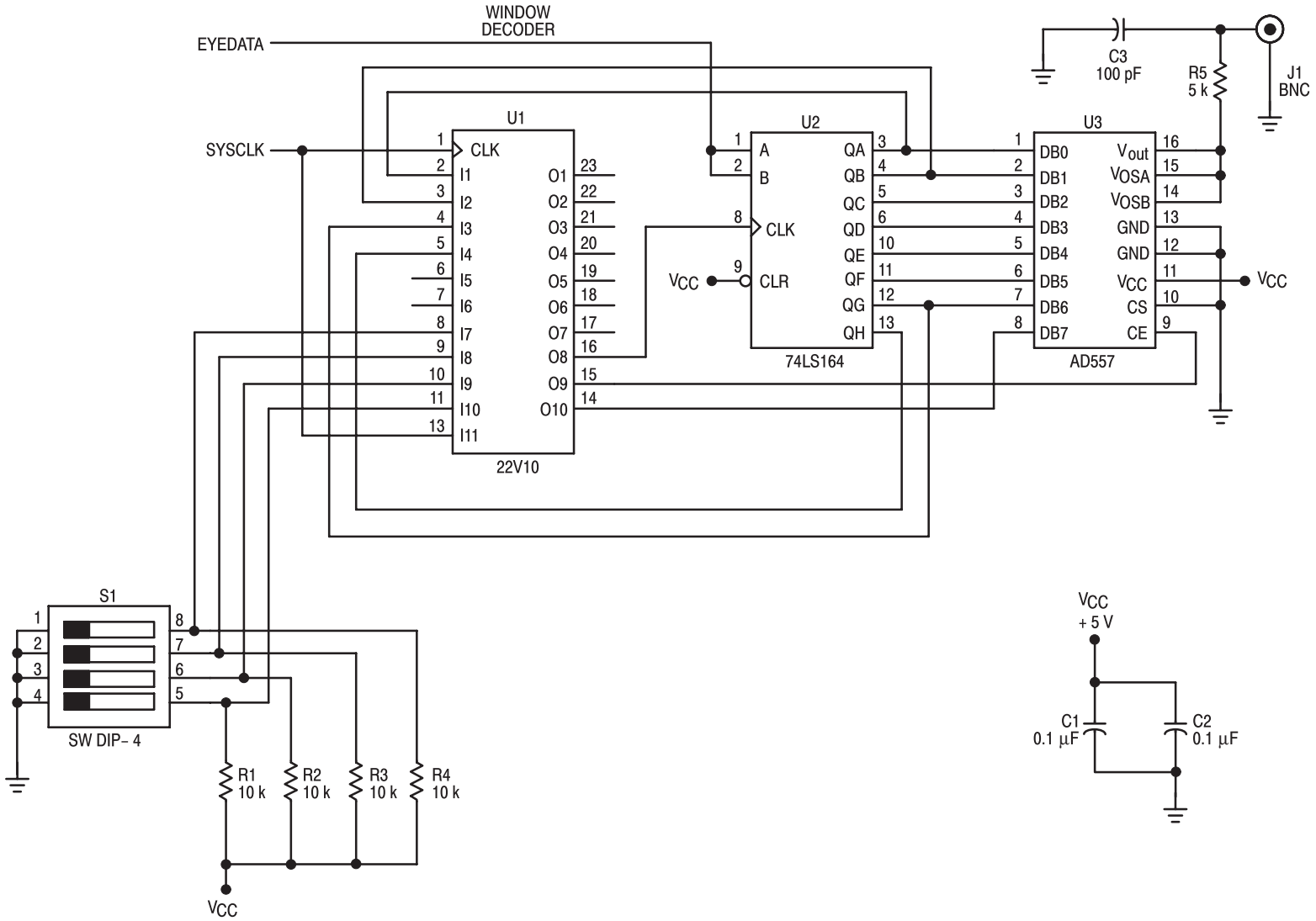


Figure D–2. Manual Eye Pattern Decoder

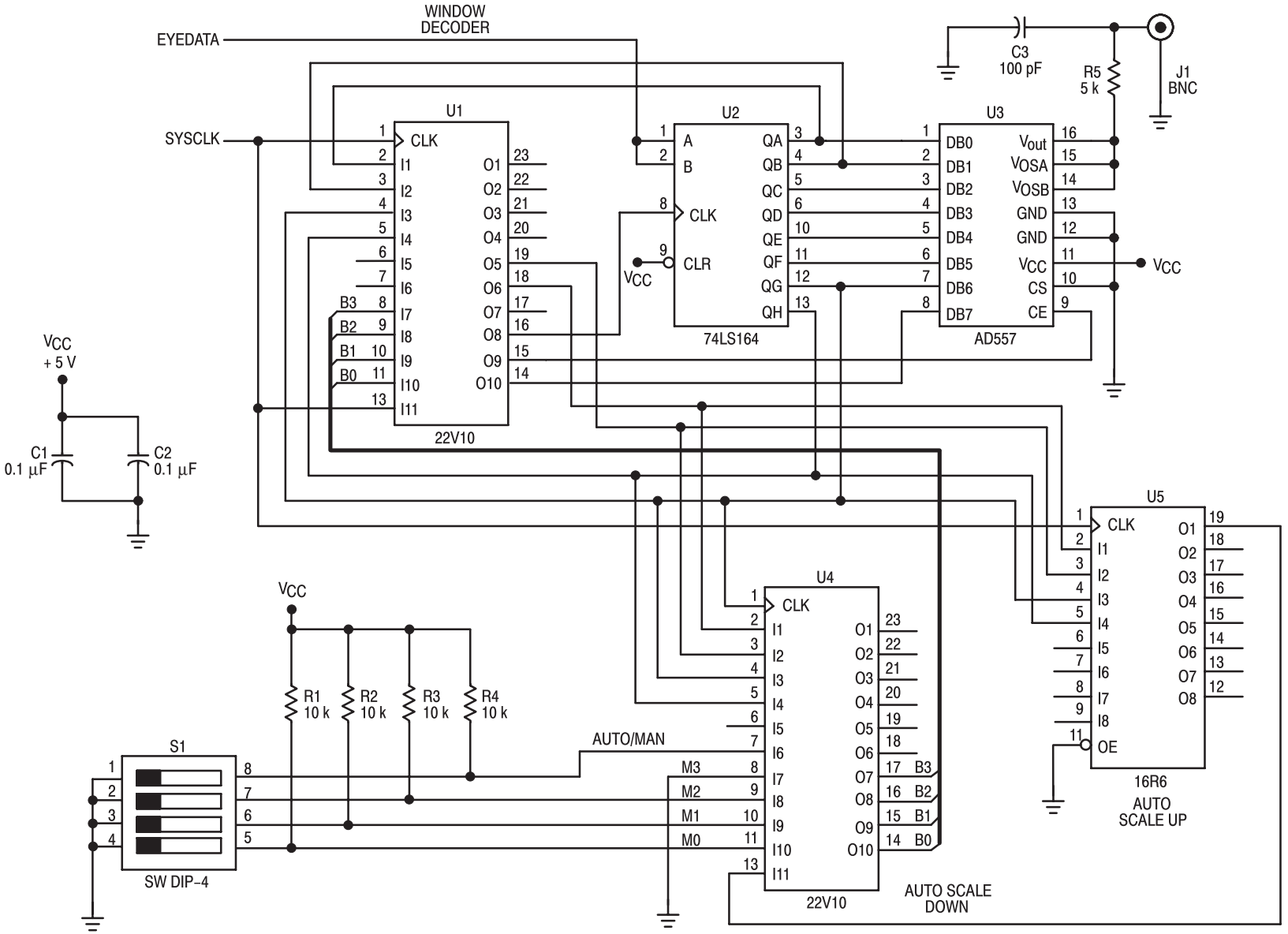


Figure D–3. Manual and Automatic Eye Pattern Decoder

D.3 WINDOW DECODER LOGIC EQUATIONS

The window decoder is used in both manual and automatic circuits. It extracts the 8–bit data word to be displayed and provides control signals to the 74LS164 serial–to–parallel converter and to the AD557.

```
TITLE  WINDOW_DECODER      ; U1 IN THE SCHEMATIC
PATTERN      WINDEC.PL
REVISION     VER_1.0
COMPANY      MOTOROLA
CHIP   WIN_DECODER   PAL22V10
;PINS
;1     2      3      4      5      6      7      8      9      10     11     12
CLK    NC     SQ1    NC     SQ7    NC     NC     B3     B2     B1     B0     GND
;PINS
;13    14     15     16     17     18     19     20     21     22     23     24
ICLK   NSQ7   /ADC   SCLK   /ENA   LESS   Q4     Q3     Q2     Q1     Q0     VCC
EQUATIONS
       NSQ7   = /SQ7
       ADC    = /Q1 * Q2 * Q3 * Q4
                     + /Q0 * Q2 * Q3 * Q4
       SCLK   = /ICLK * LESS
                + /ICLK * /Q4
                + /ICLK *  Q0 * Q1 * Q2 * Q3
       /ENA : = /SQ1  * /ENA
              +  Q0 *  Q1 *  Q2 *  Q3 * Q4
       LESS   =  Q4 * /Q3 *  B3
              +  Q4 * /Q3 * /B3 * /Q2 *  B2
              +  Q4 *  Q3 *  B3 * /Q2 *  B2
              +  Q4 * /Q3 * /B3 * /Q2 * /B2 * /Q1 *  B1
              +  Q4 * /Q3 * /B3 *  Q2 *  B2 * /Q1 *  B1
              +  Q4 *  Q3 *  B3 * /Q2 * /B2 * /Q1 *  B1
              +  Q4 *  Q3 *  B3 *  Q2 *  B2 * /Q1 *  B1
              +  Q4 * /Q3 * /B3 * /Q2 * /B2 * /Q1 * /B1 * /Q0 * B0
              +  Q4 * /Q3 * /B3 * /Q2 * /B2 *  Q1 *  B1 * /Q0 * B0
              +  Q4 * /Q3 * /B3 *  Q2 *  B2 * /Q1 * /B1 * /Q0 * B0
              +  Q4 * /Q3 * /B3 *  Q2 *  B2 *  Q1 *  B1 * /Q0 * B0
              +  Q4 *  Q3 *  B3 * /Q2 * /B2 * /Q1 * /B1 * /Q0 * B0
              +  Q4 *  Q3 *  B3 * /Q2 * /B2 *  Q1 *  B1 * /Q0 * B0
              +  Q4 *  Q3 *  B3 *  Q2 *  B2 * /Q1 * /B1 * /Q0 * B0
              +  Q4 *  Q3 *  B3 *  Q2 *  B2 *  Q1 *  B1 * /Q0 * B0
       Q0   : = ENA * /Q0
       Q1   : = ENA *  Q0 * /Q1
              + ENA * /Q0 *  Q1
       Q2   : = ENA *  Q0 *  Q1 * /Q2
              + ENA * /Q0 *  Q2
              + ENA * /Q1 *  Q2
       Q3   : = ENA *  Q0 *  Q1 * Q2 * /Q3
              + ENA * /Q0 *  Q3
              + ENA * /Q1 *  Q3
              + ENA * /Q2 *  Q3
       Q4   : = ENA *  Q0 *  Q1 * Q2 *  Q3 * /Q4
              + ENA * /Q0 *  Q4
              + ENA * /Q1 *  Q4
              + ENA * /Q2 *  Q4
              + ENA * /Q3 *  Q4
```

D.4 AUTOMATIC SCALE UP COUNTER LOGIC EQUATIONS

These equations shift the position of the 8–bit data window to the left when changes are detected in the most significant data bit.

```
TITLE         AUTO_SCALE_UP ; U5 IN THE SCHEMATIC
REVISION      VER_1.0
COMPANY       MOTOROLA
SCALE_UP      PAL16R6
;PINS
;1     2      3      4      5      6      7      8      9      10
CLK    LESS   WQ4    SQ6    SQ7    NC     NC     NC     NC     GND
;PINS
;11    12     13     14     15     16     17     18     19     20
NC     /UP    /QUP   /Q4    /Q3    /Q2    /Q1    /Q0    /CPU   VCC
STRING  RESET1  ' SQ6 * /SQ7 * WQ4 * /LESS * /QUP '
STRING  RESET2  ' /SQ6 * SQ7 * WQ4 * /LESS * /QUP '
EQUATIONS
       UP     = SQ6 *  SQ7 *  WQ4 * /LESS * /QUP
              + /SQ6 * /SQ7 *  WQ4 * /LESS * /QUP
       QUP  : =  WQ4 * /LESS
              +  WQ4 *  QUP
       CPU    =  UP * /Q0 * /Q1 * /Q2 * /Q3 * /Q4
       Q0   : = /Q0 *  UP
              +  Q0 * /UP
              +  RESET1 + RESET2
       Q1   : = /Q0 * /Q1 * UP
              +  Q0 *  Q1
              +  Q1 * /UP
              +  RESET1 + RESET2
       Q2   : = /Q0 * /Q1 * /Q2 * UP
              +  Q0 *  Q2
              +  Q1 *  Q2
              +  Q2 * /UP
              +  RESET1 + RESET2
       Q3   : = /Q0 * /Q1 * /Q2 * /Q3 * UP
              +  Q0 *  Q3
              +  Q1 *  Q3
              +  Q2 *  Q3
              +  Q3 * /UP
              +  RESET1 + RESET2
       Q4   : = /Q0 * /Q1 * /Q2 * /Q3 * /Q4 * UP
              +  Q0 *  Q4
              +  Q1 *  Q4
              +  Q2 *  Q4
              +  Q3 *  Q4
              +  Q4 * /UP
              +  RESET1 + RESET2
```

D.5 AUTOMATIC SCALE DOWN COUNTER LOGIC EQUATIONS

These equations shift the position of the 8–bit data window to the right when changes are not detected in the most significant data bits.

```
TITLE         AUTO_SCALE_DOWN     ; U4 IN THE SCHEMATIC
REVISION      VER_1.0
COMPANY       MOTOROLA
CHIP          SCALE_DOWN    PAL22V10
;PINS
;1     2      3      4      5      6      7      8      9      10     11     12
CLK    LESS   WQ4    SQ6    SQ7    NC     MAN    S3     S2     S1     S0     GND
;PINS
;13    14     15     16     17     18     19     20     21     22     23     24
/CPU   B0     B1     B2     B3     /Q2    /Q1    /Q0    /QDN   /DN    /CPD   VCC
STRING        RESET1  ' /SQ6 *  SQ7 * /LESS * WQ4 * /QDN '
              RESET2  '  SQ6 * /SQ7 * /LESS * WQ4 * /QDN '
EQUATIONS
       DN     = /SQ6 *  SQ7 * LESS * WQ4 * /QDN
              +  SQ6 * /SQ7 * LESS * WQ4 * /QDN
       QDN  : =  DN
              + /LESS * WQ4
              +  QDN  * WQ4
       CPD    =  DN * /Q0 * /Q1 * /Q2
       Q0   : = /Q0 *  DN
              +  Q0 * /DN
              +  RESET1 + RESET2
       Q1   : = /Q0 * /Q1 * DN
              +  Q0 *  Q1
              +  Q1 * /DN
              +  RESET1 + RESET2
       Q2   : = /Q0 * /Q1 * /Q2 * DN
              +  Q0 *  Q2
              +  Q1 *  Q2
              +  Q2 * /DN
              +  RESET1 + RESET2
       B0   : =  MAN * S0
              + /MAN *  CPU * /B0
              + /MAN *  CPD * /B0
              + /MAN * /CPU * /CPD * B0
       B1   : =  MAN *  S1
              + /MAN *  CPU *  B0  * /B1
              + /MAN *  CPD * /B0  * /B1
              + /MAN * /CPU * /CPD *  B1
              + /MAN *  CPU * /B0  *  B1
              + /MAN *  CPD *  B0  *  B1
       B2   : =  MAN *  S2
              + /MAN *  CPU *  B0  *  B1 * /B2
              + /MAN *  CPD * /B0  * /B1 * /B2
              + /MAN * /CPU * /CPD *  B2
              + /MAN *  CPU * /B0  *  B2
              + /MAN *  CPU * /B1  *  B2
              + /MAN *  CPD *  B0  *  B2
              + /MAN *  CPD *  B1  *  B2
       B3   :=  MAN *  S3
              + /MAN *  CPU *  B0  *  B1 *  B2 * /B3
              + /MAN *  CPD * /B0  * /B1 * /B2 * /B3
              + /MAN * /CPU * /CPD *  B3
              + /MAN *  CPU * /B0  *  B3
              + /MAN *  CPU * /B1  *  B3
              + /MAN *  CPU * /B2  *  B3
              + /MAN *  CPD *  B0  *  B3
              + /MAN *  CPD *  B1  *  B3
              + /MAN *  CPD *  B2  *  B3
```

E

LINE INTERFACE CIRCUIT COMPONENT VALUE CALCULATIONS

E.1 INTRODUCTION

The intent of this appendix is to provide information about the MC145572 2B1Q interface circuit (excluding protection, dc termination, etc.) to compute optimal component values for line interface and transformer solutions. It also provides some basic explanation regarding the function of each of the components in the 2B1Q interface circuit.

E.2 CALCULATION OF TRANSMIT SERIES RESISTORS

The transmit series resistor values, R_X, depend on the amount of dc winding resistance of the transformer. The values of these resistors also depend on the impedance of the 1 μF dc blocking capacitor, C_b. Any resistors added to the line side of the transformer for primary circuit protection may be added to the dc winding resistance of the line side windings of the transformer. Portions of the line interface circuit are internal to the MC145572. The entire line interface circuit model is shown in Figure E–1.

The total transmit circuit model is shown in Figure E–2. Due to the duplexer nature of the line interface circuit, R_XP and R_XN are at virtual signal ground for transmitted signals. Thus, each R_f appears in parallel with each R_g (see Figure E–2), but since R_g is so low, R_f can be ignored. The output impedance of the transmit drivers has been included in this model, but will be subsequently ignored due to its insignificant nature.

The transmit model is simplified to include the reflected impedances from the line side of the transformer. The output impedances of the transmit drivers are omitted here. This is shown in Figure E–3.

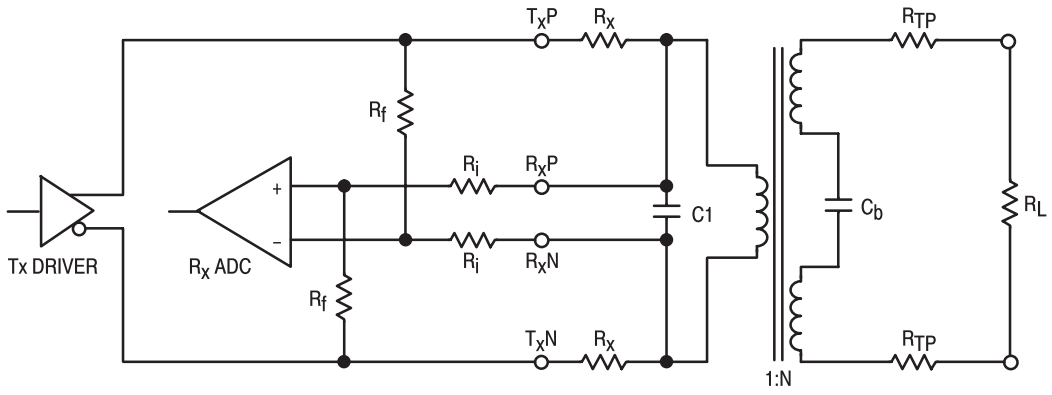


Figure E–1. Line Interface Circuit Model

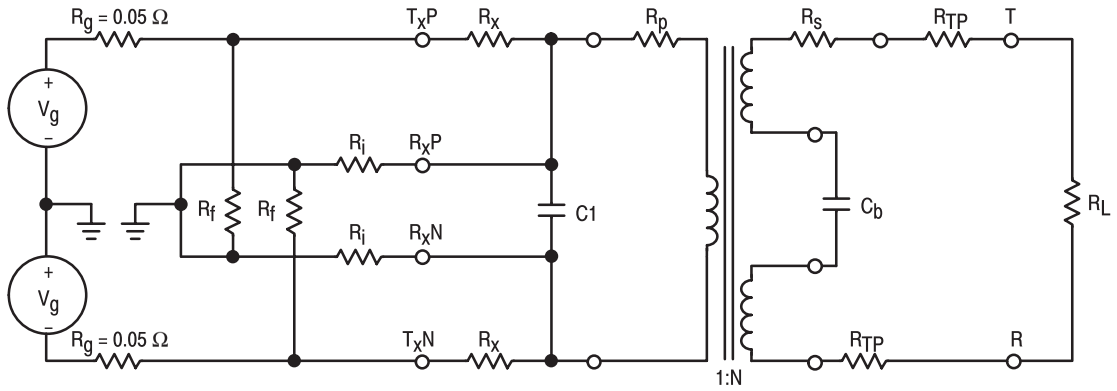


Figure E–2. Transmit Circuit Model

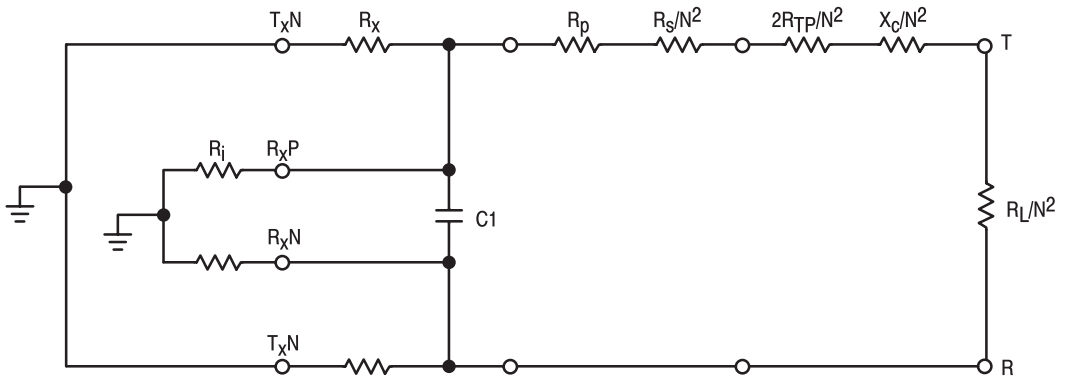


Figure E–3. Transformer Model

The impedance looking into the secondary side of the transformer must equal $R_L/(N^2)$ in order to terminate the line.

$$(2R_X * 2R_i) / (2R_i + 2R_X) + R_p + (R_S + X_C + 2 * R_{TP}) / (N^2) = R_L / (N^2) \quad (1)$$

Rearranging and solving for R_X gives:

$$R_X = R_i*(R_L - N^2*R_p - 2*R_{TP} - R_S - X_C) / (X_C + R_S + N^2*R_p + 2*N^2*R_i + 2*R_{TP} - R_L) \quad (2)$$

Substituting in values,

for a prototype transformer: $R_p = 7.9\ \Omega$ and $R_S = 8.2\ \Omega$

$$X_C = 1 / (j * 2 * PI * 40000 * 1E - 06) = - j4\ \Omega \text{ at } 40\ kHz$$

$$R_i = 5000\ \Omega$$

$$R_{TP} = 5\ \Omega$$

we get:

$$R_X = 5000 * (135 - 7.9 * 1.25^2 - 8.2 - 2 * 5 + j4) / (- j4 + 8.2 + 7.9 * 1.25^2 + 2 * 5000 * 1.25^2 + 2 * 5 - 135)$$

$$= 5000 * (104.5 + j4) / (15520.5 - j4)$$

$$= 5000 * 104.6 < 2.19° / (15520.5 < - 0.01°)$$

$$= 33.7\ \Omega < 2.20°$$

Since the reactive component is so small, having an angle of only 2.20°, it can be ignored when doing this analysis.

The equation for calculating R_X can be reduced to:

$$R_X = R_i*(R_L - N^2*R_p - 2*R_{TP} - R_S) / (R_S + N^2*R_p + 2*N^2*R_i + 2*R_{TP} - R_L) \quad (3)$$

Substituting in values gives:

$$R_X = 5000*(135 - 7.9*1.25^2 - 8.2 - 2*5) / (8.2 + 7.9*1.25^2 + 2*5000*1.25^2 + 2*5 - 135)$$

$$= 33.65\ \Omega$$

$$= 33.7\ \Omega$$

E.3 CALCULATION OF TRANSMIT NOISE FILTER CAPACITOR

Once the transmit series resistor values have been calculated, the transmit noise filter capacitor can be calculated for a 160 kHz cutoff frequency. This capacitor in conjunction with the transmit series resistors acts as a low pass filter to remove the high frequency switching noise in the output signal of the MC145572 TxP and TxN pins.

$$C1 = 1 / [2 * (2 * PI * f * R_X)] \quad (4)$$

$$C1 = 1 / [2 * (2 * PI * 160000 * 33.7)]$$

$$C1 = 0.015\ \mu F$$

The nearest commercial value can be used.

The analysis yields the following line interface circuit (see Figure E–4).

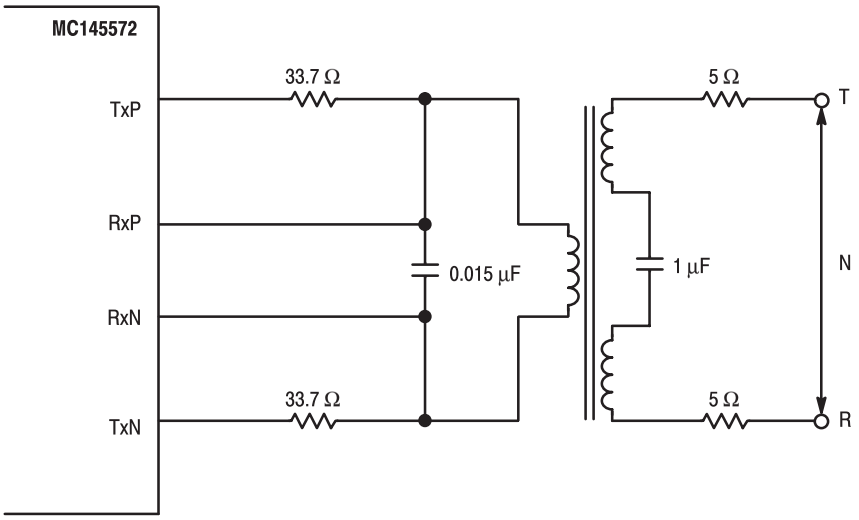


Figure E–4. Calculated Line Interface Circuit

E.4 2B1Q LINE INTERFACE

Figure E–5 shows the suggested 2B1Q interface networks for connection to the U–interface. The component specifications are shown in Table E–5. Sources and specifications for the 2B1Q line interface transformer can be found in **Appendix B**.

There are two basic topologies for the 2B1Q line interface. The first topology does not have resistors between the transformer and Tip, and the transformer and Ring. The second topology does have these resistors. By using positive temperature coefficient resistors on the line side of the transformer, electrical safety design requirements may be more easily implemented. A positive temperature coefficient resistor greatly increases its resistance value when it heats, up due to the application of external voltages across Tip and Ring. Effectively, the positive temperature coefficient resistor creates a high impedance, thereby limiting current flow between Tip and Ring when the protection diodes turn on.

NOTE

Motorola continues to qualify several third party sources for the 2B1Q line interface transformer. Contact your local Motorola representative or Motorola factory applications staff for the latest information regarding component sourcing.

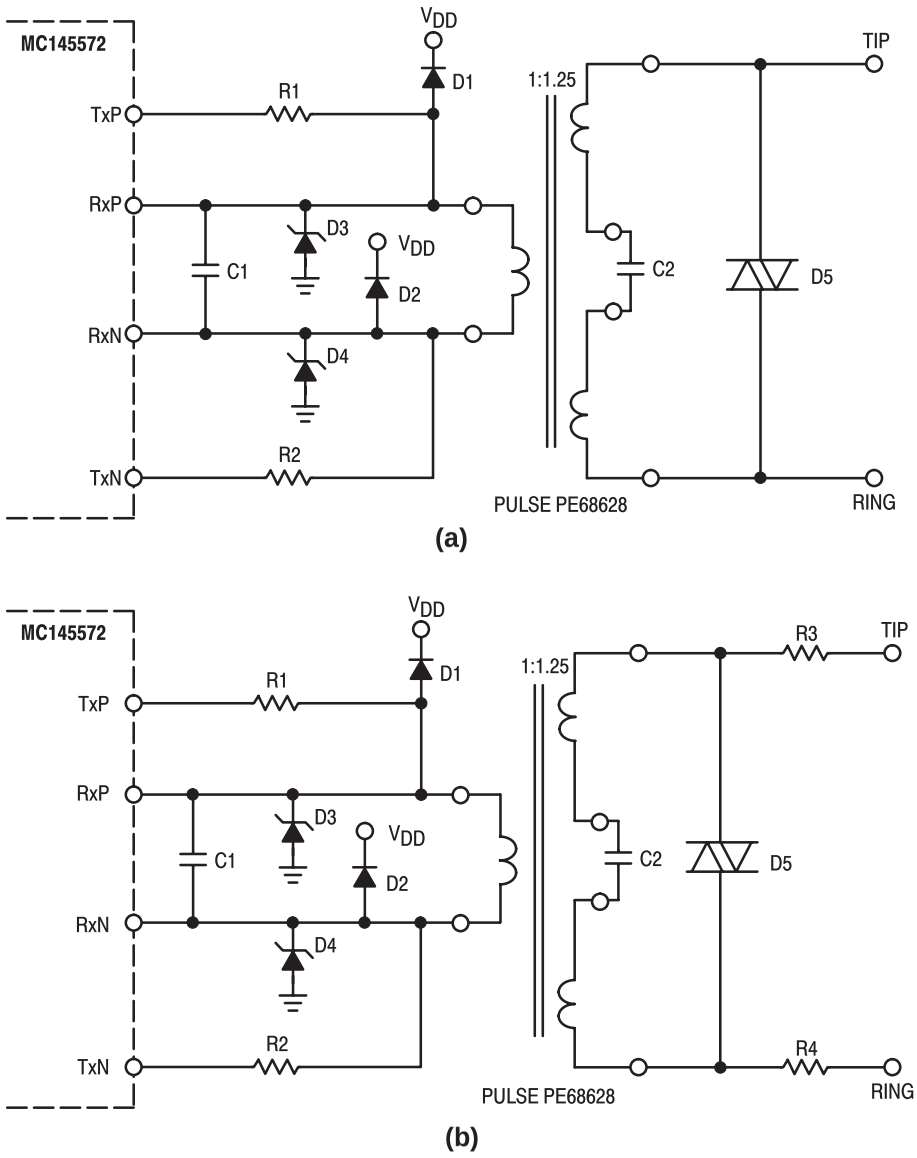


Figure E–5. Typical 2B1Q Line Interface Schematic

Table E–5. 2B1Q Line Interface Component Values

Component	Description (Figure E–5a)	Description (Figure E–5b)
C1	0.012 μF, 16 V, 10%, ceramic NPO, polystyrene, or polypropylene capacitor. See **Appendix E** for how to calculate this value.	0.012 μF, 16 V, 10%, ceramic NPO, ceramic COG, polystyrene, or polypropylene capacitor. See **Appendix E** for how to calculate this value.
C2	1.0 μF, 200 V, 10%, low distortion capacitor	1.0 μF, 200 V, 10%, low distortion capacitor
R1, R2	35 Ω, 1%, metal film or other high quality low distortion resistor. See **Appendix E** for how to calculate this value.	32 Ω, 1%, metal film or other high quality low distortion resistor. See **Appendix E** for how to calculate this value.
R3, R4	Not Used	7.5 Ω, positive temperature coefficient resistor, polyswitch TR600–150.
D1, D2	MMBD7000 LT1	MMBD7000 LT1
D3, D4	IN5232B 5.6 V Zener	IN5232B 5.6 V Zener
D5	Transient voltage suppressor, TECCOR P1300EA70	Transient voltage suppressor, TECCOR P1300EA70
T1	Pulse Engineering PE68628	Pulse Engineering PE68628

NOTES:
1. Pulse transformer, 1:1.25 turns ratio. See **Appendix B** for sourcing and specification information. Dielectric isolation must accept highest power cross voltage and highest lightning surge test voltage to be applied to Tip and Ring.
2. Pulse transformers are available from several manufacturers.
3. Diodes D1, D2, D3, and D4 can be MMBD7000 LT1. It is not required that D3, D4 be zener diodes.
4. 22 Ω, 5% resistors can be connected at RxN and RxP for additional surge protection, if desired.

F
APPLICATIONS

F.1 INTRODUCTION

This appendix shows suggested partial schematics for several MC145572 applications.

- Figure F–1 shows an example of how to connect two MC145572 U–interface transceivers as a repeater.
- Figure F–2 shows how an MC68HC05 MCU can be connected to the MC145572 and MC145474 in an NT1 application.
- Figure F–3 details the MC68302 serial interface connections to the MC145572 and MC14LC5480 for an ISDN U–interface terminal.
- Figure F–4 shows an ISDN smart NT1 application with the MC145572 and MC145574 in NT terminal mode.
- Figures F–5 and F–6 show two different remote access multi–line configurations.
- Figure F–7 gives an example of a multi–line U line card.

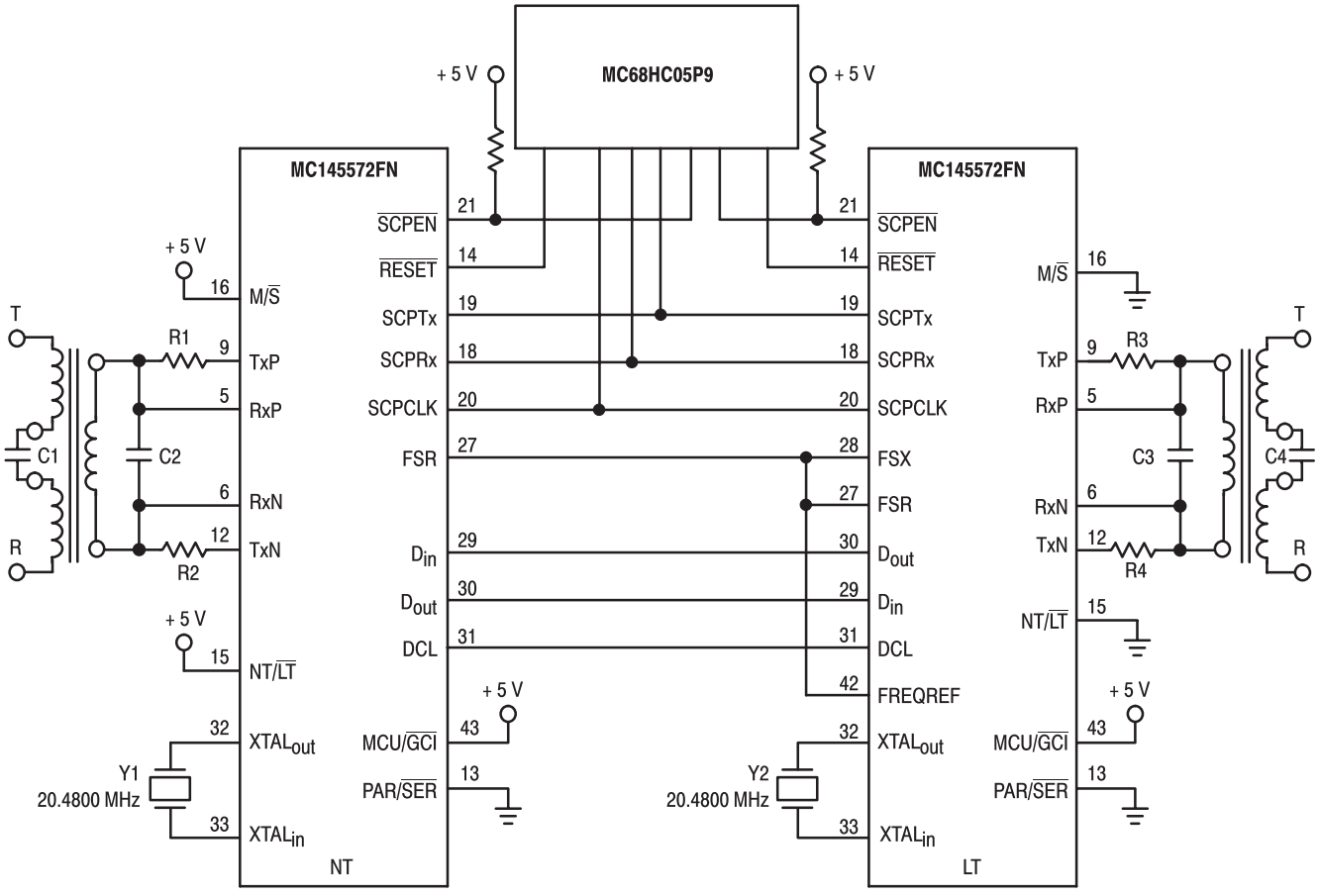


Figure F–1. U–Interface Repeater Using MC145572FN and MC68HC05P9

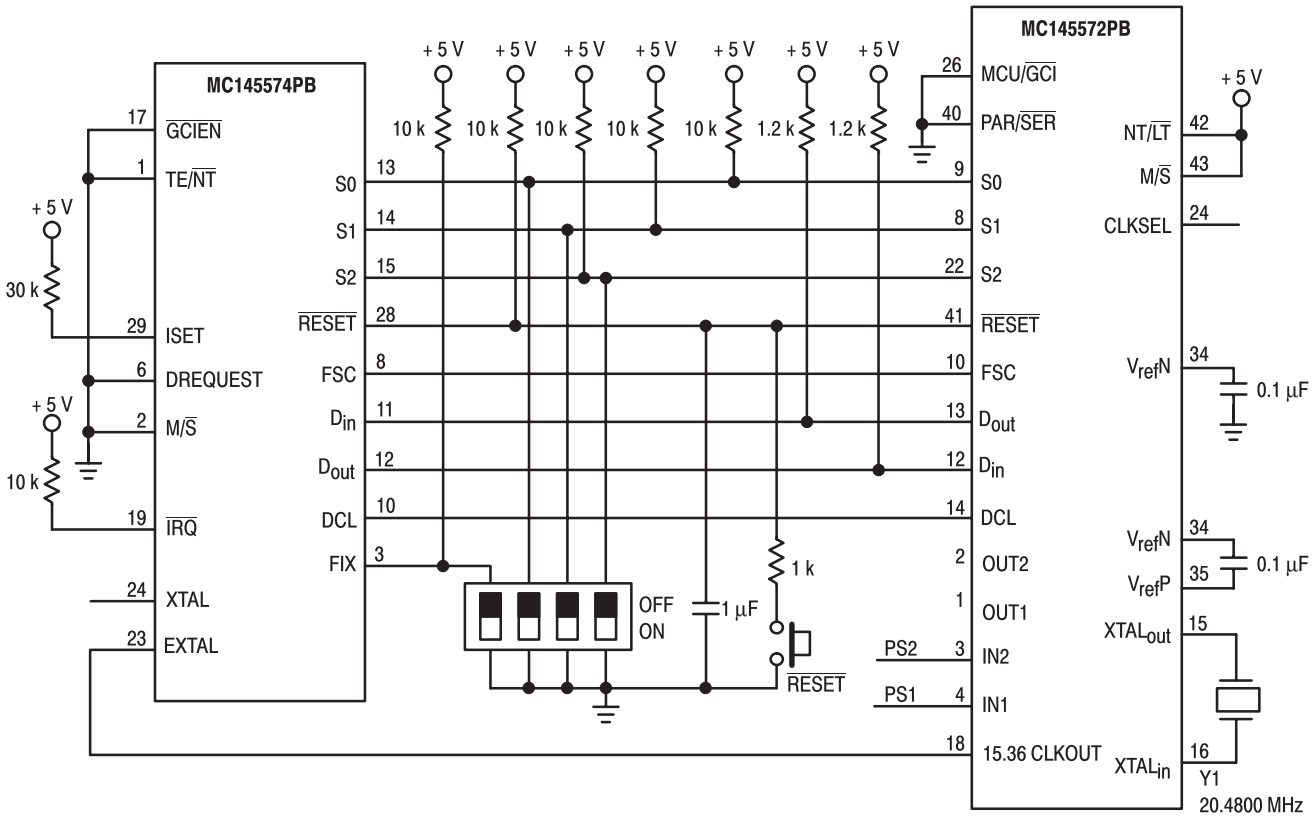


Figure F–2. Two–Chip NT1

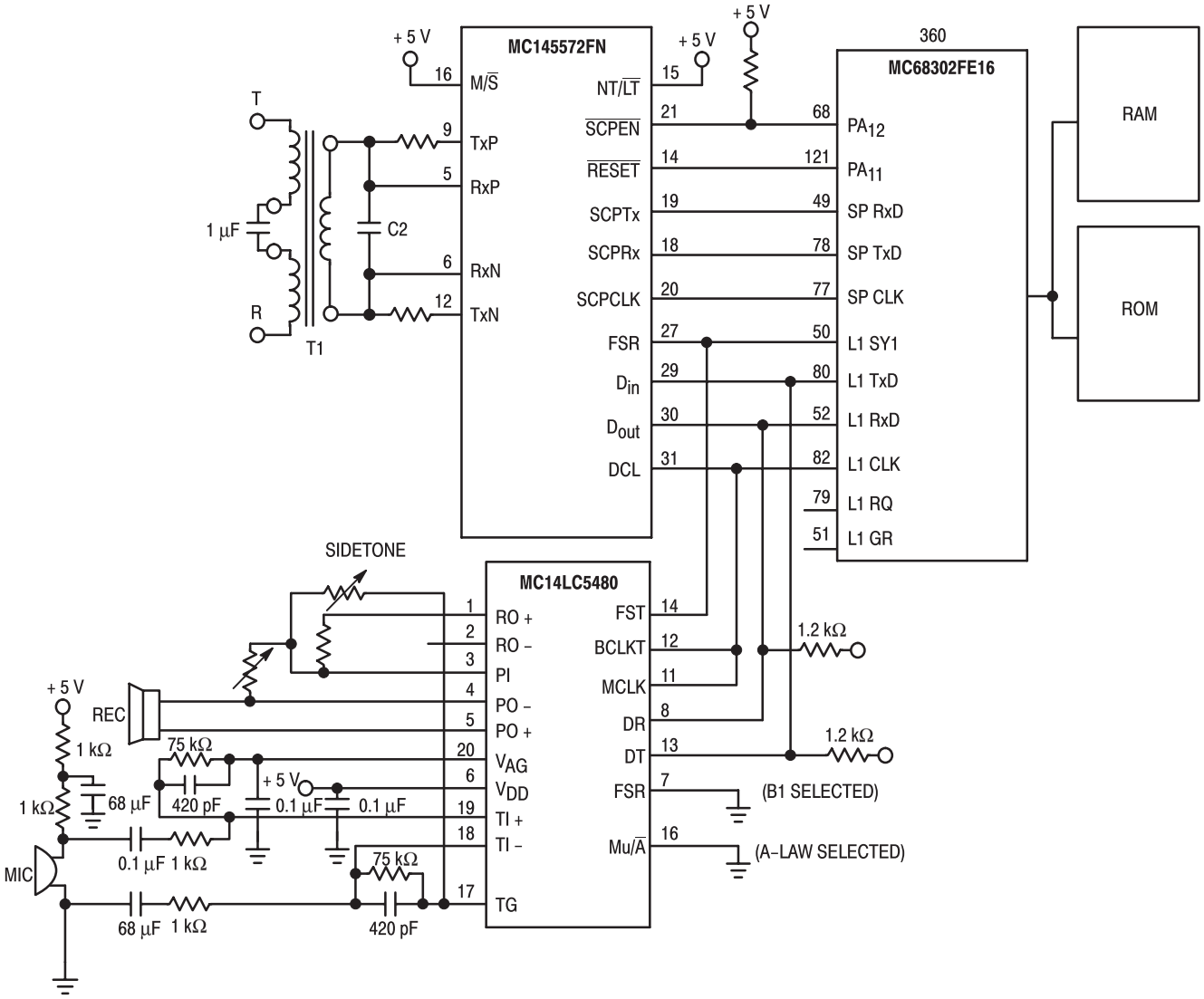
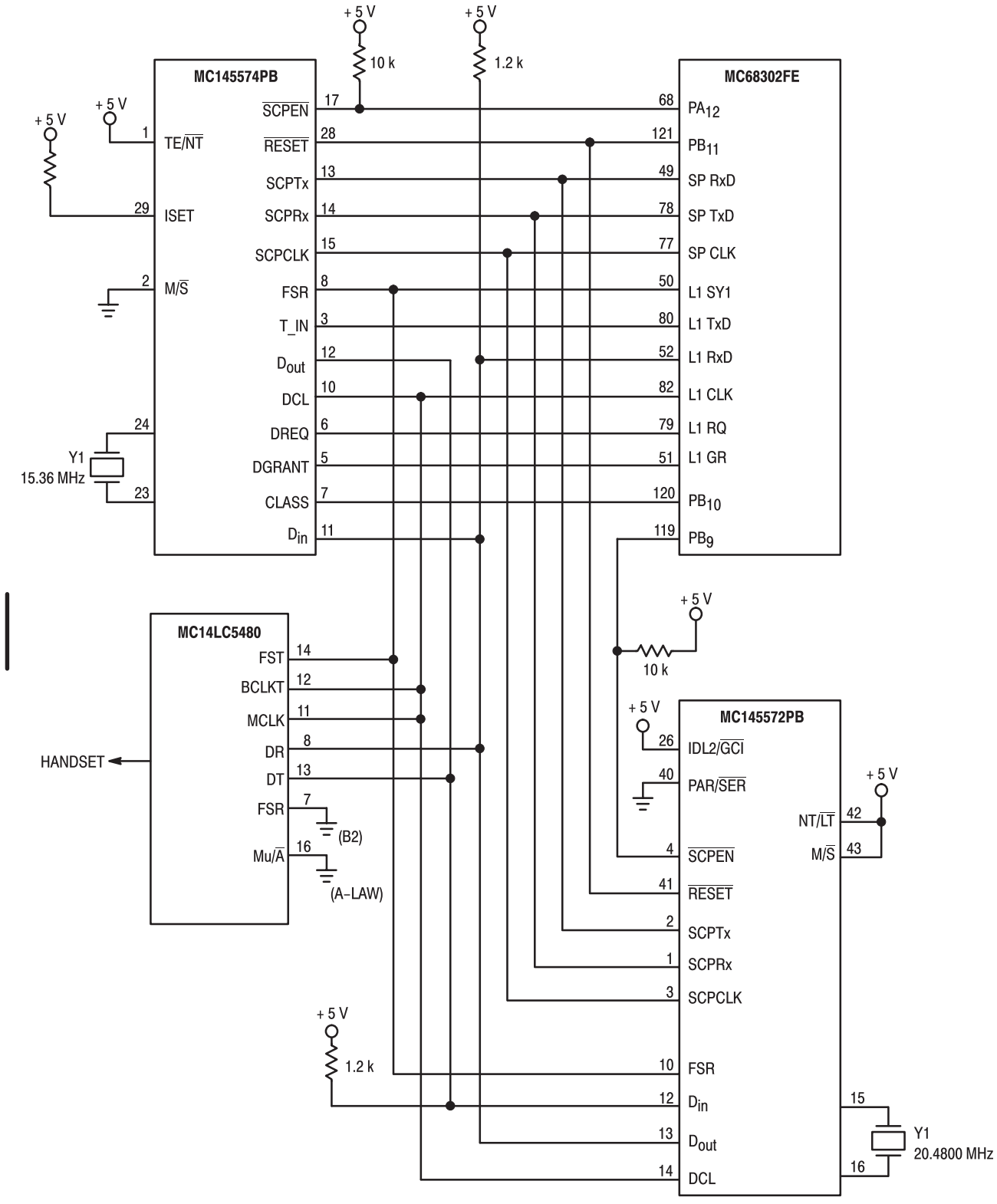
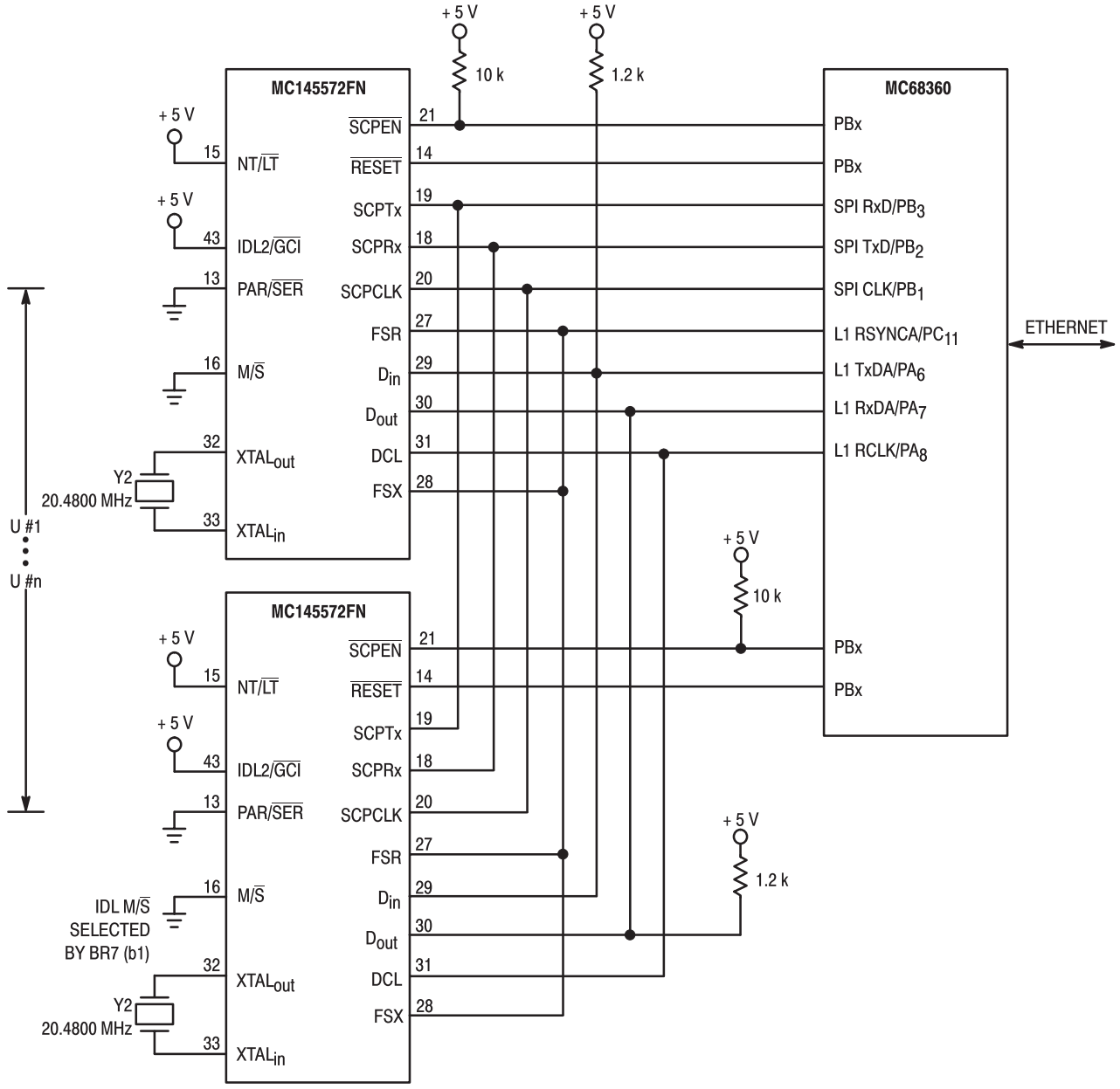


Figure F–3. U–Terminal



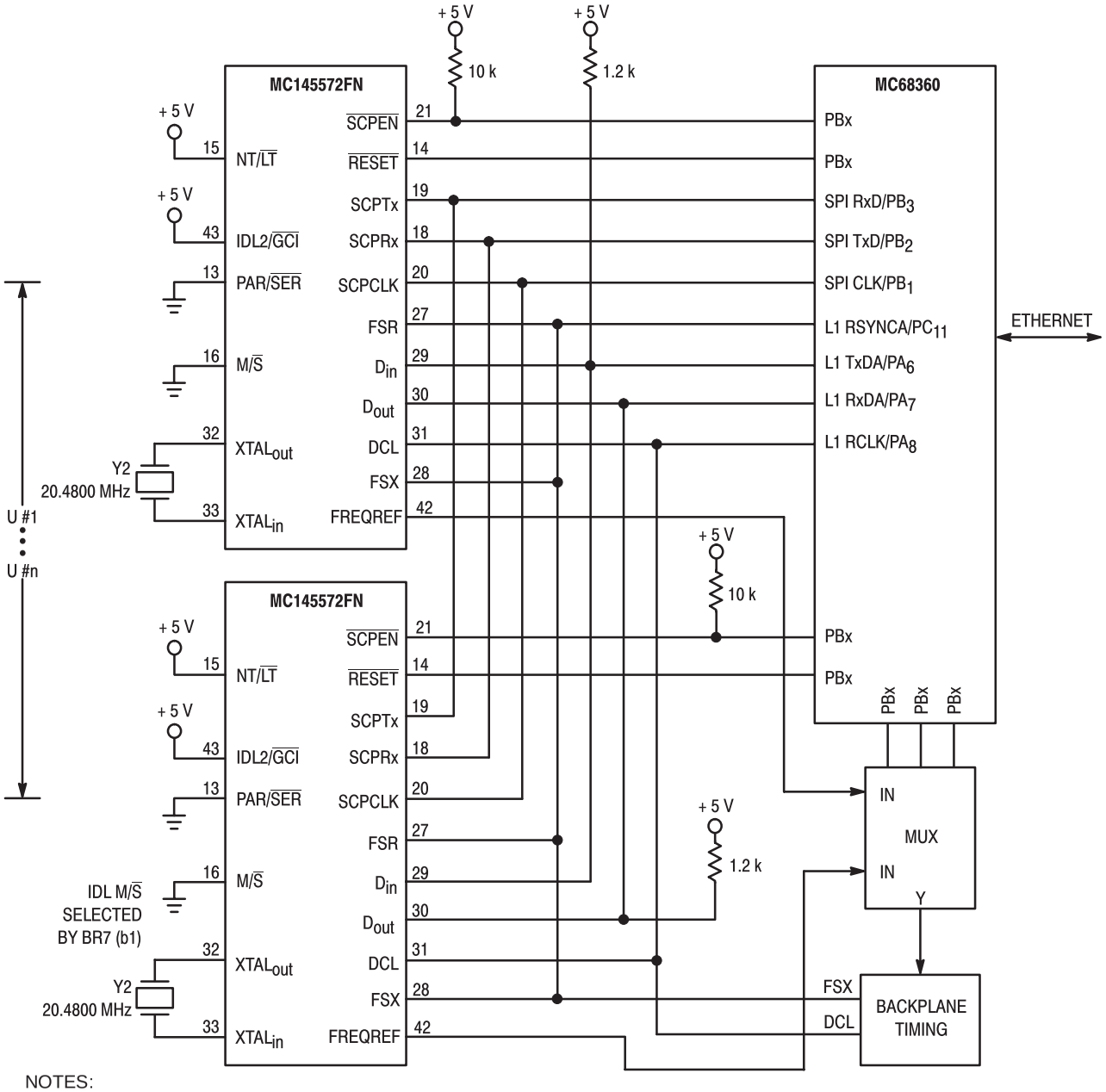
NOTE: Pullup resistors are required on IDL and SCP signals.

Figure F–4. ISDN Smart NT1 Application with MC145572 and MC145574 in NT Terminal Mode



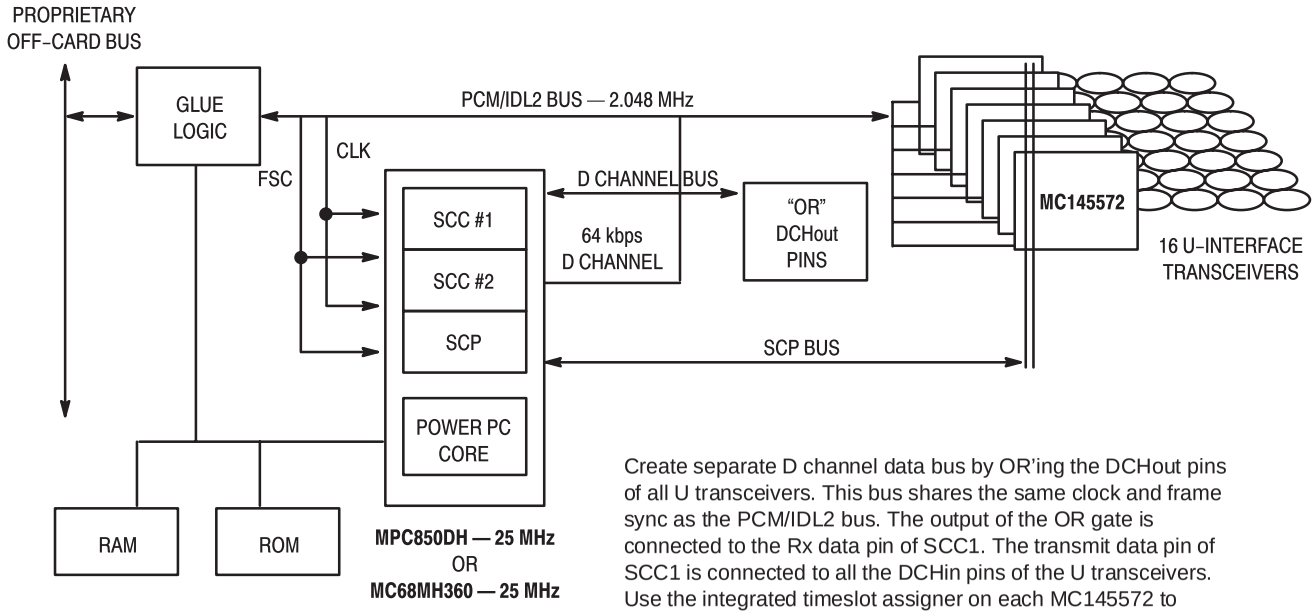
NOTES:
1. One U–transceiver is configured as IDL master, the rest are configured as slaves. Set BR7 (b1) = 1 to change master/slave mode operation.
2. Pullup resistors are required on IDL and SCP signals.

Figure F–5. Remote Access Multi–Line Configuration No. 1



NOTES:
1. All U–transceivers are configured as slaves.
2. Pullup resistors are required on IDL and SCP signals.

Figure F–6. Remote Access Multi–Line Configuration No. 2



Create separate D channel data bus by OR'ing the DCHout pins of all U transceivers. This bus shares the same clock and frame sync as the PCM/IDL2 bus. The output of the OR gate is connected to the Rx data pin of SCC1. The transmit data pin of SCC1 is connected to all the DCHin pins of the U transceivers. Use the integrated timeslot assigner on each MC145572 to assign D and B channels to individual timeslots.

One MC145572 device can generate timing, others are slaves. All MC145572s can share 20.48 MHz crystal.

NOTES:
1. MC68MH360 supports 32 HDLC channels.
2. MPC850DH supports 84 HDLC channels.

Figure F–7. Multi–Line U Line Card

G
PERFORMANCE

G.1 INTRODUCTION

The following figures show transmission performance when a typical line interface circuit in is used (see Figure G–1).

NOTE

It is the responsibility of the designer to verify that a particular combination of components used to implement a line interface circuit satisfies all criteria for the desired applications.

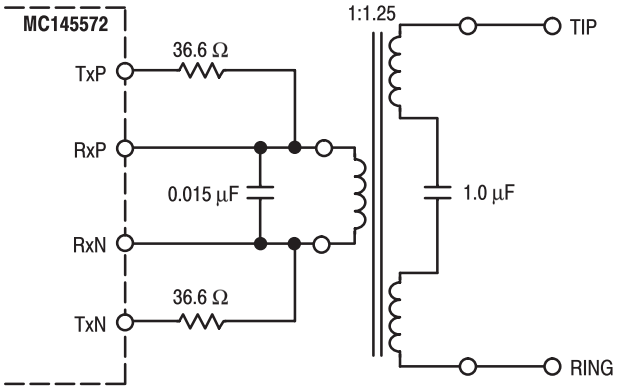


Figure G–1. Typical Line Interface Circuit

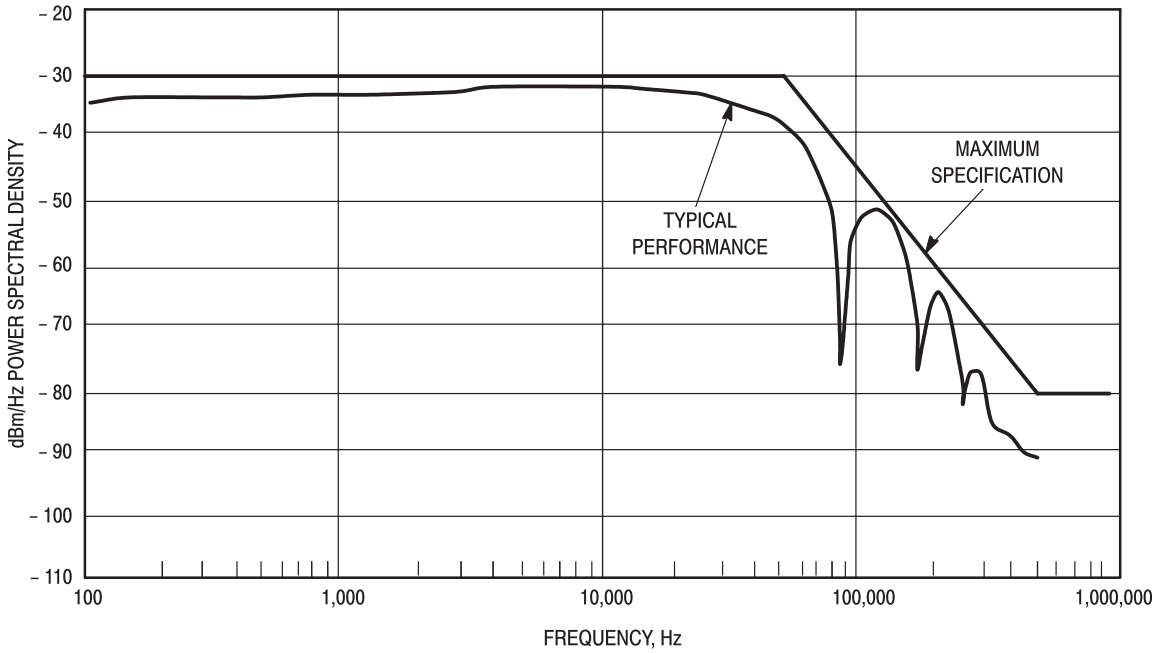


Figure G–2. Typical Power Spectral Density

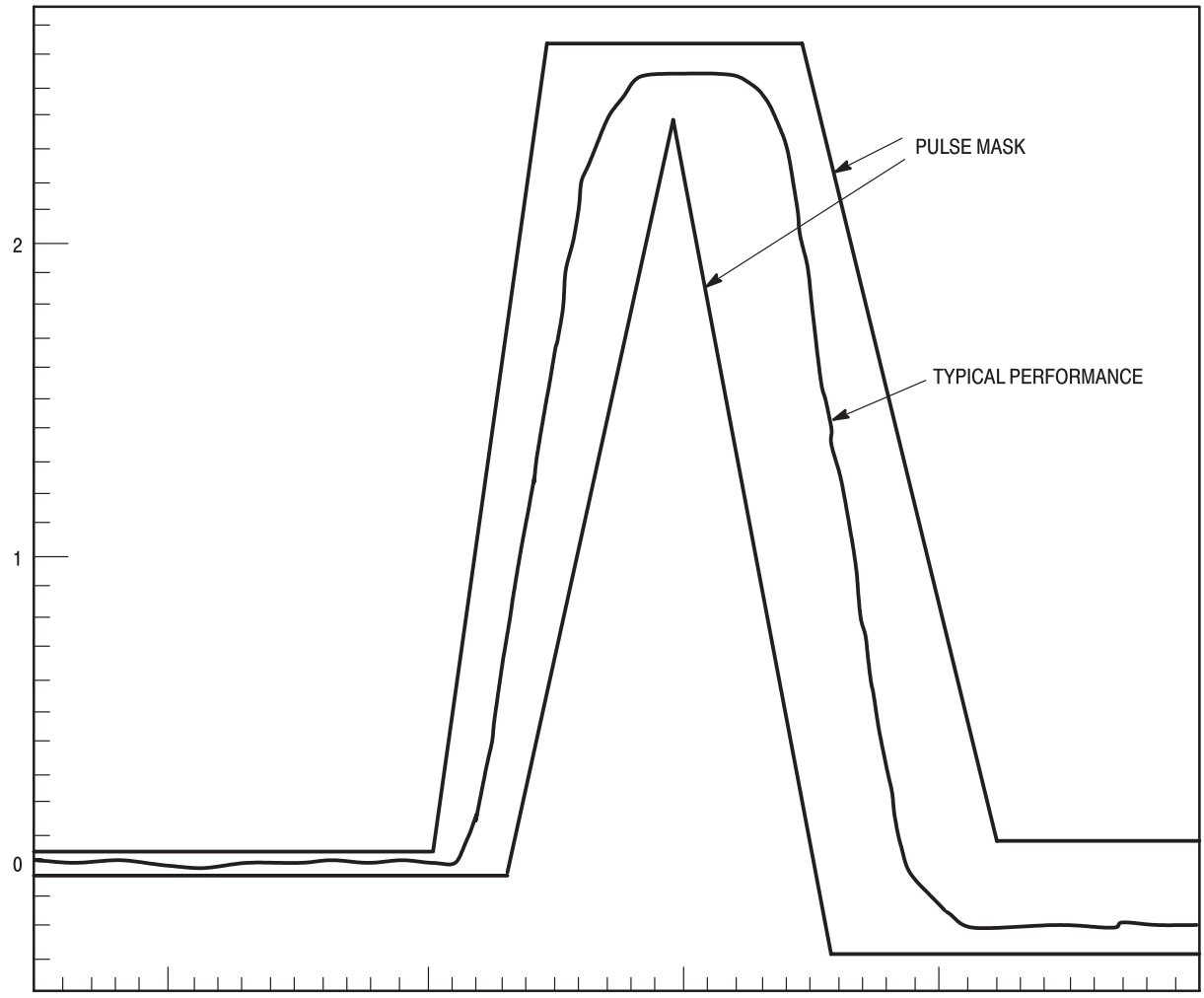
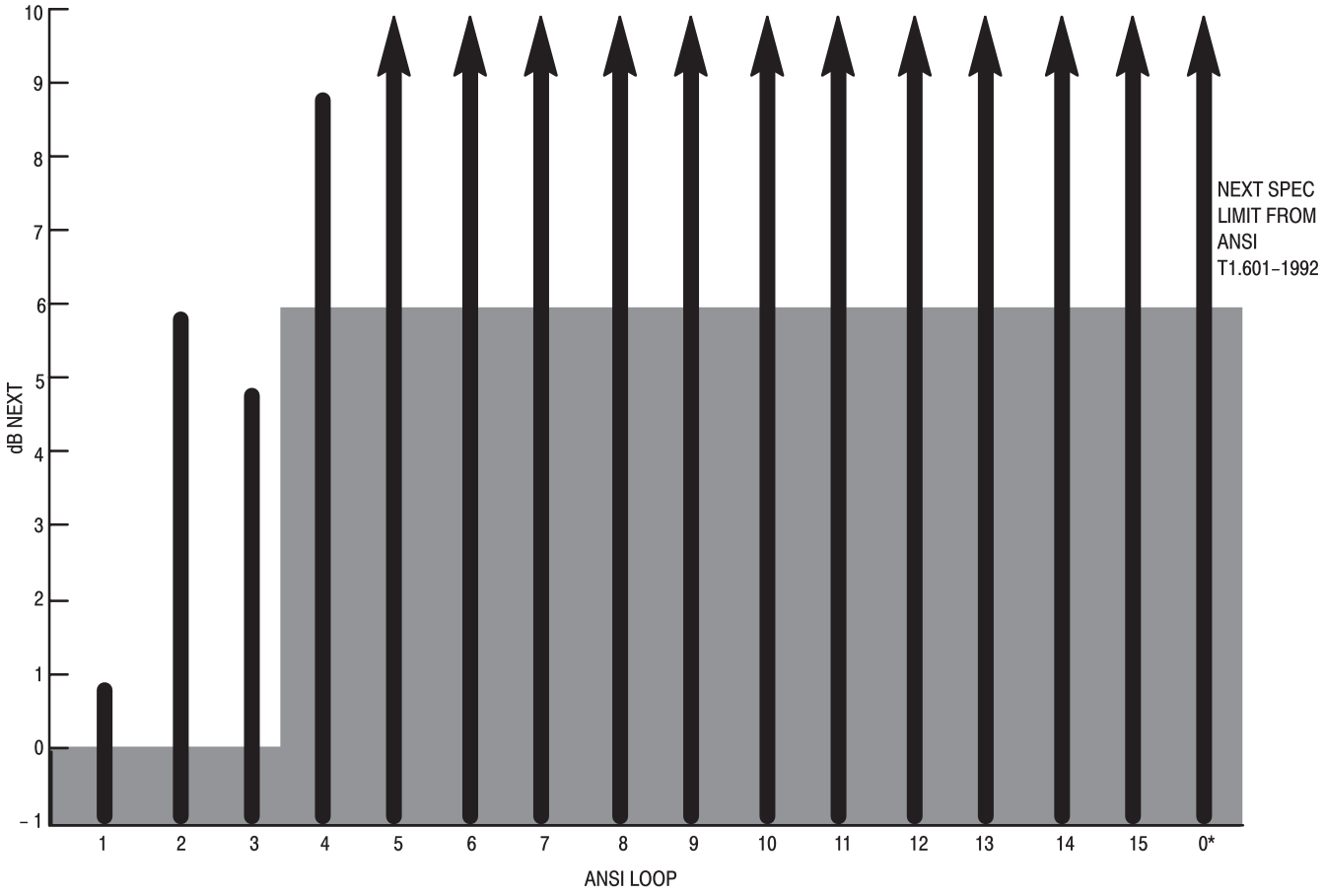


Figure G–3. Typical Pulse Mask



*Indicates zero length loop.

Figure G–4. Loop Performance Using Typical Line Interface Circuit

H

TEST AND DEBUG

H.1 HIGH IMPEDANCE DIGITAL OUTPUT MODE

The MC145572 U–interface transceiver has the capability of forcing all outputs (both analog and digital) to the high impedance state. This feature, known as the Serial Control Port High Impedance Digital Output Mode (SCP HIDOM), is provided to allow in–circuit testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145572.

The SCP HIDOM mode is entered by holding $\overline{\text{SCPEN}}$ low for a minimum of 33 consecutive rising edges of SCPCLK while SCPRx is high. If $\overline{\text{SCPEN}}$ goes high, or if SCPRx goes low, the device will exit the SCP HIDOM mode and return to normal operation.

H.2 CONTROL OF TRANSMIT SIGNALS

The MC145572 permits an external microcontroller to take control of the transmit Superframe Framer by writing to control bits in Byte register 8. This is very useful for debugging prototypes, since the MC145572 can be forced to transmit a variety of signals regardless of the presence or lack of presence, of a signal on the receive pins. Table 4–8 summarizes these signals and the control bits.

The MC145572 can be forced to transmit SL0, SL1, SL2, SL3, SN0, TN+ SN1, SN2, SN3, 10 kHz and 40 kHz tones, and alternating quats. See the description of BR8 in **Section 4.4.9** for more details.

H.3 CHARACTERIZATION OF THE PULLABLE CRYSTAL

The MC145572 makes it very easy to measure the free running frequency of oscillation of the 20.48 MHz crystal oscillator and to measure its frequency pullablility. This is done by using the 20.48 MHz square wave signal on the $\text{BUFXTAL}_{\text{out}}$ pin to drive a frequency counter. Make sure that this output has not been turned off. Never probe the crystal pins, since the capacitance of the probe introduces severe errors in the measurement.

Also, the measured frequency must be verified against the make tolerance of the crystal at 25°C. Do not include the aging and temperature tolerances of the crystal when performing free running frequency checks at room temperature. If it is desired to verify operation of the crystal oscillator over temperature, then the crystal temperature tolerance should be included. The MC145572 has a typical crystal load capacitance including board traces of about 24 pF. Note that individual board implementations may change this figure slightly.

The free running frequency of oscillation of the 20.48 MHz oscillator can be characterized when the MC145572 is set to NT mode operation. In NT mode, the on–chip variable capacitance array is set for the nominal center frequency point when the transceiver is deactivated. A frequency of 20.48 MHz plus or minus the tolerance is measured at $\text{BUFXTAL}_{\text{out}}$. It may be necessary to change the crystal calibration load capacitance specification slightly in order to have the free running frequency of oscillation meet the 20.48 MHz specification. The nominal crystal load capacitance is 24 pF.

The pullability of a crystal can be measured by putting the MC145572 into LT mode and changing the frequency applied to the FREQREF input pin. Any external square wave clock source can be used for this, but *do not* use a clock that is generated by, or derived from, the MC145572 on which the test is being performed, since this may cause the on–chip PLL to force the on–chip capacitance array to its mid–frequency point at all times.

To measure the pullability towards the low frequency direction, pull FREQREF to V_{DD} or V_{SS}. This causes the on–chip PLL to attempt to pull the 20.48 MHz crystal towards dc. Since this is not possible, the MC145572 pulls the crystal as low in frequency as possible by driving the on–chip capacitance

to its maximum value. Once the frequency of oscillation has stabilized, the negative direction pullability can be measured with a frequency counter at $BUFXTAL_{out}$. If a board is designed to have a pull up resistor on FREQREF, then automatic test equipment can be programmed for the low frequency measurement and to inject a high frequency clock for the high frequency measurement.

To measure the pullability towards the high frequency direction, FREQREF is driven with a square wave signal that can be between 8001 Hz and 20 MHz. Note that 8001 Hz is + 1000 ppm, which exceeds the pull range of the on–chip PLL. This causes the on–chip capacitance array to go to its minimum value and thereby increases the frequency of the 20.48 MHz oscillator. Once the oscillator has stabilized, the frequency of oscillation is measured at $BUFXTAL_{out}$.

It is also possible to use the 4.096 CLKOUT pin to do these measurement, but it is necessary to relate the pullability in ppm to 4096 kHz instead of 20.48 MHz.

Example 1: Free Running Frequency of Oscillation Measurement at Room Temperature

Configuration:

MC145572 in NT mode

Crystal specification is 20.48 MHz ± 15 ppm. See **Section B.3.2.**

Results:

$BUFXTAL_{out}$ measures as 20,480,307.2 Hz

((|20,480,307.2 Hz – 20,480,000 Hz|)*1,000,000 ppm) / 20,248,000 Hz = + 15 ppm

Example 2: Oscillator Pullability Measurement at Room Temperature

Crystal specification is ± 20.48 MHz with 360 ppm or ± 180 ppm pull between 15 and 45 pF. See **Section B.3.** In this example, 20,480,000 MHz is used as the nominal frequency. In a real life situation it may be desirable to use the actual measured free run frequency when measuring pullability.

Configuration 1:

MC145572 in LT mode

FREQREF connected to V_{SS}

Results:

$BUFXTAL_{out}$ measures as 20,475,801.6 Hz

((|20,475,801.6 Hz – 20,480,000 Hz|)*1,000,000 ppm) / 20,248,000 Hz = – 205 ppm

Configuration 2:

MC145572 in LT mode

FREQREF connected to 4 MHz

Results:

$BUFXTAL_{out}$ measures as 20,483,952.6 Hz

((|20,483,952.6 Hz – 20,248,000 Hz|)*1,000,000 ppm) / 20,248,000 Hz = + 193 ppm

Conclusion:

Since 20.48 MHz + 193 ppm, – 205 ppm exceeds the ± 180 ppm minimum crystal pull range specification, the oscillator is working correctly.

GLOSSARY OF TERMS AND ABBREVIATIONS

The list contains terms found in this and other Motorola publications concerned with Motorola Semiconductor Products for Communications.

A–Law — A European companding/encoding law commonly used in PCM systems.

A/B Signaling — A special case of 8th–bit (LSB) signaling in a μ–law system that allows four logic states to be multiplexed with voice on PCM channels.

A/D (analog–to–digital) converter (ADC) — A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

Aliasing Noise — A distortion component that is created when frequencies present in a sampled signal are greater than one–half the sample rate.

Answer Back — A signal sent by receiving data–processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data.

Anti–Aliasing Filter — A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

Asynchronous — A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Attenuation — A decrease in magnitude of a communication signal.

Bandwidth — The information–carrying frequencies between the limiting frequencies of a communication line or channel.

Baseband — The frequency band occupied by information–bearing signals before combining with a carrier in the modulation process.

Baud — A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel.

Bit Rate — The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

Blocking — A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party.

BORS(C)HT — Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

Broadband — A transmission facility whose bandwidth is greater than that available on voice–grade facilities. (Also called wide band.)

C Message — A frequency weighting that evaluates the effects of noise based on its annoyance to the “typical” subscriber of standard telephone service or the effects of noise (background and impulse) on voice–grade data service.

Carrier — An analog signal of fixed amplitude and frequency that combines with an information–bearing signal by modulation to produce an output signal suitable for transmission.

CCITT — Consultative Committee for International Telephone and Telegraph; an international standards group of European International Telecommunications Union.

CCSN — Common Channel Signaling Network.

Central Office (CO) — A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers.

Channel Bank — Communication equipment commonly used for multiplexing voice–grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

CIDCW — Calling Identity Delivery on Call Waiting; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party, while the called party is off–hook.

CLASS — Custom Local Area Signaling Service; a set of services, enhancements, provided to TELCO customers which may include CND, CNAM, Message Waiting, and other features.

CLID — Calling Line IDentification; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

CNAM — Calling Name Delivery; a subscriber feature which allows for the display of the time, date, number, and name of the caller to the called party.

CND — Calling Number Delivery; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

CODEC — COder–DECoder; the A/D and D/A function on a subscriber line card in a telephone exchange.

COFIDEC — COder–Filter–DECoder; the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

Common Mode Rejection — The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential–input terminals.

Companding — The process in which dynamic range compression of a signal is followed by expansion in accordance with a given transfer characteristic (companding law) which is usually logarithmic.

Compander — A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal–to–noise ratio.

Conference Call — A call between three or more stations, in which each station can carry on a conversation simultaneously.

CPE — Customer Premise Equipment; this could be a POTS phone, answering machine, fax machine, or any number of other devices connected to the PSTN.

Crosspoint — The operating contacts or other low–impedance–path connection over which conversations can be routed.

Crosstalk — The undesired transfer of energy from one signal path to another.

CSN — Circuit Switched Network.

CTS — Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line.

CVSD — Continuous Variable Slope Delta (modulation); a simple technique to converting an analog signal (like voice) into a serial bit stream.

D3 — D3 channel bank; a specific generation of an AT&T 24–channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

D/A (digital–to–analog) converter (DAC) — A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

Data Compression — A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

dB (decibel) — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and

20 x log (V1/V2) for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

dBmO — Signal power measured at a point in a standard test tone level at the same point.

i.e., dBmO = dBm = dBr

where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

dBmOp — Relative power expressed in dBmp. (See dBmO and dBmp.)

dBmp — Indicates dBm measurement made with a psophometric weighting filter.

dBrn — Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = – 90 dBm.

dBrnC — Indicates dBrn measurement made with a C–message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.)

dBrnc0 — Noise measured in dBrnc referenced to zero transmission level.

Decoding — A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delay Distortion — Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.)

Delta Modulation — A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable–slope delta (CVSD) modulation.

Demodulator — A functional section of a modem that converts received analog line signals to digital form.

DN — Directory Number.

Digital Telephone — A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.)

Distortion — The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

DPSK — Differential Phase Shift Keying; a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180°, and 290° to define the digital information.

DTMF — Dual Tone Multi–Frequency. It is the "tone dialing" system based on outputting two non–harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Duplex — A mode of operation permitting the simultaneously two–way independent transmission of telegraph or data signals.

Echo — A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregularities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both.

Echo Suppressor — A device used to minimize the effect of echo by blocking the echo return currents; typically a voice–operated gate that allows communication one way at a time.

Encoder (PCM) — A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Equalizer — An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency–dependent transmission line.

ET — Exchange Termination (CO Switch).

FDM — Frequency–Division Multiplex; a process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

Four Wire Circuit — The portion of a telephone, or central office, that operates on two pairs of wires. One pair is for the transmit path (generally from the microphone), and one pair is for the receive path (generally from the receiver).

Frame — A set of consecutive digit timeslots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Full Duplex — A mode of operation permitting simultaneous transmission of information between two locations in both directions.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Gain Tracking Error — The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

HDLC — High–Level Data Link Control; a CCITT standard data communication line protocol.

Half Duplex — A transmission system that permits communication in one direction at a time. CB ratios, with “push–to–talk” switches, and voice–activated speakerphones, are half duplex.

Handset — A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear.

Hookswitch — A switch that connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Idle Channel Noise (ICN) — The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wide–band noise measurement using a C–message weighting filter to band–limit the output noise).

Intermodulation — The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation Distortion — An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation.

IRED — Infrared. Used as a wireless link for remote control or to transfer data.

ISDN — Integrated Services Digital Network; a communication network intended to carry digitized voice and data multiplexed onto the public network.

Jitter — A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency, or phase.)

Key System — A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

Mu–Law — (μ–law) A companding law accepted as the North American standard for PCM based systems.

LAN — Local Area Network; a data–only communication network between data terminals using a standard interface to the network.

Line — The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges.

Line Length Compensation — Also referred to as loop length compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Longitudinal Balance — The common–mode rejection of a telephone circuit.

Loop — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loopback — Directing signals back toward the source at some point along a communication path.

Loop Current — The dc current that flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

LT — Line Termination (Line Card).

MCU — MicroComputer Unit (also MicroController Unit).

MPU — MicroProcessor Unit.

Mu–Law — A companding/encoding law commonly used in U.S. (same as μ–law).

MUX — Multiplex or multiplexer.

Modem — MOdulator–DEModulator; a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

Multiplex — To simultaneously transmit two or more messages on a single channel.

NT1 — Network Termination 1 (OSI Layer 1 Only).

NT2 — Network Termination 2 (OSI Layers 2 and 3).

Off–Hook — The condition when the telephone is connected to the phone system, permitting loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On–Hook — The condition when the telephone's dc path is open, and no dc loop current flows. The central office regards an on–hook phone as available for ringing.

PABX — Private Automatic Branch Exchange; a customer–owned, switchable telephone system providing internal and/or external station–to–station dialing.

Pair — The two associated conductors that form part of a communication channel.

Pass–Band Filter — A filter used in communication systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

PBX — Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

PCM — Pulse Code Modulation; a method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8–bit words.

Phase Jitter — Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

PLL — Phase–Locked Loop.

PLL Frequency Synthesizer — Phase–locked loop frequency synthesizer. A frequency synthesizer utilizing a closed loop, as opposed to DDS (direct digital synthesis) which is not a closed loop.

POTS — Plain Old Telephone Service.

Propagation Delay — The time interval between specified reference points on the input and output voltage waveforms.

Psophometric Weighting — A frequency weighting similar to C–Message weighting that is used as the standard for European telephone system testing.

PSN — Packet Switched Network.

PSTN — Public Switched Telephone Network.

Pulse Dialer — A device that generates pulse trains corresponding to digits or characters used in impulse or loop–disconnect dialing.

Quantizing Noise — Signal–correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

REN — Ringer Equivalence Number; an indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals about 8 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Repeater — An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

Repertory Dialer — A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

Ring — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

RTS — Request To Send; an EIA–232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

Sampling Rate — The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band–limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction.

SCU — Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2–to–4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Signaling — The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

Signal–to–Distortion Ratio (S/D) — The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

SLIC — Subscriber Line Interface Circuit; a circuit that performs the 2–to–4 wire conversion, battery feed, line supervision, and common mode rejection at the central office (or PBX) end of the telephone line.

SOG Package — Small–Outline Gull–wing package; formerly SOIC with gull–wing leads. This package has leads which fold out from the body.

SOJ Package — Small–Outline J–lead package; formerly SOIC with J leads. This package has leads which are tucked under the body.

Speech Network — A circuit that provides 2–to–4 wire conversion, i.e., connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber Line — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Switchhook — A synonym for hookswitch.

Syn (Sync) — (1) A bit character used to synchronize a time frame in a time–division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

Synchronous Modem — A modem that uses a derived clocking signal to perform bit synchronization with incoming data.

T1 Carrier — A PCM system operating at 1.544 MHz and carrying 24 individual voice–frequency channels.

TA — Terminal Adapter.

Talkdown — Missed signals in the presence of speech. Commonly used to describe the performance of a DTMF receiver when it fails to recognize a valid DTMF tone due to cancellation of that tone by speech.

Talkoff — False detections caused by speech. Commonly used to describe the performance of a DTMF receiver when speech, emulating DTMF, causes the receiver to believe it has detected a valid DTMF tone.

Tandem Trunk — See trunk.

Telephone Exchange — A switching center for interconnecting the lines that service a specific area.

TE1 — Terminal Equipment 1 (ISDN Terminal).

TE2 — Terminal Equipment 2 (Non–ISDN Terminal).

TELETEX — A text communication service between entirely electronic workstations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.)

TELETEXT — The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.)

Time–Division Multiplex — A process that permits the transmission of two or more signals over a common path by using a different time interval for each signal.

Tin Cans and String — A *crude* analog communications system commonly used to introduce voice communications to children.

Tip — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80 – 90 volts rms, 20 Hz.

Trunk — A telephone circuit or channel between two central offices or switching entities.

TSAC — Timeslot Assigner Circuit; a circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream.

TSIC — Timeslot Interchange Circuit; a device that switches digital highways in PCM based switching systems; a "digital" cross-point switch.

Twist — The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.)

Two Wire Circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

UDLT — Universal Digital Loop Transceiver; a Motorola originated name for a voice/data transceiver circuit.

VCO — Voltage–Controlled Oscillator. Input is a voltage; output is a sinusoidal waveform.

VCM — Voltage–Controlled Multivibrator. Input is a voltage; output is a square wave.

Voice Frequency — A frequency within that part of the audio range that is used for the transmission of speech of commercial quality (i.e., 300 – 3400 Hz).

Weighting Network — A network whose loss varies with frequency in a predetermined manner.

J

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