Power Solution for Wearable AMOLED Products

General Description

The RT4730 is a highly integrated power solution with Buck-Boost, and inverting charge pump to generate positive and negative output voltage. The output voltages can be adjusted with by SWIRE interface protocols. With its input voltage range of 2.9V to 5.2V, the RT4730 is optimized for products powered by single-cell batteries and symmetrical output currents up to 50mA. The RT4730 is available in the WL-CSP-16B 2.34x2.34 (BSC) package.

Ordering Information

RT4730 □

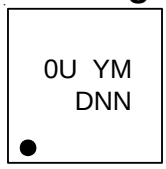
Package Type
WSC : WL-CSP-16B 2.34x2.34 (BSC)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



0U : Product Code

YMDNN : Date Code

Features

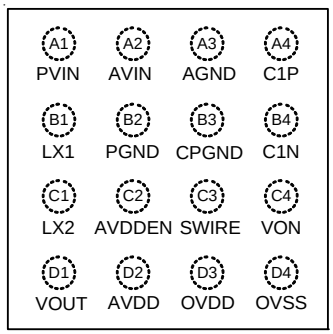
- **Input Voltage Range : 2.9V to 5.2V**
- **Positive Output Voltage AVDD : 3.3V**
- **Positive Output Voltage OVDD Range : 2.8V to 4V (Default is 3.3V ±1%)**
- **Negative Output Voltage OVSS Range : –0.6V to –4V (Default is –3.3V ±1%)**
- **Excellent Line/Load Regulation**
- **Excellent Line/Load Transient**
- **Advanced Power-Save Mode for Light-Load Efficiency**
- **Low Output Ripple Voltage**
- **Built-in Internal Soft-Start**
- **True Output Load Disconnect From Input**
- **UVLO, SCP, OCP, OTP, OVP Protection**
- **Shutdown Current : Typ. 0.1μA**

Applications

- Wearable AMOLED Products

Pin Configuration

(TOP VIEW)



WL-CSP-16B 2.34x2.34 (BSC)

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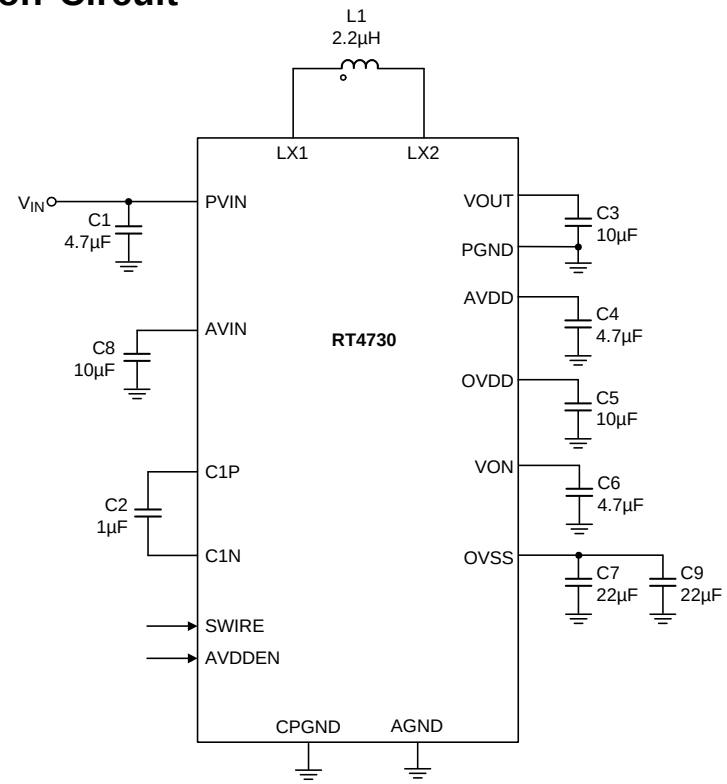
Typical Application Circuit



Recommend Component BOM List

Reference	Quantity	Description	Part Number	Package	Supplier
L1	1	2.2µH	1269AS-H-2R2M=P2	2.5mm x 2.0mm x 1.0mm	Murata
			ZTLF-2016TB-2R2M	2.0mm x 1.6mm x 1.0mm	ZenithTek
C1、C4、C6	3	4.7µF/16V/X5R	GRM188R61C475KAAJD	0603	Murata
C3、C5	2	10µF/16V/X5R	GRM188R61C106KAALD	0603	Murata
C2	1	1µF/6.3V/X5R	GRM033R60J105MEA2	0201	Murata
C8	1	10µF/6.3V/X5R	GRM155R60J106ME15	0402	Murata
C7、C9	2	22µF/6.3V/X5R	GRM155R60J226ME11D	0402	Murata

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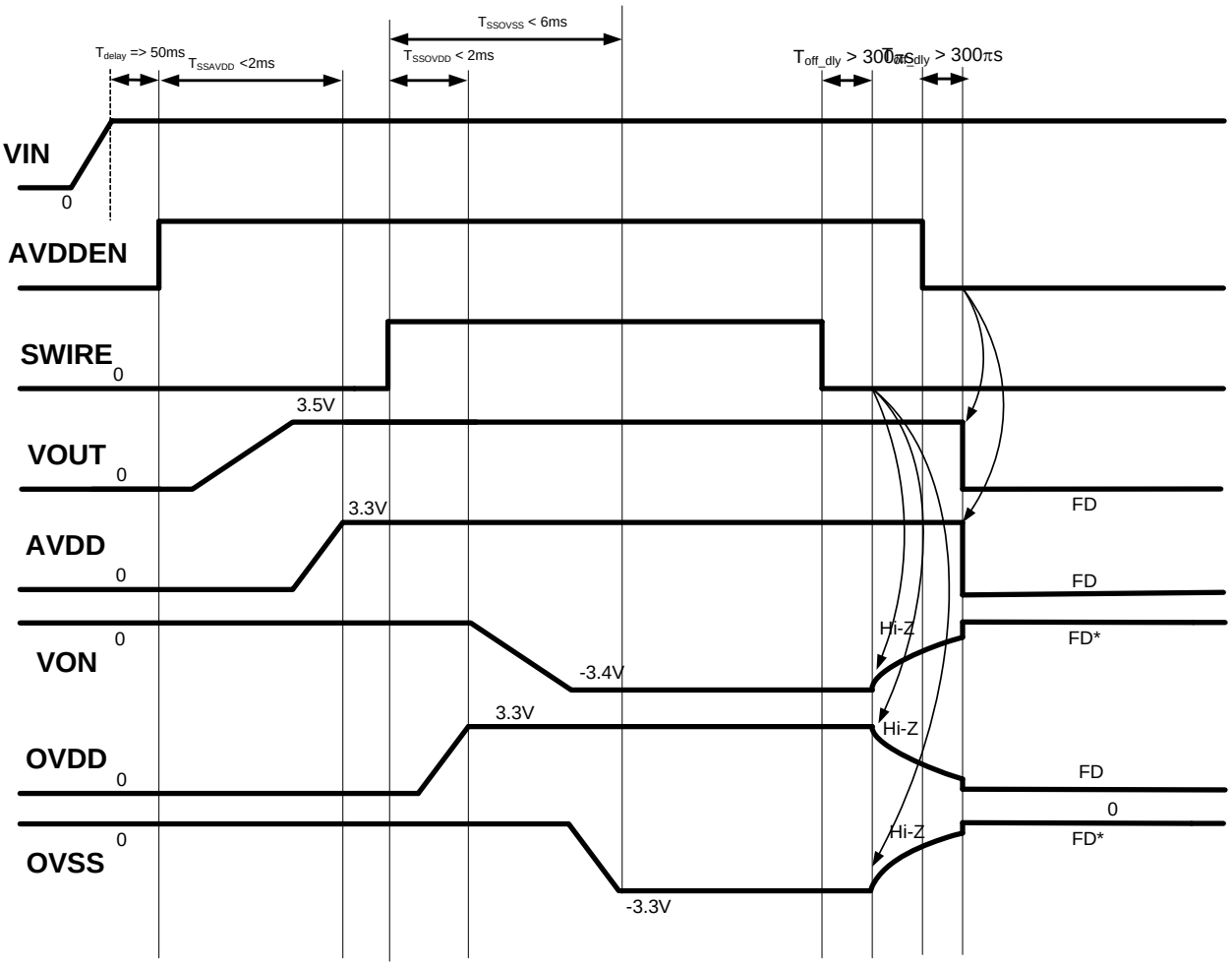
Timing Diagram

Power On/Off Sequence 1

AVDDEN = On→ SWIRE = On→ SWIRE = Off → AVDDEN = Off



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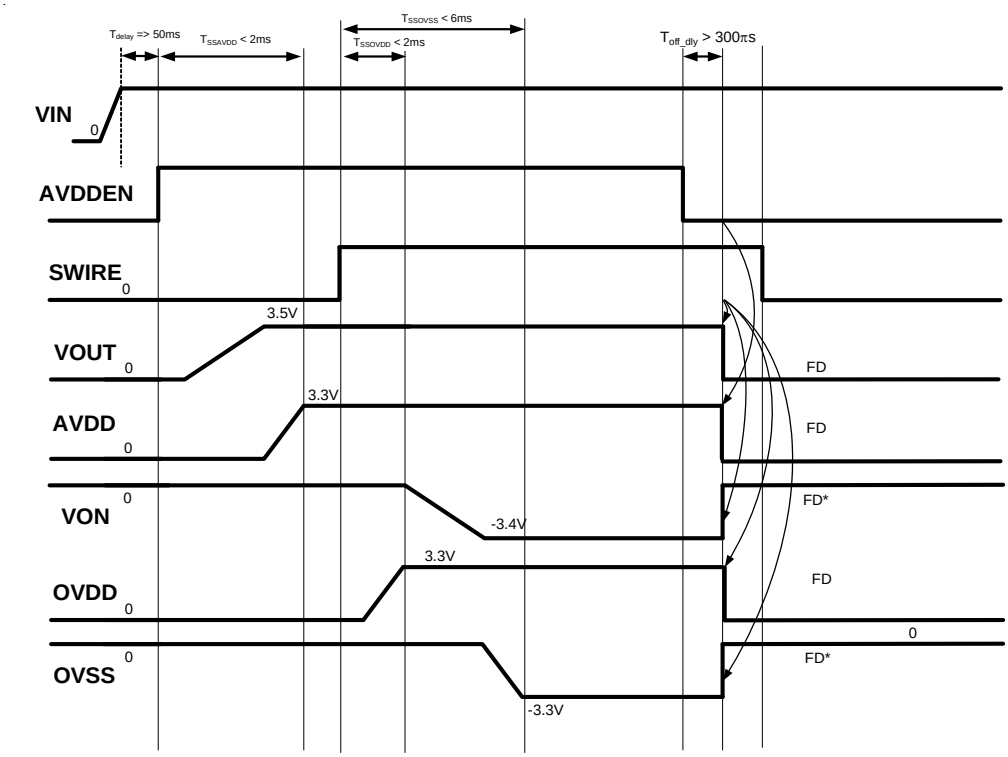
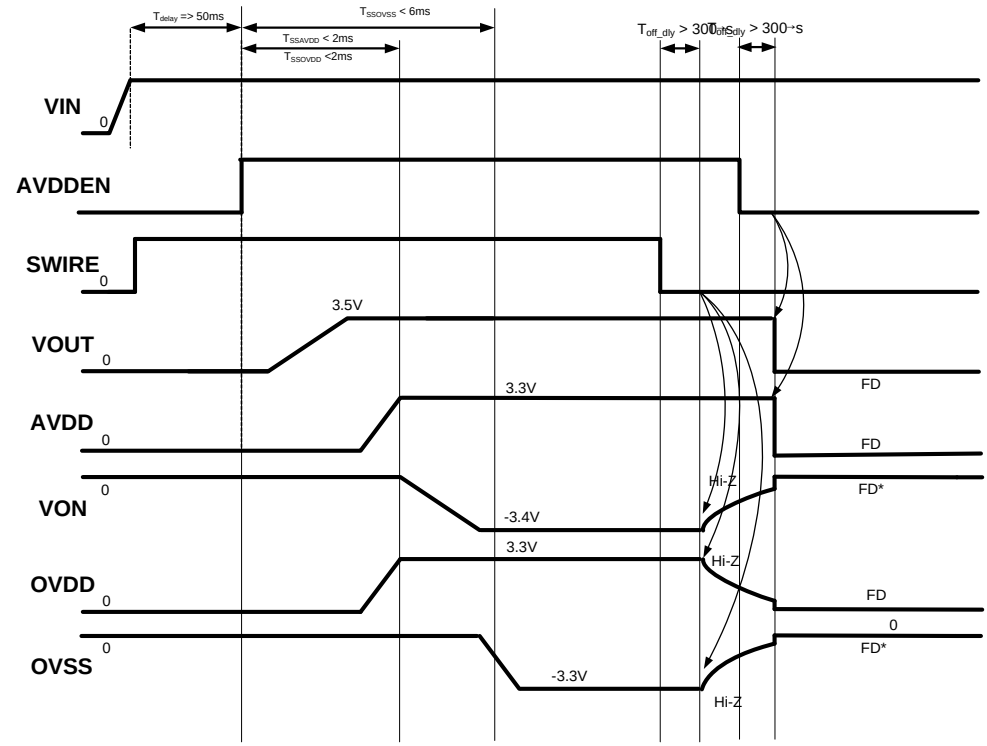
Power On/Off Sequence 2

AVDDEN = On → SWIRE = On → AVDDEN = Off → SWIRE=Off



Power On/Off Sequence 3

SWIRE= On → AVDDEN = On → SWIRE = Off → AVDDEN = Off



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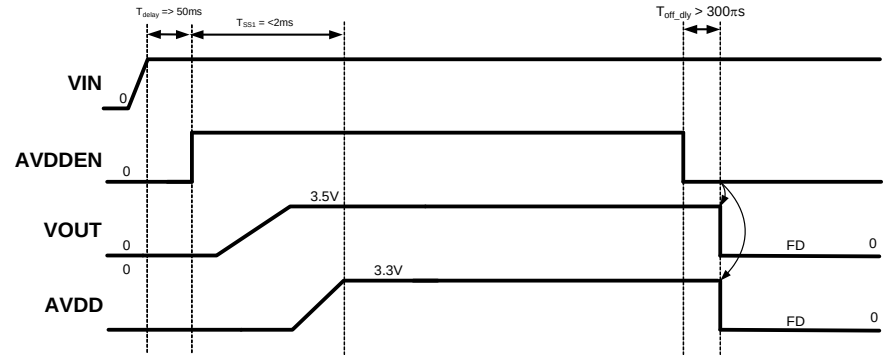
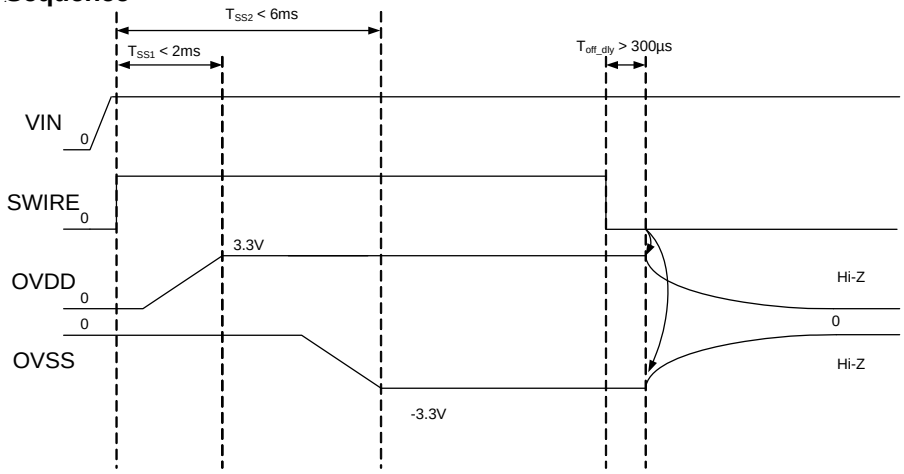
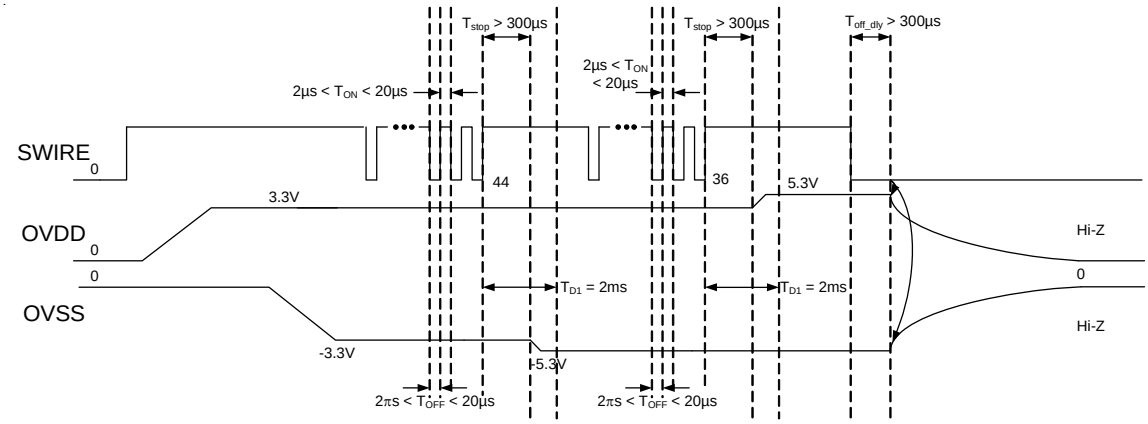
AVDD Power On Sequence



SWIRE Power On Sequence



SWIRE Command Timing Diagram



Power Off Discharge Table

AVDD_EN	SWIRE	AVDD	OVDD	OVSS	BBST	NCP
0	0	FD	FD	FD*	FD	FD*
0	1	FD	FD	FD*	FD	FD*
1	0	--	Hi Z	Hi Z	--	Hi Z
1	1	--	--	--	--	--

FD* : Fast Discharge only 30ms

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Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	PVIN	Power input for buck-boost.
A2	AVIN	Analog power input for IC.
A3	AGND	Analog ground.
A4	C1P	Fly capacitor positive connection.
B1	LX1	LX1 switching node for buck-boost.
B2	PGND	Power ground for buck-boost.
B3	CPGND	Negative charge pump ground.
B4	C1N	Fly capacitor negative connection.
C1	LX2	LX2 switching node for buck-boost.
C2	AVDDEN	Enable for AVDD.
C3	SWIRE	SWIRE control interface.
C4	VON	Negative charge pump output.
D1	VOUT	Buck-boost output.
D2	AVDD	AVDD output.
D3	OVDD	OVDD output.
D4	OVSS	OVSS output.

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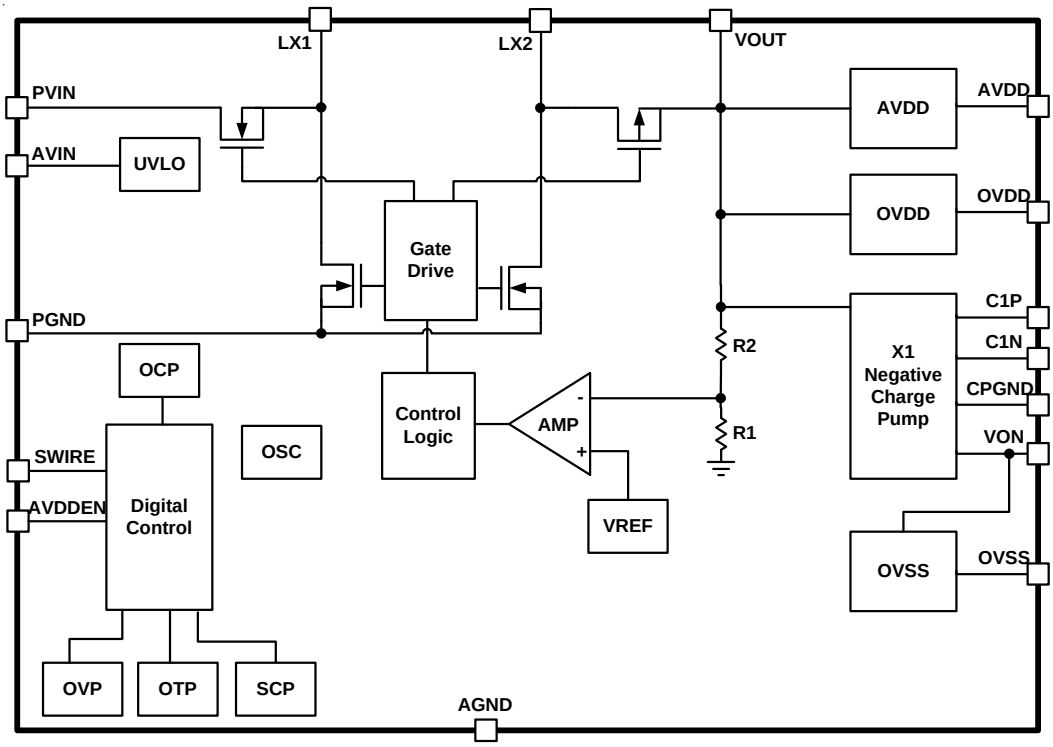
Functional Block Diagram



Operation

The RT4730 is a highly integrated power solution with Buck-Boost, and inverting charge pump to generate positive and negative output voltage. The output voltages can be adjusted with by SWIRE interface protocols. The OVDD voltage range is from 2.8V to 4V with 100mV per step. The OVSS voltage is from –0.6V to –4V with 100mV per step. The AVDD positive output voltage is set at a typical value of 3.3V. With its input voltage range of 2.9V to 5.2V, the RT4730 is optimized for products powered by single-cell batteries and symmetrical output current up to 50mA. The RT4730 provides Over-Temperature Protection (OTP) and Short Circuit Protection (SCP) mechanisms to prevent the device from damage with abnormal operations. When the SWIRE and AVDDEN voltage are logic low, the IC will be shut down with low input supply current less than 2μA.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, AVIN, PVIN to AGND ---------- –0.3V to 6V
- VOUT, AVDD, OVDD, SWIRE, AVDDEN to AGND ---------- –0.3V to 6V
- VON, OVSS to AGND ---------- –6.6V to 0.3V
- C1P, LX1, LX2 ---------- –1V to 6.6V
- C1N ---------- –6.6V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-16B 2.34 x 2.34 (BSC) ---------- 2.36W
- Package Thermal Resistance (Note 2)
  WL-CSP-16B 2.34 x 2.34 (BSC), θ_{JA} ---------- 42.3°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V
  CDM (Charge Device Model) ---------- 500V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.9V to 5.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.7V, AVDD = 3.3V, OVDD = 3.3V, OVSS = –3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply						
Input Supply Voltage	V_{IN}		2.9	3.7	5.2	V
Quiescent Current	I_Q	AVDDEN = high, SWIRE = high	200	400	500	µA
		AVDDEN = high, SWIRE = low	100	200	300	
Shutdown Current	I_{SHDN}	AVDDEN = low, SWIRE = low	--	0.01	2	µA
Under-Voltage Lockout Threshold	V_{UVLOH}	VIN rising	2.3	2.6	2.85	V
	V_{UVLOL}	VIN falling	2.1	2.4	2.65	V
Thermal Shutdown	T_{SD}		135	140	163	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	10	--	°C
SWIRE						
SWIRE Logic High-Level Voltage	V_{SRH}	V_{IN} = 2.9V to 5.2V	1.2	--	--	V
SWIRE Logic Low-Level Voltage	V_{SRL}	V_{IN} = 2.9V to 5.2V	GND	--	0.4	V
SWIRE Pulldown Resistor	R_{SR}		200	500	900	kΩ

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWIRE Turn-off Detection Time	T_{off_dly}		300	--	--	µs
SWIRE Signal Stop Indicate Time	T_{stop}		300	--	--	µs
SWIRE Rising Time	t_r		--	--	200	ns
SWIRE Falling Time	t_f		--	--	200	ns
Clocked SWIRE High	T_{ON}		2	--	20	µs
Clocked SWIRE Low	T_{OFF}		2	--	20	µs
Input Clocked SWIRE Frequency	f_{SWIRE}		25	--	250	kHz
AVDDEN						
AVDD Enable Input Voltage	V_{IH}	V_{IN} = 2.9V to 5.2V	1.2	--	--	V
	V_{IL}	V_{IN} = 2.9V to 5.2V	GND	--	0.4	
Buck_Boost						
Positive Output Voltage Range	V_{OUT_RANGE}		3.5	--	4.2	V
Switching Frequency	f_{SW}		2.75	--	3.25	MHz
Over Current Protection	I_{OCP}		1.2	1.5	1.8	A
Negative Charge Pump						
Negative Output Voltage Range	V_{ON_RANGE}		–4.1	--	–0.7	V
Switching Frequency	f_{SW}		0.8	1	1.2	MHz
AVDD						
Positive Output Voltage Range	AVDD_RANGE		--	3.3	--	V
Positive Output Voltage Accuracy	AVDD_Acc	AVDD = 3.3V, AVDD = 3.3V I_{AVDD} = 0 to 10mA	–1	--	1	%
Output Current Capability	I_{AVDD}	V_{IN} = 2.9 to 5.2V, AVDD = 3.3V	10	--		mA
Line Regulation	V_{AVDD_LINE}	V_{IN} = 2.9 to 5.2V, I_{AVDD} = 10mA	–10	--	10	mV
Load Regulation	V_{AVDD_LOAD}	I_{AVDD} = 0 to 10mA	–10	--	10	mV
Output Ripple	V_{AVDD_RIPPLE}	AVDD = 3.3V, I_{AVDD} = 0 to 10mA	--	--	20	mV
Current Limit	I_{AVDD_LIMIT}		100	150	300	mA
Discharge Resistance	R_{AVDD_RDIS}		100	400	430	Ω
Short Circuit Protection	AVDD_SCP		75	80	92	%
OVDD						
Positive Output Voltage Range	V_{OVDD_RANGE}		2.8	3.3	4	V
Positive Output Voltage Accuracy	OVDD_Acc	OVDD = 3.3V, I_{OVDD} = 0mA to 10mA	–1	--	1	%
Output Current Capability	I_{OVDD}	V_{IN} = 2.9 to 5.2V, OVDD = 3.3V	50	--	--	mA

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	V_{OVDD_LINE}	V_{IN} = 2.9 to 5.2V, I_{OVDD} = 10mA	–10	--	10	mV
Load Regulation	V_{OVDD_LOAD}	I_{OVDD} = 0 to 10mA	–10	--	10	mV
Output Ripple	V_{OVDD_RIPPLE}	OVDD = 3.3V, I_{OVDD} = 0 to 10mA	--	--	10	mV
Current Limit	I_{OVDD_LIMIT}		100	150	300	mA
Discharge Resistance	R_{OVDD_RDIS}		100	400	430	Ω
Short Circuit Protection	OVDD_SCP		75	80	92	%
OVSS						
Negative Output Voltage Range	V_{OVSS_RANGE}		–4	–3.3	–0.6	V
Negative Output Voltage Accuracy	OVSS_Acc	OVSS = –3.3V, I_{OVSS} = 0mA to 10mA	–1	--	1	%
Output Current Capability	I_{OVSS}	V_{IN} = 2.9 to 5.2V, OVSS = –3.3V, Fly cap is 4.7μF & accuracy + / - 1%	50	--	--	mA
Line Regulation	V_{OVSS_LINE}	V_{IN} = 2.9 to 5.2V, I_{OVSS} = 10mA	–10	--	10	mV
Load Regulation	V_{OVSS_LOAD}	I_{OVSS} = 0 to 10mA	–10	--	10	mV
Output Ripple	V_{OVSS_RIPPLE}	OVSS = 3.3V, I_{OVDD} = 0 to 10mA	--	--	20	mV
Current Limit	I_{OVSS_LIMIT}		90	100	300	mA
Discharge Resistance	R_{OVSS_RDIS}		5	400	430	Ω
Short Circuit Protection	OVSS_SCP		75	80	92	%

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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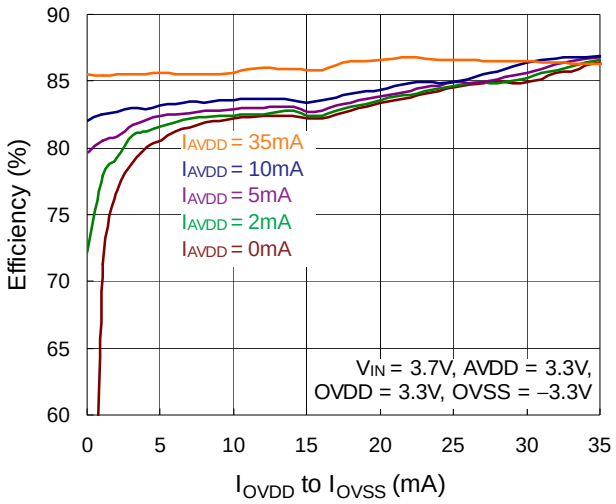
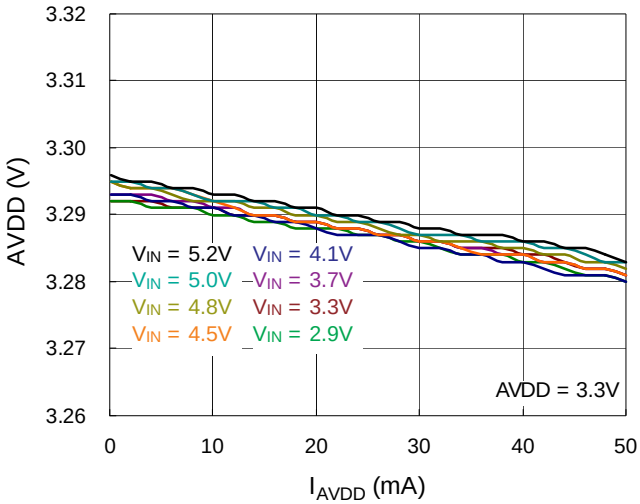
Typical Operating Characteristics

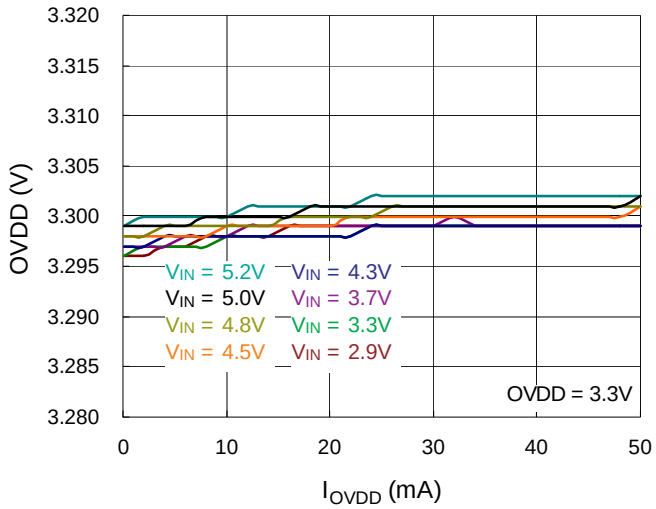
Efficiency vs. Output Current



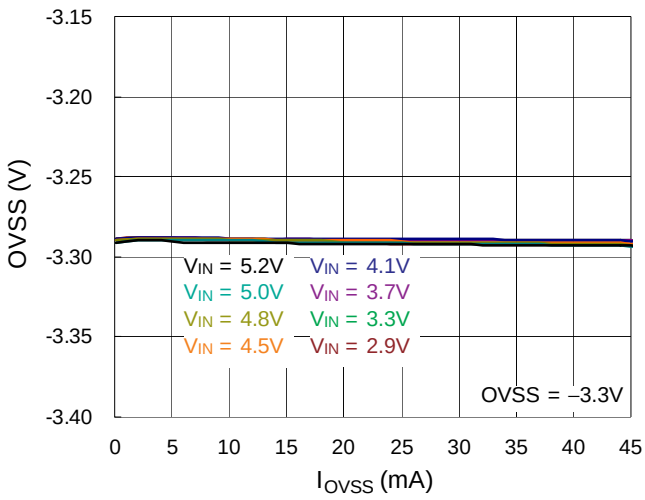
AVDD vs. Output Current



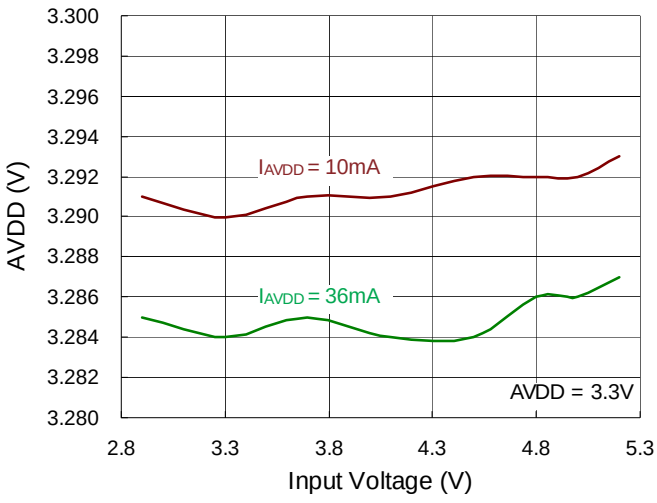
OVDD v.s Output Current



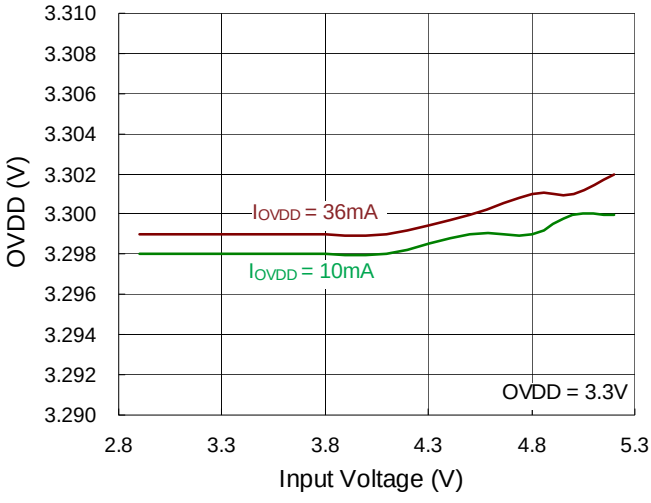
OVSS vs. Output Current



AVDD vs. Input Voltage



OVDD vs. Input Voltage



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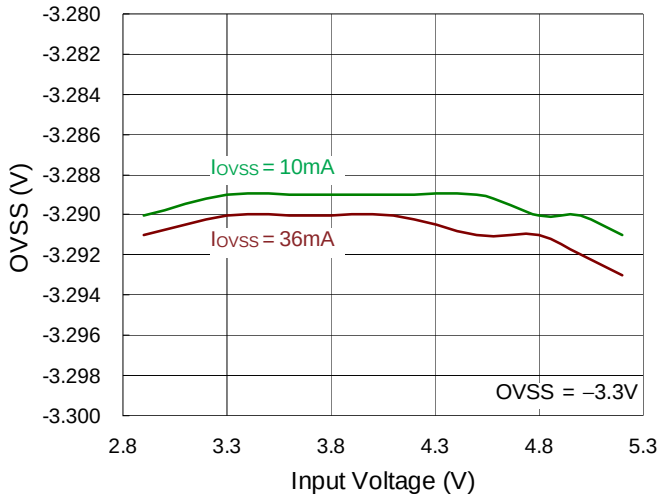
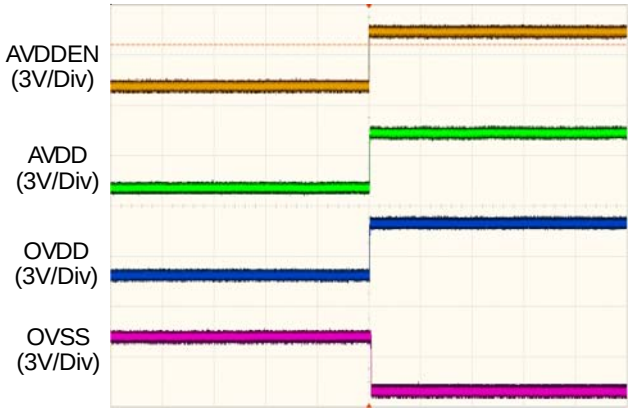
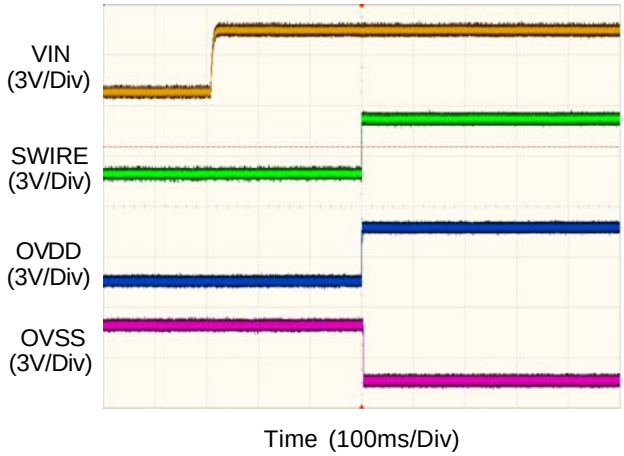
OVSS vs. Input Voltage



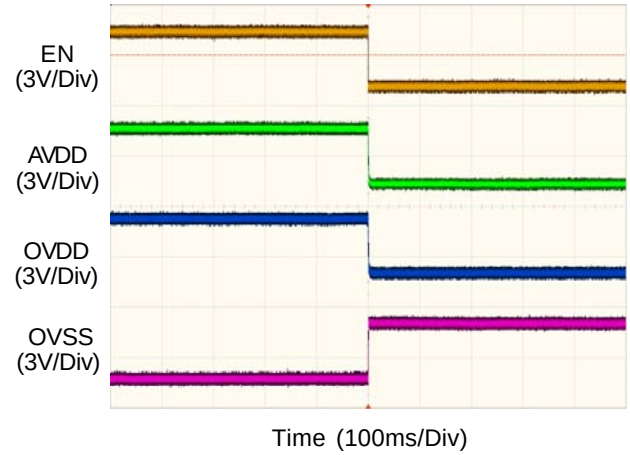
AVDDEN Power On



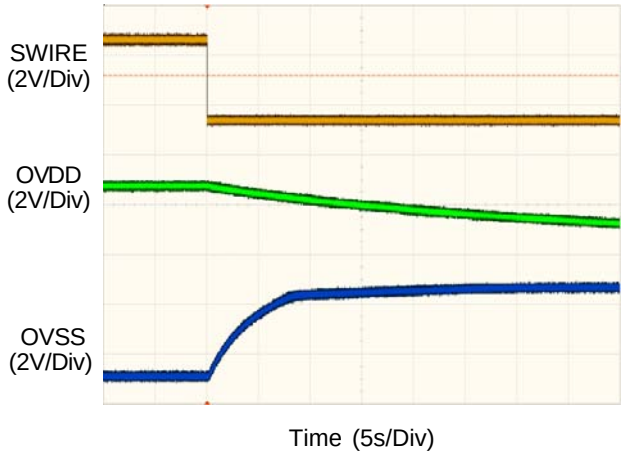
SWIRE Power On



AVDDEN Power Off



SWIRE Power Off



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Application Information

The RT4730 is a highly integrated power solution with Buck-Boost and inverting charge pump to generate positive and negative output voltage for AMOLED bias. The Buck-Boost DC-DC converter can operate with wide input voltage from 2.9V to 5.2V. The converter feedback loop is internally compensated for both Buck and Boost operation and it provides seamless transition between Buck and Boost modes operation.

Input Capacitor Selection

PVIN input ceramic capacitor with 4.7µF capacitance and AVIN input ceramic capacitor with 10µF capacitance is suggested for applications. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types are suitable because of their voltage and temperature ranges.

Inductor Selection

The recommended power inductor is 2.2µH. In applications, need to select an inductor with the low DCR to provide good performance and efficiency.

Output Capacitor Selection

The output capacitor selection determines the output voltage ripple and transient response. It is recommended to use ceramic capacitors placed as close as possible to output and GND pins of the IC.

Under Voltage Lockout

The prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included which shuts down IC operation when input voltage is lower than the specified threshold voltage.

Positive and Negative Output Voltage Setting

The positive and negative output voltage can be programmed by a MCU through the dedicated pin according to SWIRE pulse.

Over Current Protection

The RT4730 includes a cycle-by-cycle current limit function which monitor the inductor current during each ON period. The power switch will be forced off to avoid large current damage once the current is over the limit level.

Short Circuit Protection

The RT4730 has an advanced output short-circuit protection mechanism which prevents the IC from damage by unexpected application. When the output becomes shorted to ground, and the output voltage is under the limit level, the IC enters shutdown mode and can only re-start normal operation after re-power on.

Over Temperature Protection

The RT4730 equips an over temperature protection circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down the bias operation when ambient temperature exceeds 140°C. Once the ambient temperature cools down by approximately 10°C, IC will automatically resume normal operation. To maintain continuous operation, the maximum junction temperature should be prevented from rising above 130°C.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-16B 2.34 x 2.34 (BSC), the thermal resistance, θ_{JA}, is 42.3°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (42.3°C/W) = 2.36W for a WL-CSP-16B 2.34 x 2.34 (BSC) package.

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The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

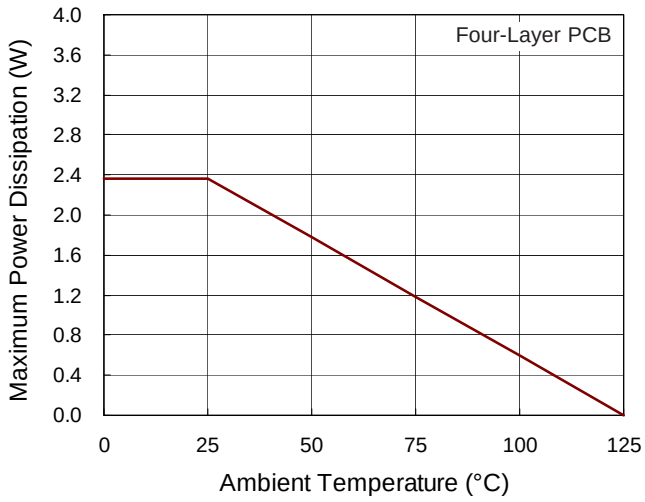

Figure 1. Derating Curve of Maximum Power Dissipation

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SWIRE Setting

Pulse	Function Description
0	Default value: OVDD = 3.3V, OVSS = –3.3V
116	OVDD is turned on
117	VON/OVSS is turned on
118	OVDD is turned off
119	VON/OVSS is turned off
120	VON/OVSS discharge to GND, with slow slew rate then enter high impendance state
121	Soft-reset, clear all setting and back to default state
10-22	OVDD setting (2.8V to 4V)
58-92	OVSS setting (–4V to –0.6V)

Pulse	VOUT	OVDD
10	3.5	2.8
11	3.5	2.9
12	3.5	3
13	3.5	3.1
14	3.5	3.2
15	3.5	3.3
16	3.6	3.4
17	3.7	3.5
18	3.8	3.6
19	3.9	3.7
20	4	3.8
21	4.1	3.9
22	4.2	4

Pulse	VON	OVSS	Pulse	VON	OVSS
58	-4.1	-4	76	-2.3	-2.2
59	-4	-3.9	77	-2.2	-2.1
60	-3.9	-3.8	78	-2.1	-2
61	-3.8	-3.7	79	-2	-1.9
62	-3.7	-3.6	80	-1.9	-1.8
63	-3.6	-3.5	81	-1.8	-1.7
64	-3.5	-3.4	82	-1.7	-1.6
65	-3.4	-3.3	83	-1.6	-1.5
66	-3.3	-3.2	84	-1.5	-1.4
67	-3.2	-3.1	85	-1.4	-1.3
68	-3.1	-3	86	-1.3	-1.2
69	-3	-2.9	87	-1.2	-1.1
70	-2.9	-2.8	88	-1.1	-1
71	-2.8	-2.7	89	-1	-0.9
72	-2.7	-2.6	90	-0.9	-0.8
73	-2.6	-2.5	91	-0.8	-0.7
74	-2.5	-2.4	92	-0.7	-0.6
75	-2.4	-2.3			

VOUT = MAX(AVDD, OVDD, |OVSS|) + 0.2V

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Layout Considerations

For the best performance of the RT4730, the following PCB layout guidelines should be strictly followed.

- For good regulation, place the power component as close to the IC as possible. The traces should be wide and short especially for the high current output loop.
- The input and output bypass capacitor should be placed as close the IC as possible and connected to the ground plane of the PCB.
- The flying capacitor should be placed as close to the C1P/C1N pin as possible to avoid noise injection.
- The inductor should be placed as close to LX1 and LX2 pin for reducing EMI.
- Minimize the size of the LX1 and LX2 and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near LX1 and LX2

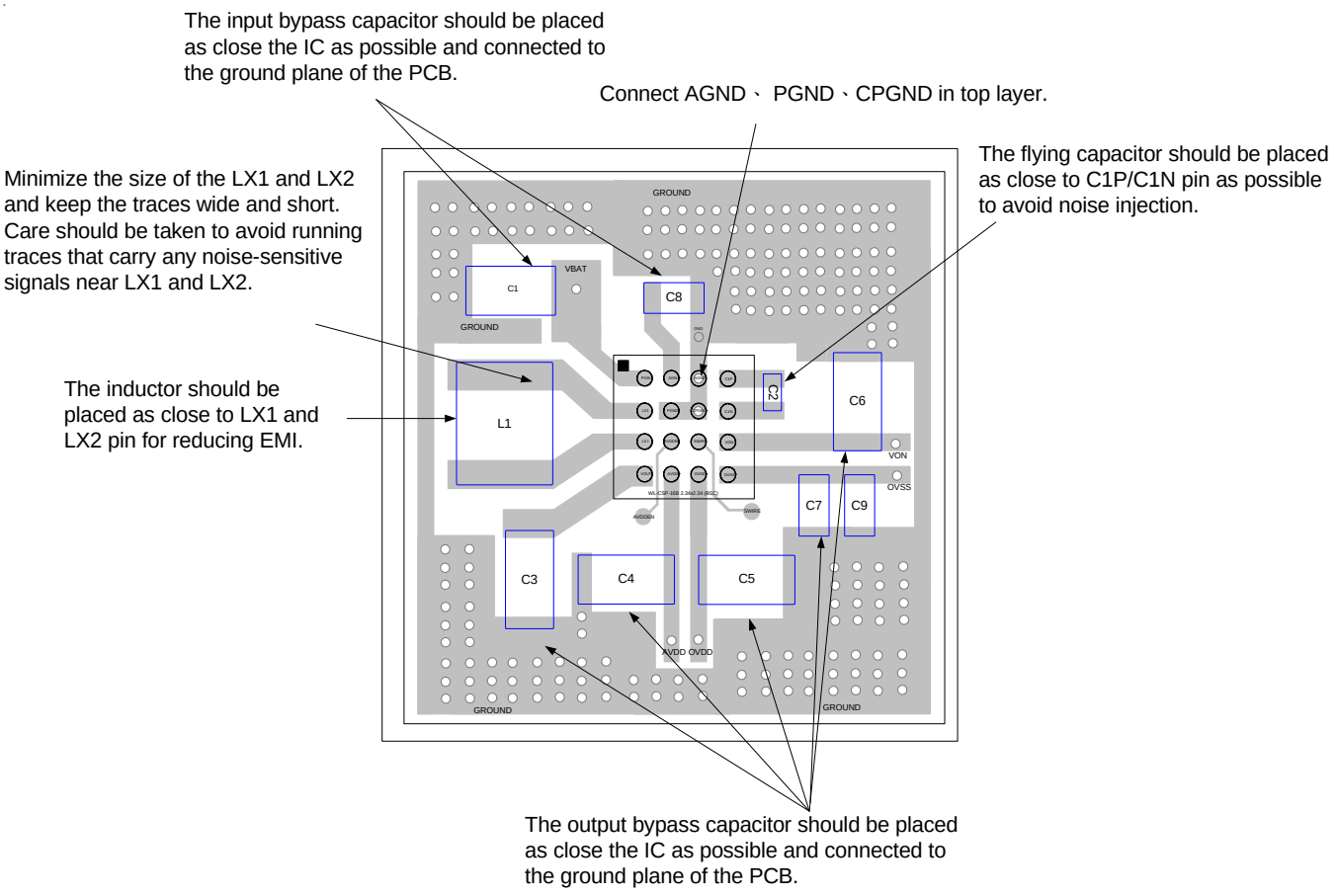

Figure 2. PCB Layout Guide

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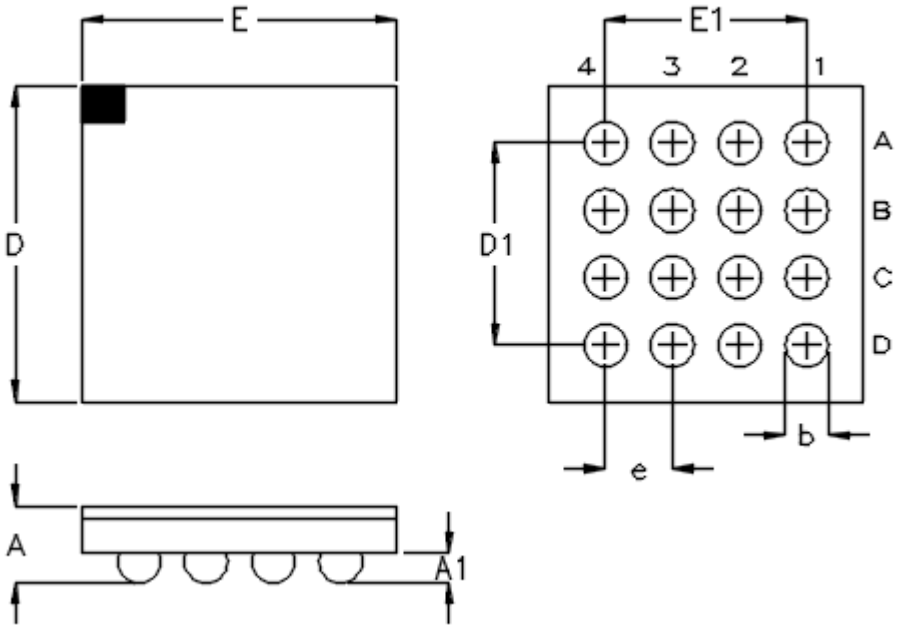
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.525	0.625	0.021	0.025
A1	0.200	0.260	0.008	0.010
b	0.290	0.350	0.011	0.014
D	2.300	2.380	0.091	0.094
D1	1.500		0.059	
E	2.300	2.380	0.091	0.094
E1	1.500		0.059	
e	0.500		0.020	

16B WL-CSP 2.34x2.34 Package (BSC)

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