



ON Semiconductor®

<http://onsemi.com>

LV5693P

Bi-CMOS IC

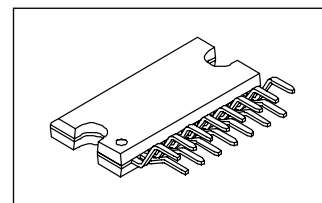
System Power Supply IC for Automotive Infotainment Multiple Output Linear Voltage Regulator

Overview

The LV5693P is a multiple output linear regulator IC, which allows reduction of quiescent current. The LV5693P is specifically designed to address automotive infotainment systems power supply requirements. The LV5693P integrates 5 linear regulator outputs, a linear regulator controller which gives USB supply with external P-channel FET, a high side power switch, over current protection, overvoltage protection and thermal shutdown circuitry.

Function

- Five channel regulator and one channel P-FET pre-driver (for USB-power)
 - For VDD: V_{OUT} is 5.7V, I_{Omax} is 300mA
 - For DSP: V_{OUT} is 3.3V, I_{Omax} is 300mA
 - For CD: V_{OUT} is 8.0V, I_{Omax} is 1300mA
 - For illumination: V_{OUT} is 8.4V, I_{Omax} is 500mA
 - For audio systems: V_{OUT} is 8.4V, I_{Omax} is 500mA
 - For USB (controller) :
 - V_{OUT} is flexible (configurable with external resistor),
 - I_{Omax} is 1000mA
- High side switch: Voltage difference between input and output is 0.5V, I_{Omax} is 500mA
- Over current protector
- Overvoltage protector (Without V_{DD-OUT}) Clamp voltage is 21V (typical)
- Thermal Shut down 175°C (typical)
- Quiescent current 50 μ A (Typ. when only VDD is in operation)



HZIP15J

(Warning) The protector functions only improve the IC's tolerance and they do not guarantee the safety of the IC if used under the conditions out of safety range or ratings. Use of the IC such as use under over current protection range or thermal shutdown state may degrade the IC's reliability and eventually damage the IC.

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

LV5693P

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC} max		36	V
Power dissipation	P_d max	IC unit	$T_a \leq 25^\circ\text{C}$	1.5
		At using Al heat sink		5.6
		At infinity heat sink		32.5
Peak voltage	V_{CC} peak	Regarding Bias wave, refer to below the	50	V
Junction temperature	T_j max		150	$^\circ\text{C}$
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Conditions	Ratings	Unit
Power supply voltage rating 1	V_{DD} output ON, DSP output ON	7.7 to 16	V
Power supply voltage rating 2	ILM output ON	10.8 to 16	V
Power supply voltage rating 3	Audio output ON, CD output ON	10 to 16	V

* V_{CC1} should be as follows: $V_{CC1} > V_{CC} - 0.7\text{V}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = V_{CC1} = 14.4\text{V}$ (*2)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC}	V_{DD} no load, CTRL1/2/3 = $\lceil L/L/L \rceil$		50	100	μA
CTRL1 Input						
Low input voltage	V_{IL1}		0		0.3	V
Middle input voltage	V_{IM1}		1.1	1.65	2.1	V
High input voltage	V_{IH1}		2.5		5.5	V
Input impedance	R_{IH1}		280	400	520	$\text{k}\Omega$
CTRL2 Input						
Low input voltage	V_{IL2}		0		0.3	V
Middle1 input voltage	V_{IM12}		0.8	1.06	1.4	V
Middle2 input voltage	V_{IM22}		1.9	2.13	2.4	V
High input voltage	V_{IH2}		2.9	3.2	5.5	V
Input impedance	R_{IH2}		280	400	520	$\text{k}\Omega$
CTRL3 input.						
Low input voltage	V_{IL3}		0		0.3	V
High input voltage	V_{IH3}		2.5		5.5	V
Input impedance	R_{IH3}		280	400	520	$\text{k}\Omega$
$V_{DD}5.7\text{V}$ output						
Output voltage	V_{O1}	$I_{O1} = 200\text{mA}$	5.415	5.7	5.985	V
Output current	I_{O1}	$V_{O1} \geq 5.35\text{V}$	300			mA
Line regulation	ΔV_{OLN1}	$8.2\text{V} < V_{CC1} < 16\text{V}$, $I_{O1} = 200\text{mA}$		30	100	mV
Load regulation	ΔV_{OLD1}	$1\text{mA} < I_{O1} < 200\text{mA}$		70	150	mV
Dropout voltage 1	V_{DROP1}	$I_{O1} = 400\text{mA}$		0.5	1.2	V
Dropout voltage 2	V_{DROP1}'	$I_{O1} = 200\text{mA}$		0.25	0.6	V
Ripple rejection	R_{REJ1}	$f = 120\text{Hz}$, $I_{O1} = 200\text{mA}$	30	40		dB

Continued on next page.

LV5693P

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
USB output: CTRL3 = [H] (When external power FET 2SJ650, it external resists 27kΩ, and 9.1kΩ is set)						
USB output voltage	V _{O2}	I _{O2} = 1000mA	4.75	5	5.25	V
USB output current	I _{O2}	V _{O2} ≥ 4.75V	1000			mA
Line regulation	ΔV _{OLN2}	10V < V _{CC} < 16V, I _{O2} = 1000mA		50	90	mV
Load regulation	ΔV _{OLD2}	10mA < I _{O2} < 1000mA		100	150	mV
Dropout voltage	V _{DROP2}	I _{O2} = 1000mA		1.0	1.5	V
Ripple rejection	R _{REJ1}	f = 120Hz, I _{O2} = 1000mA	40	50		dB
AUDIO (8.4V) Output ; CTRL1 = [M or H]						
AUDIO output voltage 1	V _{O3}	I _{O3} = 400mA	8.0	8.4	8.8	V
AUDIO output current	I _{O3}	V _{O3} ≥ 8.0V	500			mA
Line regulation	ΔV _{OLN3}	10V < V _{CC} < 16V, I _{O3} = 400mA		30	90	mV
Load regulation	ΔV _{OLD3}	1mA < I _{O3} < 400mA		70	150	mV
Dropout voltage 1	V _{DROP3}	I _{O3} = 400mA		0.4	0.8	V
Dropout voltage 2	V _{DROP3'}	I _{O3} = 200mA		0.2	0.4	V
Ripple rejection	R _{REJ3}	f = 120Hz, I _{O3} = 400mA	40	50		dB
ILM (8.4V) Output ; CTRL2 = [M1 or H]						
ILM output voltage	V _{O4}	I _{O4} = 400mA	8.0	8.4	8.8	V
ILM output current	I _{O4}		500			mA
Line regulation	ΔV _{OLN4}	10.8V < V _{CC} < 16V, I _{O4} = 400mA		30	90	mV
Load regulation	ΔV _{OLD4}	1mA < I _{O4} < 400mA		70	150	mV
Dropout voltage 1	V _{DROP4}	I _{O4} = 400mA		1.0	1.5	V
Dropout voltage 2	V _{DROP4'}	I _{O4} = 200mA		0.7	1.05	V
Ripple rejection	R _{REJ4}	f = 120Hz, I _{O4} = 400mA	40	50		dB
AMP_HS-SW; CTRL2 = [M2 or H]						
Output voltage	V _{O5}	I _{O5} = 500mA	V _{CC} -1.0	V _{CC} -0.5		V
Output current	I _{O5}	V _{O5} ≤ V _{CC} -1.0	350			mA
DSP(3.3V output); CTRL1 = [M or H]						
DSP output voltage	V _{O7}	I _{O7} = 200mA	3.1	3.3	3.5	V
DSP output current	I _{O7}		300			mA
Line regulation	ΔV _{OLN7}	10V < V _{CC} < 16V, I _{O7} = 200mA		30	90	mV
Load regulation	ΔV _{OLD7}	1mA < I _{O7} < 200mA		70	150	mV
Ripple rejection	R _{REJ7}	f = 120Hz, I _{O7} = 200mA	40	50		dB
CD(8.0V output); CTRL1 = [H]						
CD output voltage	V _{O8}	I _{O8} = 1000mA	7.6	8.0	8.4	V
CD output current	I _{O8}		1300			mA
Line regulation	ΔV _{OLN8}	10.5V < V _{CC} < 16V, I _{O8} = 1000mA		50	100	mV
Load regulation	ΔV _{OLD8}	10mA < I _{O8} < 1000mA		100	200	mV
Dropout voltage	V _{DROP8}	I _{O8} = 1000mA		1.0	1.5	V
Ripple rejection	R _{REJ8}	f = 120Hz, I _{O8} = 1000mA	40	50		dB

*2: The entire specification has been defined based on the tests performed under the conditions where T_j and T_a (=25°C) are almost equal. There tests were performed with pulse load to minimize the increase of junction temperature (T_j).

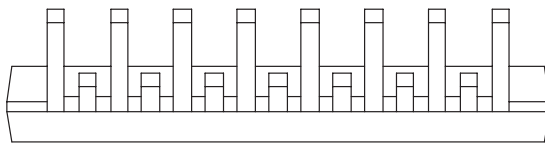
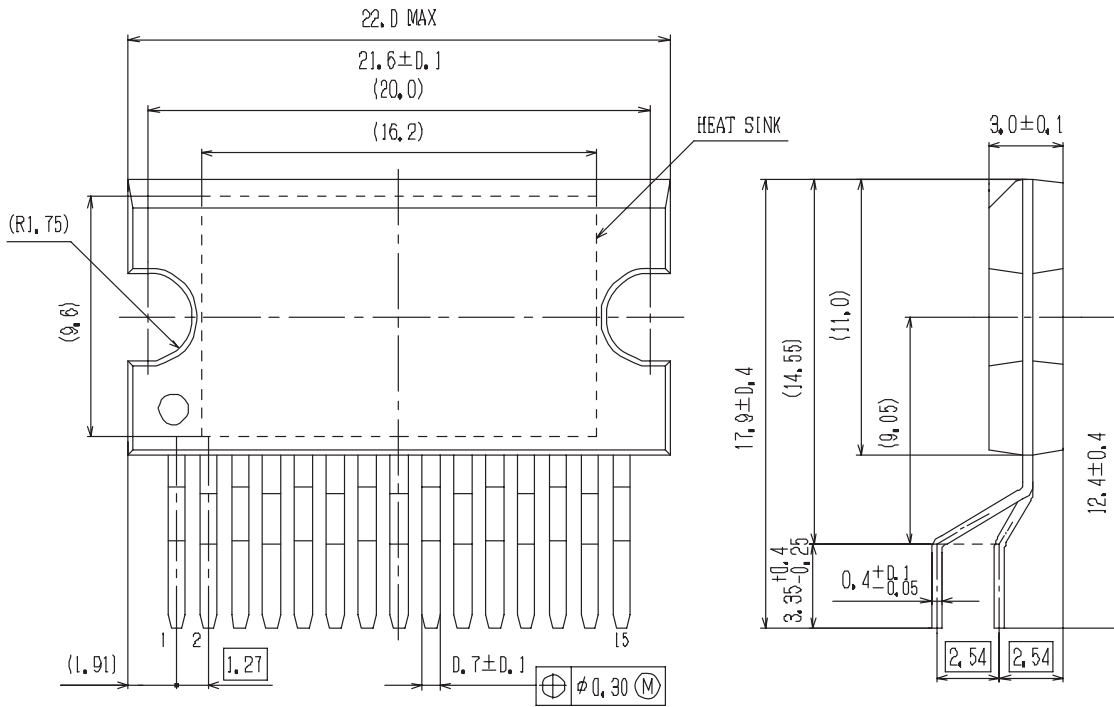
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

LV5693P

Package Dimensions

unit : mm

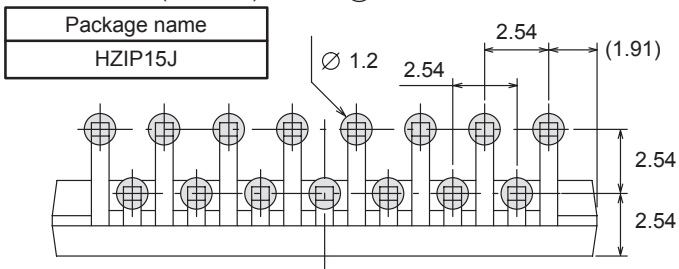
HZIP15J
CASE 945AC
ISSUE A



SOLDERING FOOTPRINT*

(Unit: mm)

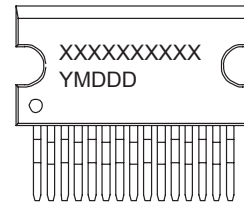
○ Through Hole Area



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

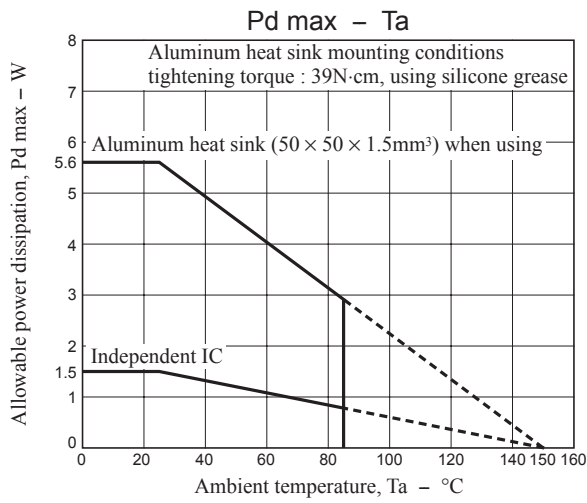
GENERIC MARKING DIAGRAM*



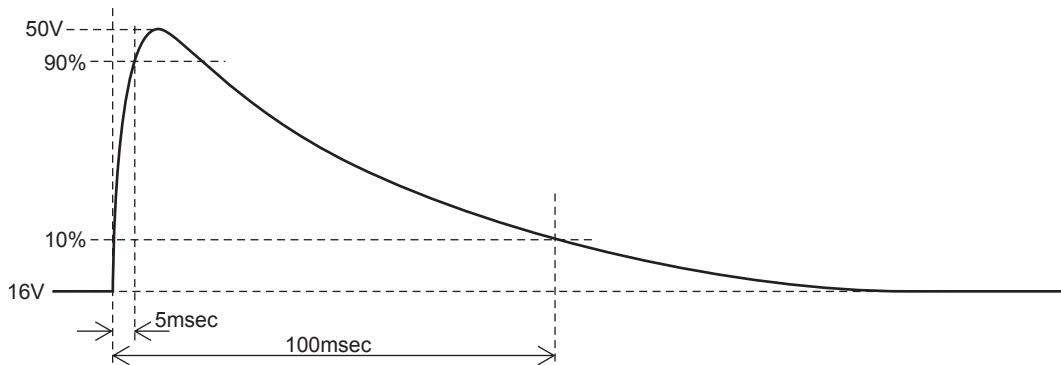
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

- Allowable power dissipation derating curve



- Waveform applied during surge test



CTRL Pin Output Truth Table

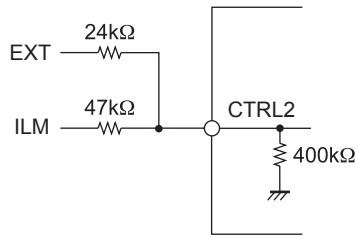
CTRL1	CD	DSP	AUDIO
L	OFF	OFF	OFF
M	OFF	ON	ON
H	ON	ON	ON

CTRL3	USB
L	OFF
H	ON

CTRL2	EXT	ILM
L	OFF	OFF
M1	OFF	ON
M2	ON	OFF
H	ON	ON

LV5693P

Example of CTRL2 application circuit



EXT	ILM	CTRL2
0V	0V	0V
0V	3.3V	1.06V
3.3V	0V	2.13V
3.3V	3.3V	3.20V

note) The control terminal is input 3.3V correspondence. Please set it by the input resistance at 5V input.

(Warning) Usage of CTRL2

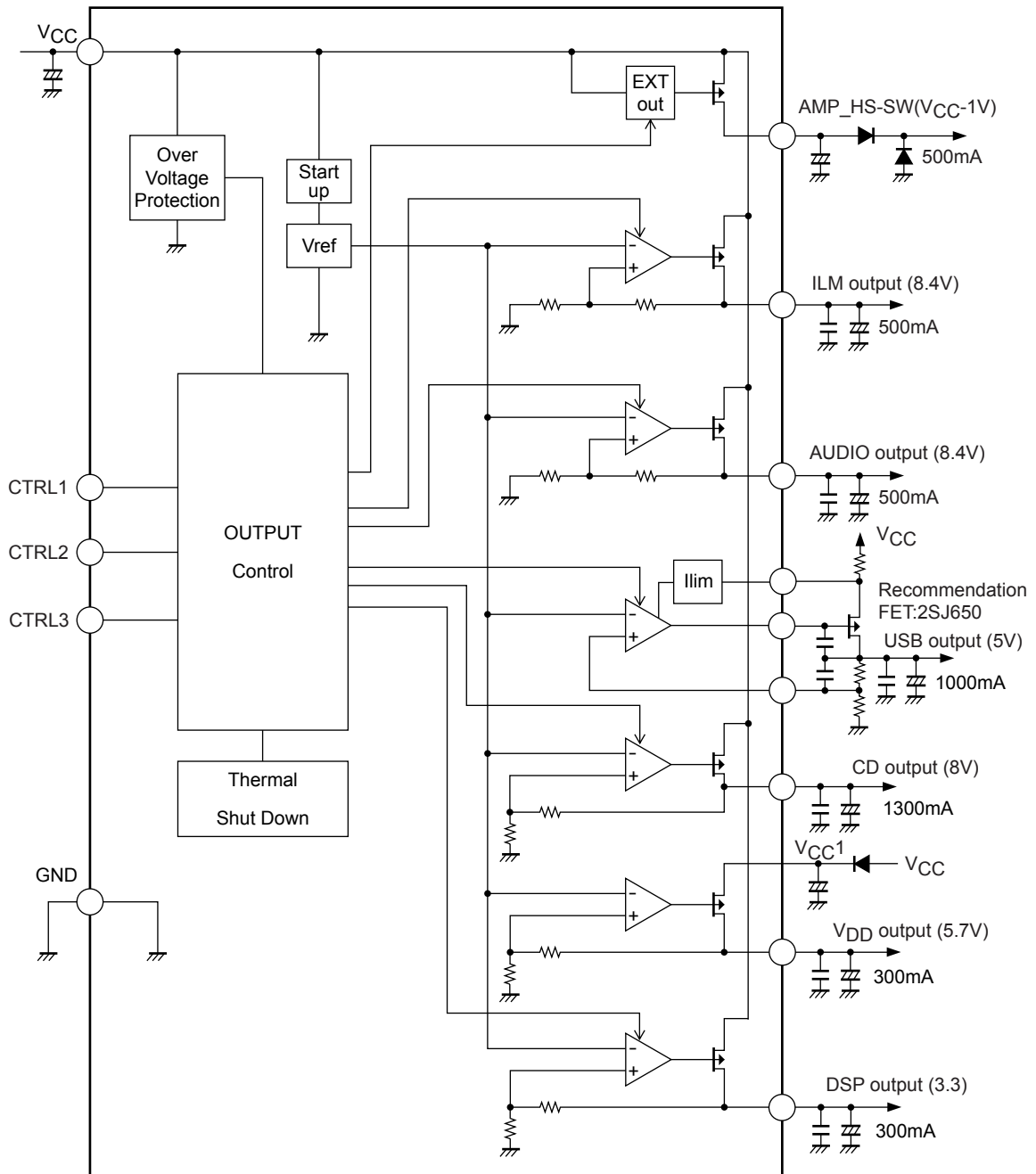
When CTRL pin transits between L and M2, since it passes M1, ILM is turned on for a moment. Likewise, when CTRL pin transits between H and M1, since it passes M2, ILM is turned off for a moment.

To avoid operation failure by the above factors, please refer to the following precautions.

- Do not connect parasitic capacitor to CTRL as much as possible.
- If use of capacitor for CTRL is required, keep the resistance value as low as possible.
- Make sure that the output load capacitor has enough margin against the voltage fluctuation due to instantaneous ON/OFF.

LV5693P

● Block Diagram



LV5693P

Pin Function

Pin No.	Pin name	Description	Equivalent Circuit
1	ILM	ILM output pin ON when CTRL2 = M1, H 8.4V/0.5A	
2	GND	GND pin	
3	CD	CD output pin ON when CTRL1 = H 8.0V/1.3A	
4	CTRL1	CTRL1 input pin Three value input	
5	AUDIO	AUDIO output pin ON when CTRL1 = M, H 8.4V/0.5A	

Continued on next page.

LV5693P

Continued from preceding page.

Pin No.	Pin name	Description	Equivalent Circuit
6	CTRL2	CTRL2 input pin Four-value input	
7	DSP	DSP output pin ON when CTRL1 = M, H 3.3V/0.3A	
8	CTRL3	CTRL3 input pin Two-value input	
9	FB	USB-FB pin 1.26V	

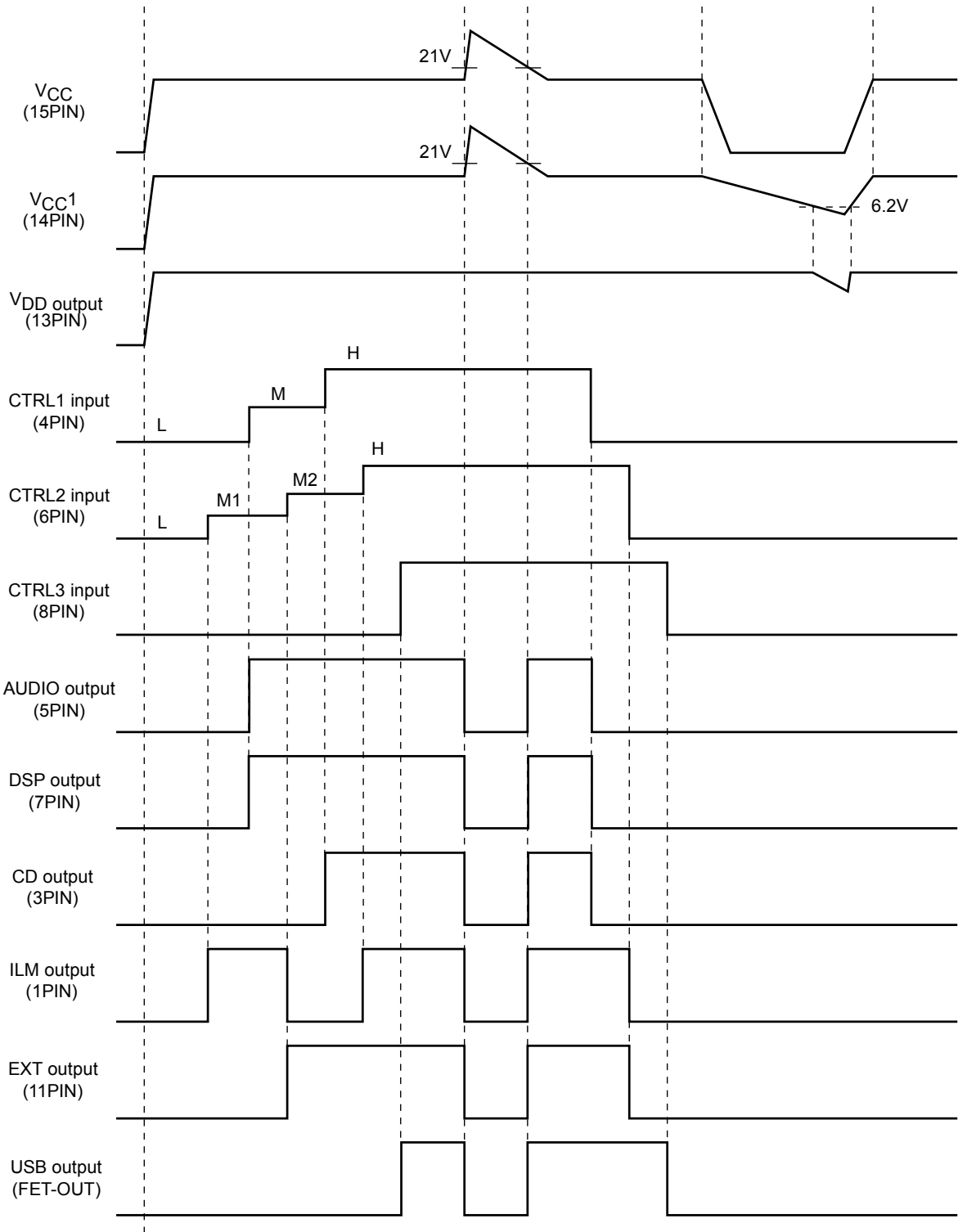
Continued on next page.

LV5693P

Continued from preceding page.

Pin No.	Pin name	Description	Equivalent Circuit
10	USBGT	Pch-FET gate connect pin 12.0V	
11	EXT	EXT output pin ON when CTRL2 = M2, H V _{CC} -0.5V/500mA	
12	RSNS	USB current detection resistance connection pin 14.3V	
13	V _{DD}	V _{DD} output pin 5.7V/0.3A	
14	V _{CC1}	V _{DD} power supply pin	
15	V _{CC}	Power supply pin	

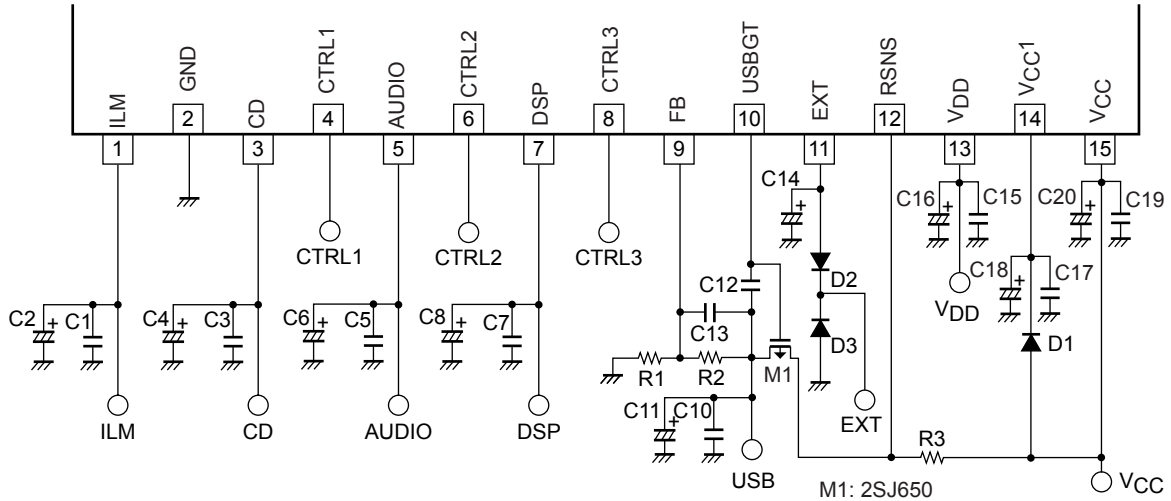
Timing Chart



*Usage condition: Use under typical value.

LV5693P

Recommended Operation Circuit



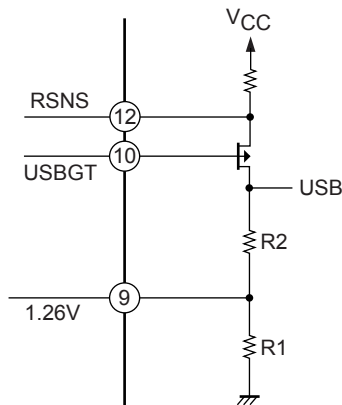
Peripheral parts list

Name of part	Description	Recommended value	Remarks
C2, C4, C6, C8, C11, C16	Output stabilization capacitor	10 μ F or more*	Electrolytic capacitor
C1, C3, C5, C7, C10, C15	Output stabilization capacitor	0.22 μ F or more*	Ceramic capacitor
C12, C13	Capacity for phase amends	C12=1000pF (C13=0pF: TBD)	Ceramic capacitor
C18, C20	Power supply bypass capacitor	100 μ F or more	These capacitors must be placed near the V _{CC} and GND pins.
C17, C19	Oscillation prevention capacitor	0.22 μ F or more	
C14	EXT output stabilization capacitor	2.2 μ F or more	
R1, R2	Resistor for ILM voltage adjustment	R1/R2=9.1k Ω /27k Ω for 5.0V	A resistor with resistance accuracy as low as less than $\pm 1\%$ must be used.
R3	Resistor for AUDIO voltage setting	0.1 Ω for I _{peak} =3A	Panasonic ERJB1CFR10U(Reference)
M1	USB output Pch-FET	2SJ650	
D1	Diode for prevention of backflow		
D2, D3	Diode for internal element protection	SB1003M3	

note)The circuit diagram and the values are only tentative which are subject to change.

* : Make sure that the capacitors of the output pins are 10 μ F or higher and ESR is 10 Ω or lower in total and temperature characteristics and accuracy are taken into consideration. Also the E-cap should have good high frequency characteristics.

• USB output voltage setting method



Formula for USB voltage calculation

$$USB = \frac{1.26[V]}{R_1} \times R_2 + 1.26[V]$$

$$\frac{R_2}{R_1} = \frac{(USB-1.26)}{1.26}$$

Please design so that the ratio of R1 and R2 may fill the above-mentioned expression for the set USB voltage.

$$\frac{R_2}{R_1} = \frac{(5.0-1.26)}{1.26} \cong 2.968$$

$$\frac{R_2}{R_1} = \frac{27k\Omega}{9.1k\Omega} \cong 2.967$$

The FB voltage is determined by the internal band gap voltage of the IC (typ = 1.26V)

$$USB = 1.26V \times 2.967 + 1.26V \cong 4.998V$$

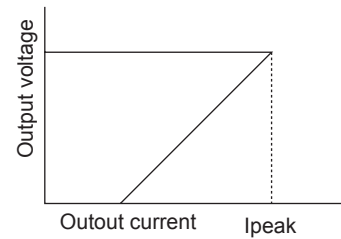
LV5693P

- How to set USB overcurrent limit value (OCP)

OCP of the USB works when the voltage of RSNS is under $V_{CC}-0.3V$. The peak current value of OCP is calculated as follows: $I_{peak}(A) = 0.3/R3$. (ex.) $R3=0.1\Omega \rightarrow I_{peak}=3A$

- Since this IC does not detect the heat generation of the external FET, keep the temperature of the FET as low as possible so as not to exceed the ratings.
- Recommended FET: 2SJ650.

(note)The above values were obtained under typical conditions. The values may fluctuate in manufacturing processes due to external resistor and IC variation.



- Warning

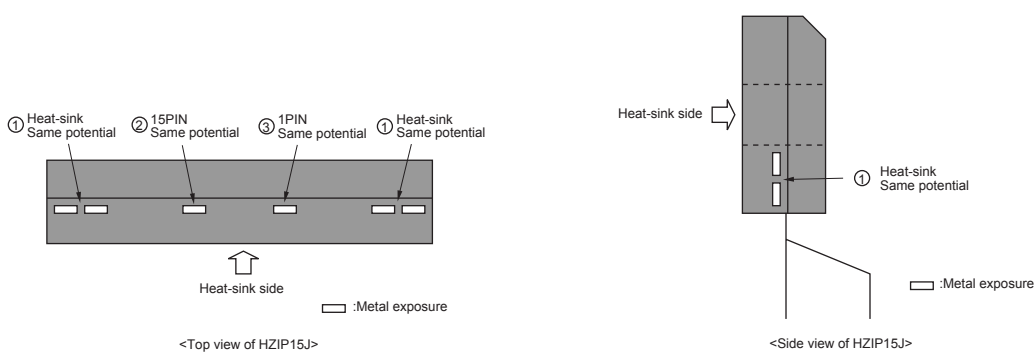
The internal circuit of USBGT and RSNS consist of components that support 5V. Do not bias 7V or above between V_{CC} and these pins to prevent the IC from destruction. Do not use the device under overvoltage condition (for example shorting these terminals to low voltage node) even for short period of time .

In normal operating condition with recommended application, the device controls voltage of these terminals within 5V.

Caution for implementing LV5693P to a system board

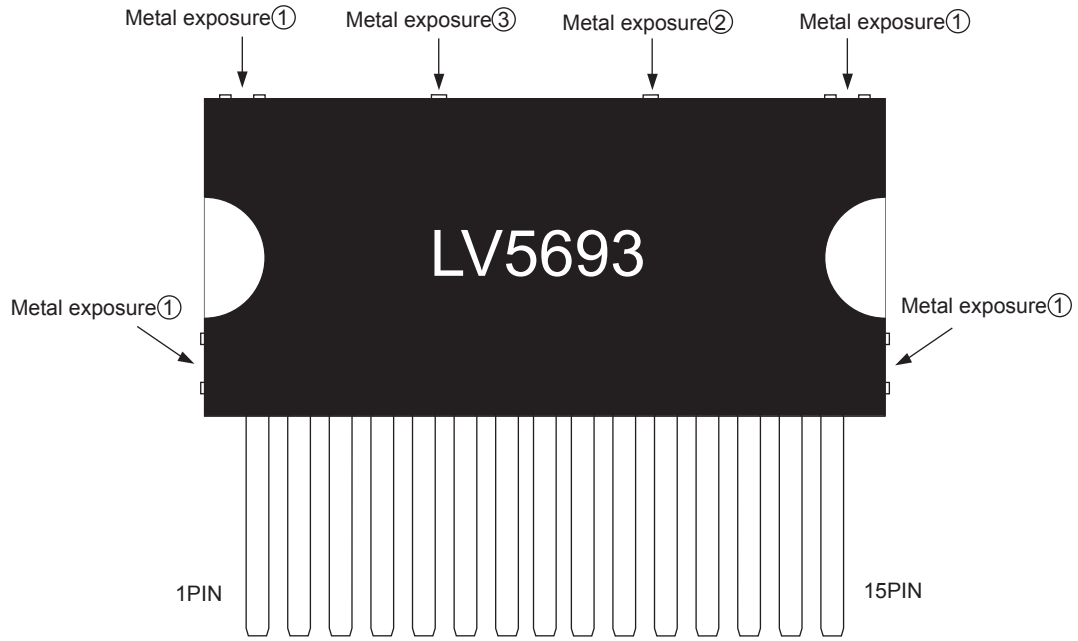
The package of LV5693P is HZIP15J which has some metal exposures other than connection pins and heatsink as shown in the diagram below. The electrical potentials of (2) and (3) are the same as those of pin 15 and pin 1, respectively. (2) (=pin 15) is the V_{CC} pin and (3) (=pin 1) is the ILM (regulator) output pin. When you implement the IC to the set board, make sure that the bolts and the heatsink are out of touch from (2) and (3). If the metal exposures touch the bolts which has the same electrical potential with GND, GND short occurs in ILM output and V_{CC} . The exposures of (1) are connected to heatsink which has the same electrical potential with substrate of the IC chip (GND). Therefore, (1) and GND electrical potential of the set board can connect each other.

- HZIP15J outline



LV5693P

- Frame diagram (LV5693P) *In the system power supply other than LV5693P, pin assignment may differ.



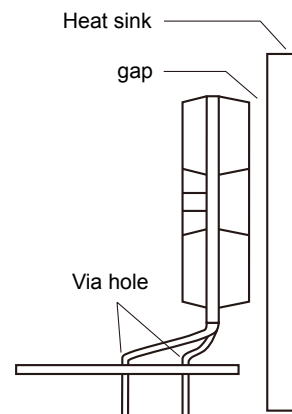
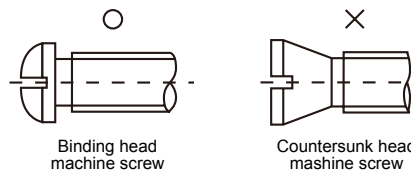
HZIP15J Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the heat generated by the device to the outer environment and dissipating that heat.

- a. Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

b. Heat sink attachment

- Use flat-head screws to attach heat sinks.
- Use also washer to protect the package.
- Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
- If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
- Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Take care a position of via hole .
- Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
- Verify that there are no press burrs or screw-hole burrs on the heat sink.
- Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
- Twisting must be limited to under 0.05 mm.
- Heat sink and semiconductor device are mounted in parallel.
- Take care of electric or compressed air drivers
- The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.



c. Silicone grease

- Spread the silicone grease evenly when mounting heat sinks.
- Our company recommends YG-6260 (Momentive Performance Materials Japan LLC)

d. Mount

- First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
- When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

e. When mounting the semiconductor device to the heat sink using jigs, etc.,

- Take care not to allow the device to ride onto the jig or positioning dowel.
- Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

f. Heat sink screw holes

- Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
- When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
- When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

- g. There is a method to mount the semiconductor device to the heat sink by using a spring band. But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.

LV5693P

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5693P-E	HZIP15J (Pb-Free)	20 / Fan-Fold

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.