

9-Line Low Capacitance SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 and SPI-2 Standards
- 5pF Channel Capacitance during Disconnect
- Meets SCSI Hot Plugging
- -400mA Sourcing Current for Termination
- +100mA Sinking Current for Active Negation
- 1V Dropout Voltage Regulator
- Logic High Command Disconnects all Termination Lines
- 100µA Supply Current in Disconnect Mode
- Trimmed Termination Current to 5%
- Trimmed Impedance to 5%
- Low Thermal Resistance Surface Mount Packages

DESCRIPTION

The UC5612 provides 9 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

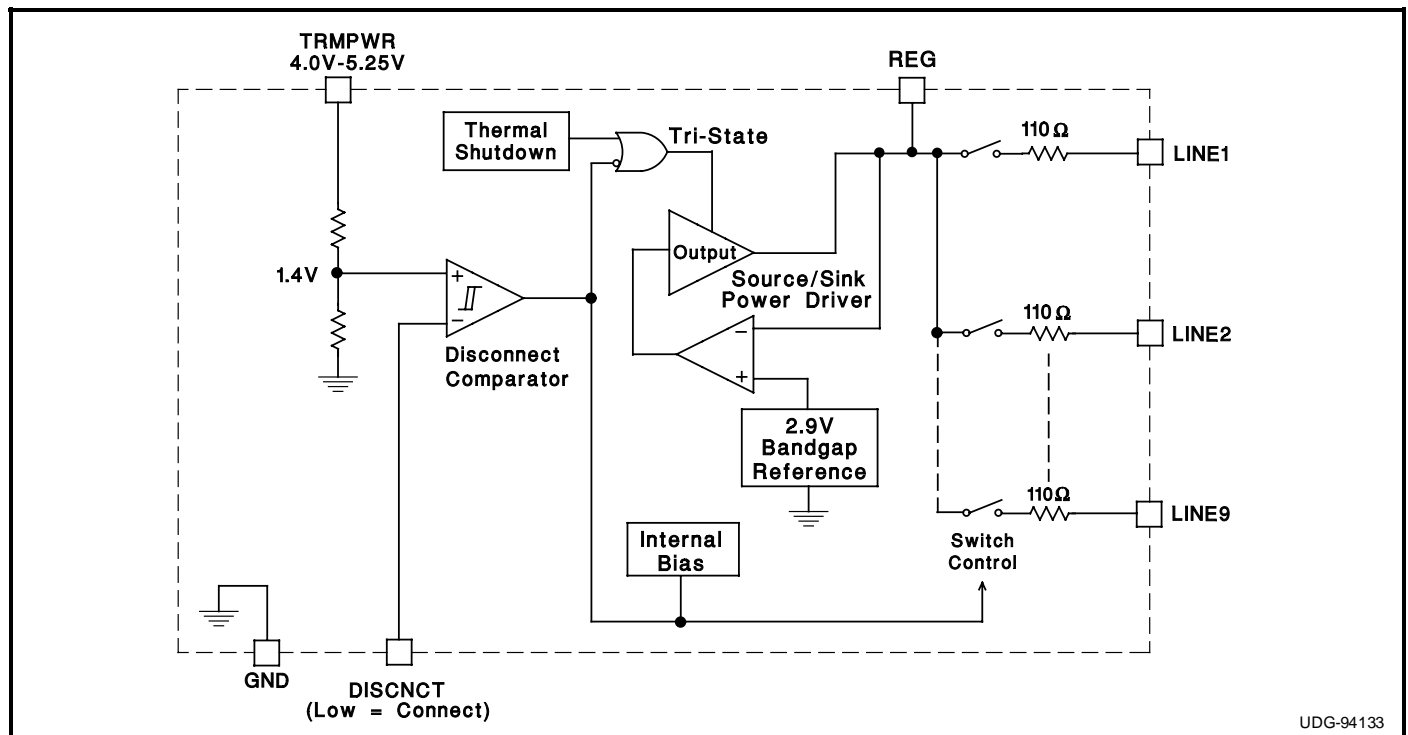
The only functional differences between the UC5603 and UC5612 is the absence of the negative clamps on the output lines. Parametrically, the UC5612 has a 5% tolerance on impedance and current compared to a 3% tolerance on the UC5603. Custom power packages are utilized to allow normal operation at full power (2 Watts).

The UC5612 provides a disconnect feature which, when opened or driven high, disconnects all terminating resistors, disables the regulator and greatly reduces standby power consumption. The output channels remain high impedance even without *Termpwr* applied. A low channel capacitance of 5pF allows interim points of the bus to have little to no effect on the signal integrity.

Internal circuit trimming is utilized, first to trim the impedance to a 5% tolerance, and then most importantly, to trim the output current to a 5% tolerance, as close to the maximum SCSI specification as possible. This maximizes the noise margin in fast SCSI operation. Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16 pin narrow body SOIC, 16 pin ZIP (zig-zag in line package) and 24 pin TSSOP.

BLOCK DIAGRAM



UDG-94133

Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Tempwr Voltage	+7V
Signal Line Voltage.....	0V to +7V
Regulator Output Current	0.6A
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 Sec.).....	+300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

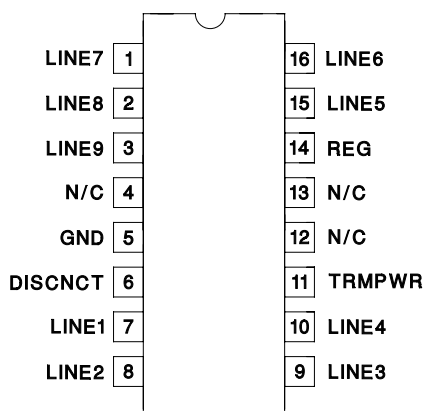
Consult Packaging Section of Unitrode Integrated Circuits data-book for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

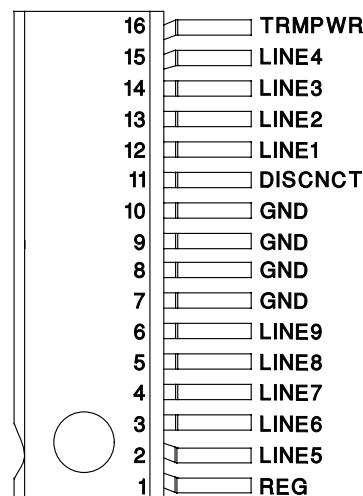
Tempwr Voltage	3.8V to 5.25V
Signal Line Voltage.....	0V to +5V
Disconnect Input Voltage	0V to Tempwr

CONNECTION DIAGRAMS

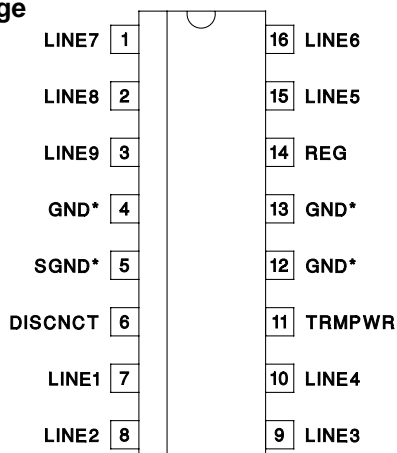
DIL-16 (Top View)
N or J Package



ZIP-16 (Top View)
Z Package

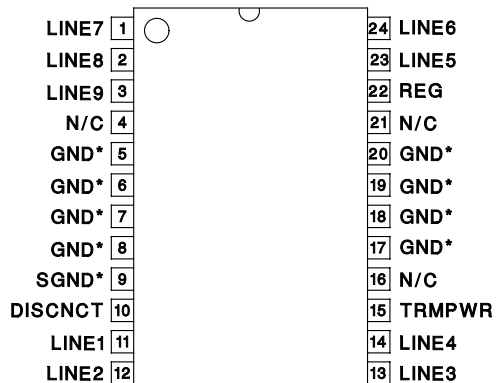


SOIC-16 (Top View)
DP Package



* DP package pin 5 serves as signal ground; pins 4, 12, 13 serve as heatsink/ground.

TSSOP-24 (Top View)
PWP Package



* PWP package pin 9 serves as signal ground; pins 5, 6, 7, 8, 17, 18, 19, and 20 serve as heatsink/ground.

Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = 0^\circ\text{C}$ to 70°C .
 $\text{TRMPWR} = 4.75\text{V}$, $\text{DISCNCT} = 0\text{V}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Current Section						
Tempwr Supply Current	All termination lines = Open		17	23	mA	
	All termination lines = 0.5V		200	225	mA	
Power Down Mode	DISCNCT = Open		100	150	μA	
Output Section (Termination Lines)						
Terminator Impedance	$\Delta\text{LINE} = -5\text{mA}$ to -15mA	104.5	110	115.5	Ohms	
Output High Voltage		2.65	2.9	3.1	V	
Max Output Current	$V_{\text{LINE}} = 0.5\text{V}$	$T_J = 25^\circ\text{C}$	-20.3	-21.5	-22.4	mA
		$0^\circ\text{C} < T_J < 70^\circ\text{C}$	-19.8	-21.5	-22.4	mA
Max Output Current	$V_{\text{LINE}} = 0.5\text{V}$, $\text{TRMPWR} = 4\text{V}$ (Note 1)	$T_J = 25^\circ\text{C}$	-19.5	-21.5	-22.4	mA
		$0^\circ\text{C} < T_J < 70^\circ\text{C}$	-19.0	-21.5	-22.4	mA
Output Leakage	DISCNCT = 4V TRMPWR = 0V to 5.25V	REG = 0V	$V_{\text{LINE}} = 0$ to 4V	10	400	nA
		REG = Open		$V_{\text{LINE}} = 5.25\text{V}$	100	μA
		REG = Open	$V_{\text{LINE}} = 0\text{V}$ to 5.25V	10	400	nA
Output Capacitance	DISCNCT = Open (Note 2) (DP Package)		5	6	pF	
Regulator Section						
Regulator Output Voltage		2.7	2.9	3.1	V	
	All Termination Lines = 4V	2.7	2.9	3.1	V	
Line Regulation	TRMPWR = 4V to 6V		10	20	mV	
Drop Out Voltage	All Termination Lines = 0.5V		1.0	1.2	V	
Short Circuit Current	REG = 0V	-200	-400	-600	mA	
Sinking Current Capability	REG = 3.5V	75	100	400	mA	
Thermal Shutdown			170		$^\circ\text{C}$	
Thermal Shutdown Hysteresis			10		$^\circ\text{C}$	
Disconnect Section						
Disconnect Threshold		1.1	1.4	1.7	V	
Input Current	DISCNCT = 0V		-10	-20	μA	

Note 1: Measuring each termination line while other 8 are low.

Note 2: Guaranteed by design. Not 100% tested in production.

APPLICATION INFORMATION

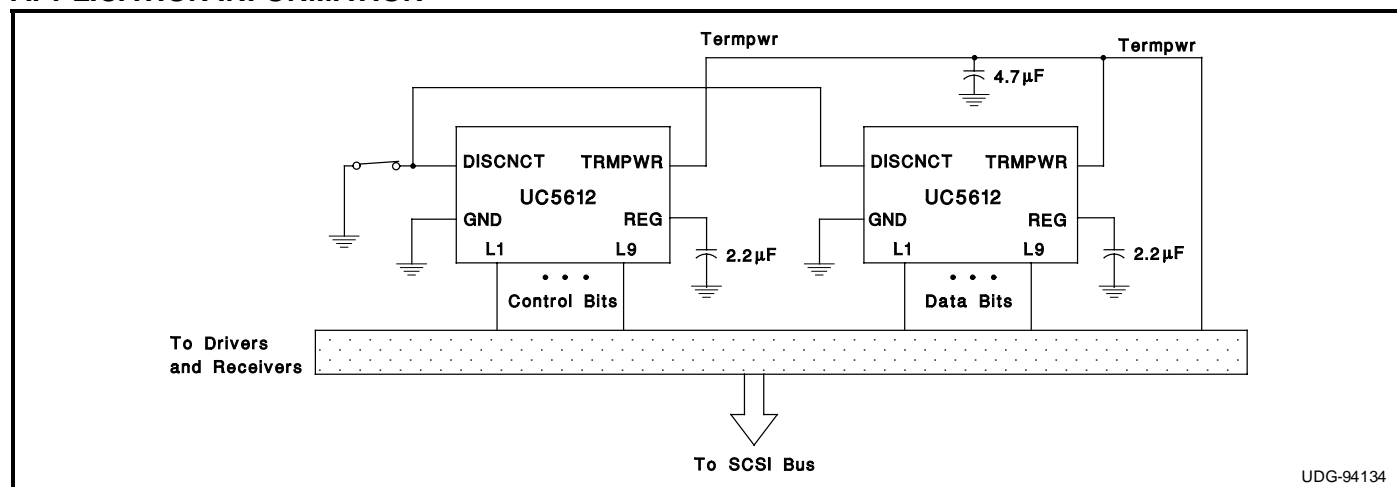


Figure 1: Typical SCSI Bus Configurations Utilizing 2 UC5612 Devices

APPLICATION INFORMATION (cont.)

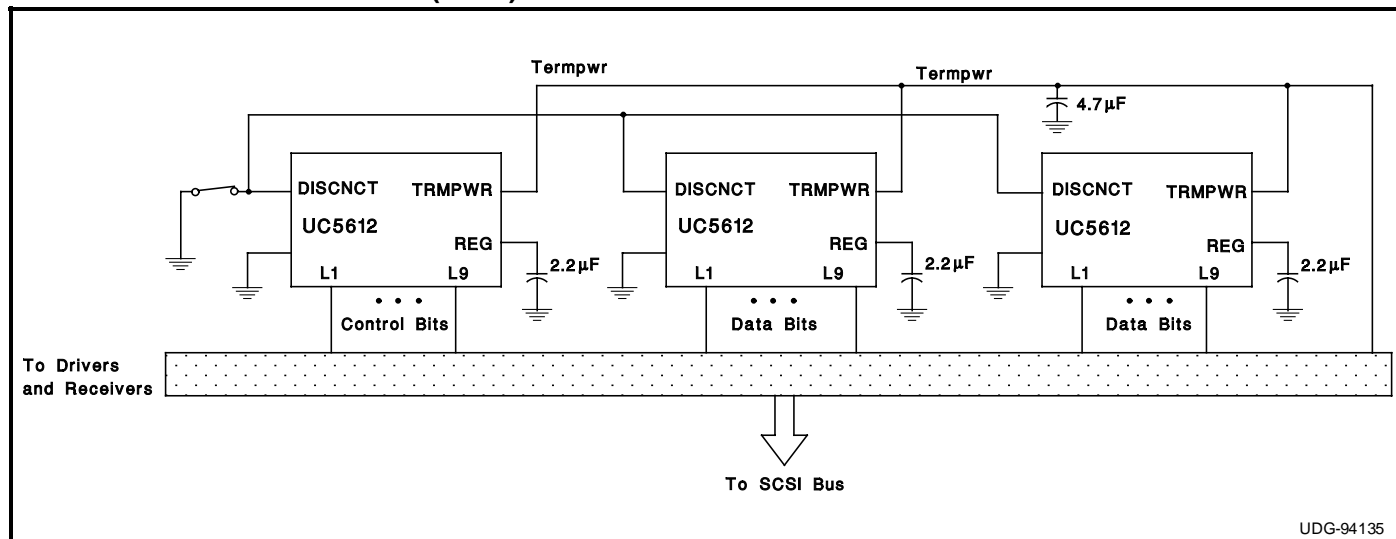


Figure 2: Typical Wide SCSI Bus Configurations Utilizing 3 UC5612 Devices.

UDG-94135

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UC5612, 9-LINE 5V SE TERMINATOR FOR SCSI AND FAST SCSI WITH INVERTED SENSING

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Applications](#)

Parameter Name	UC5612
Number of Lines	9
Driver Types Supported	SE
TERMPWR Voltage (max) (V)	5.25
TERMPWR Voltage (min) (V)	4.0
Disconnect Active State	High
Integrated SPI-3 Mode Switching Filter/Delay	No
Process	Bi-Polar
Active Negation Support	Yes
Channel Capacitance (pF)	4
Resistor Tolerance (ppm)	50
Typical Sink Current (mA)	200
Current Tolerance (%)	5
Single-Ended Termination Impedance (ohms)	110
Single-Ended Tolerance (%)	5
Integrated TERMPWR Regulation	No

Description

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To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: [slus164.pdf](#) (279 KB)

Pricing/Samples/Availability

Orderable Device	Package	Pins	Temp (°C)	Status	Price/unit USD (100-999)	Pack Qty	Availability / Samples
UC5612DP	D	16	0 TO 70	ACTIVE	4.37	1	Check stock or order
UC5612DPTR	D	16	0 TO 70	ACTIVE	3.84	1	Check stock or order
UC5612N	N	16	0 TO 70	ACTIVE	3.47	1	Check stock or order
UC5612PWP	PWP	24	0 TO 70	ACTIVE	4.87	1	Check stock or order
UC5612PWPTR	PWP	24	0 TO 70	ACTIVE	4.31	1	Check stock or order

Application Reports

- COMPARING BUS SOLUTIONS (SLLA067 - Updated: 03/06/2000)
- ELECTROSTATIC DISCHARGE APPLICATION NOTE (SSYA008 - Updated: 05/05/1999)
- JITTER ANALYSIS (SLLA075 - Updated: 03/31/2000)
- THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS (SZZA017A - Updated: 09/10/1999)

Table Data Updated on: 8/16/2000

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