

Low Voltage Differential (LVD/SE) SCSI 9 Line Terminator

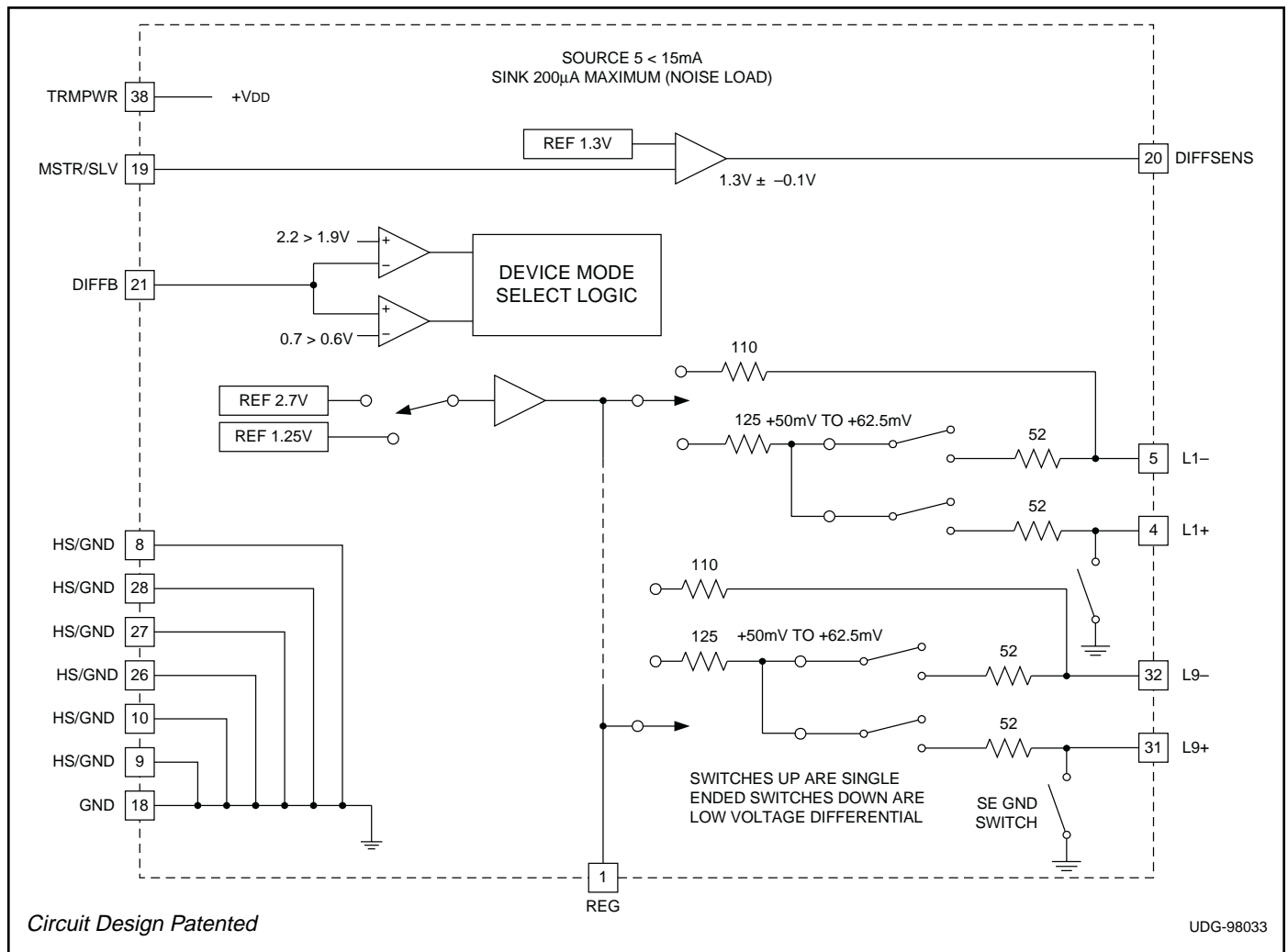
FEATURES

- Auto Selection Multi-Mode Single Ended or Low Voltage Differential Termination
- 3.0V to 5.25V Operation
- Differential Failsafe Bias
- Thermal Packaging for Low Junction Temperature and Better MTBF
- Master/Slave Inputs
- Supports Active Negation
- 3pF Channel Capacitance

DESCRIPTION

The UCC5510 Multi-Mode Low Voltage Differential and Single Ended Terminator is specially designed for automatic termination of Single-Ended or Low Voltage Differential SCSI Bus. The Multi-Mode operation of this device allows for a transition system design for the next generation SCSI Parallel Interface (SPI-2). Compliant with SPI-2, with SPI and Fast-20 the UCC5510 incorporates all the functions necessary to properly terminate the SCSI Bus and has internal thermal shut down and short circuit limiting.

BLOCK DIAGRAM



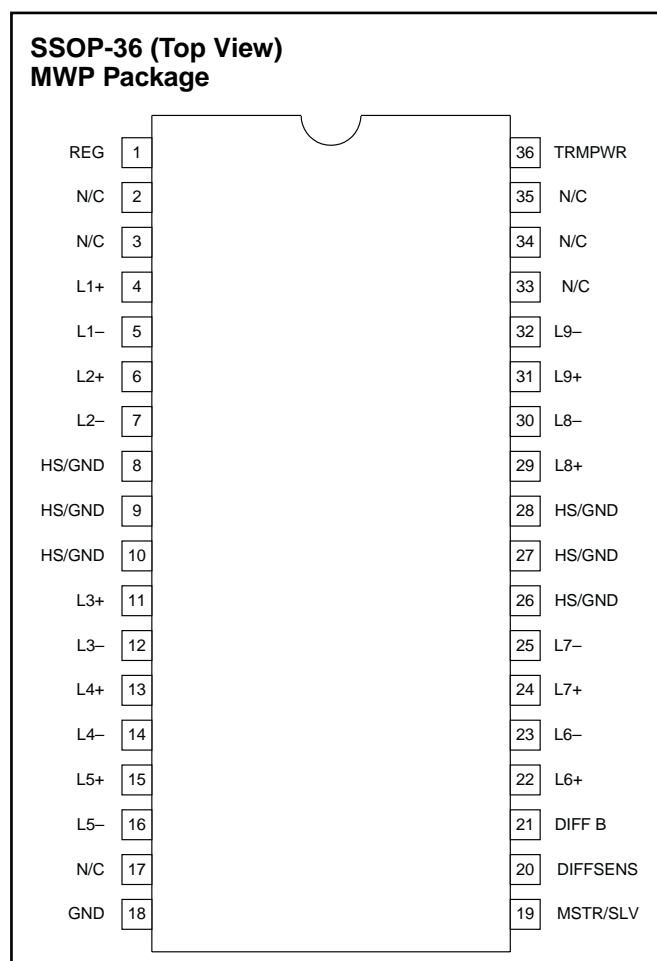
ABSOLUTE MAXIMUM RATINGS

| | |
|--------------------------------------|-----------------|
| TRMPWR Voltage | 6V |
| Signal Line Voltage | 0V to TRMPWR |
| Package Power Dissipation | 2W |
| Storage Temperature | -65°C to +150°C |
| Junction Temperature | -55°C to +150°C |
| Lead Temperature (Soldering, 10sec.) | +300°C |

RECOMMENDED OPERATING CONDITIONS

| | |
|----------------|---------------|
| TRMPWR Voltage | 3.0V TO 5.25V |
|----------------|---------------|

All voltages are with respect to pin 1. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, $T_A = 0^\circ\text{C}$ to 70°C , TRMPWR = 3.3V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|--|------|------|------|---------------|
| TRMPWR Supply Current Section | | | | | |
| TRMPWR Supply Current | | | | 20 | mA |
| | Disable Terminator, in DISCNCT mode. | | | 35 | μA |
| Regulator Section | | | | | |
| 1.25V Regulator | LVD Mode | 1.15 | 1.25 | 1.35 | V |
| 1.25V Regulator Source Current | LVD Mode, Differential Sense Floating | -80 | -100 | | mA |
| 1.25V Regulator Sink Current | LVD Mode, Differential Sense Floating | 80 | 100 | | mA |
| 1.3V Regulator | DIFFSENS | 1.2 | 1.3 | 1.4 | V |
| 1.3V Regulator Source Current | DIFFSENS | -5 | | -15 | mA |
| 1.3V Regulator Sink Current | DIFFSENS | 50 | | 200 | μA |
| 2.7V Regulator | Single Ended Mode | 2.5 | 2.7 | 3 | V |
| 2.7V Regulator Source Current | Single Ended Mode | -200 | -400 | -800 | mA |
| 2.7V Regulator Sink Current | Single Ended Mode | 100 | 200 | 400 | mA |
| 2.7V Regulator Dropout Voltage | $V_{\text{TRMPWR}} - (V_{\text{REG}} - 3.0 \text{ Min})$ | | | 200 | mV |

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, $T_A = 0^\circ\text{C}$ to 70°C , $\text{TRMPWR} = 3.3\text{V}$.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|-------|------|-------|---------------|
| Differential Termination Section | | | | | |
| Differential Impedance | | 100 | 105 | 110 | Ω |
| Common Mode Impedance | | 110 | 125 | 165 | Ω |
| Differential Bias Voltage | Drivers Tri-stated | 100 | | 125 | mV |
| Common Mode Bias | | | 1.25 | | V |
| Output Capacitance | Single Ended Measurement to Ground (Note 1) | | | 3 | pF |
| Single Ended Termination Section | | | | | |
| Impedance | | 102.3 | 110 | 117.7 | Ω |
| Termination Current | Signal Level 0.2V | -21 | -23 | -24 | mA |
| | Signal Level 0.5V | | | -22.4 | mA |
| Output Leakage | Disabled, $\text{TRMPWR} = 0\text{V}$ to 5.25V | | | 400 | nA |
| Output Capacitance | Single Ended Measurement to Ground (Note 1) | | | 3 | pF |
| Single Ended GND SW Impedance | | | | 60 | Ω |
| Differential Sense (DIFF B) Input Sections | | | | | |
| DIFFB Single Ended Threshold | | 0.6 | | 0.7 | V |
| DIFFB Sense LVD Threshold | | 1.9 | | 2.2 | V |
| DIFFB Input Current | $V_{\text{DIFFB}} = 0\text{V}$ and 3.3V | -10 | | 10 | μA |
| Master/Slave (MSTR/SLV) Input Section | | | | | |
| MSTR/SLV Threshold | | 0.8 | | 2 | V |
| MSTR/SLV Input Current | | -30 | | 30 | μA |

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

DIFFB: DIFF SENSE filter pin should be connected to a $0.1\mu\text{F}$ capacitor to GND and 20k resistor to SCSI/Bus DIFF SENSE Line.

DIFFSENS: The SCSI bus DIFF SENSE line is driven to 1.3V to detect what type of devices are connected to the SCSI bus.

HS/GND: Heat Sink GND. Connect to large area PC board traces to increase power dissipation capability.

GND: Power Supply Return.

L1– thru L9–: Signal line/active line for single ended or

negative line in differential applications for the SCSI bus.

L1+ thru L9+: Ground line for single ended or positive line for differential applications for the SCSI bus.

MSTR/SLV: Mode select for the non-controlling terminator. MSTR enables the 1.3V regulator, when the terminator is enabled. **Note:** This function will be removed on further generations of the multimode terminators.

REG: Regulator bypass, must be connected to a $4.7\mu\text{F}$ capacitor.

TRMPWR: V_{IN} 3.0V to 5.25V supply.

APPLICATION INFORMATION

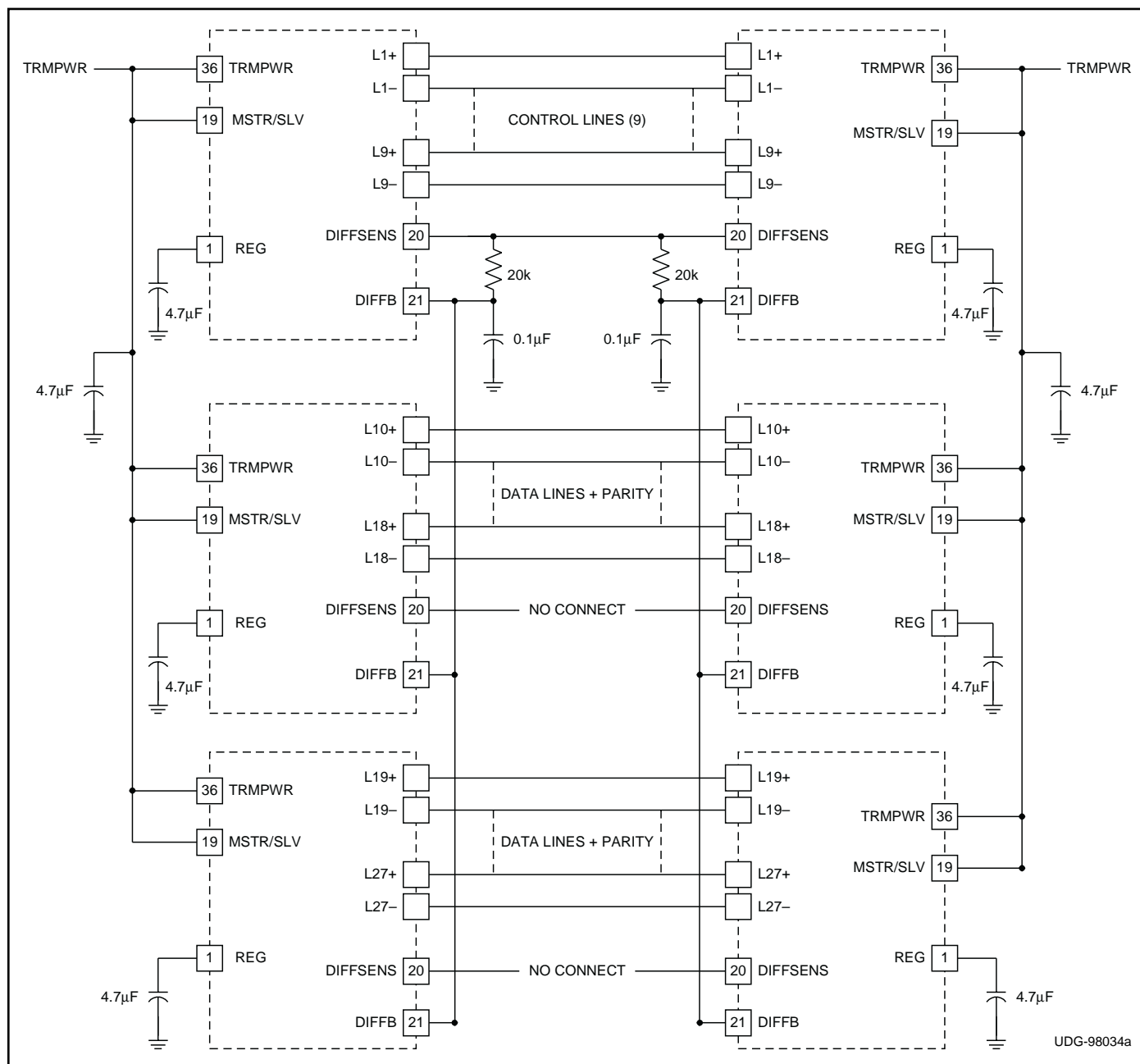


Figure 1. Application Drawing

The master is selected by placing TRMPWR on MSTR/SLV and enabling the 1.3V regulator. The master is the only terminator connected directly to the DIFFSENS bus line. All the other terminators receive a mode signal by connecting the DIFFFB pins together.

The balancing capacitor is very important during high speed operation. The typical capacitor balance between the positive (+) and negative (-) signals is 0.1pF, except

in the MWP package where between L8 and L9 the balance is 0.23pF and 0.4pF respectively. The negative (-) signal line has a higher capacitance than the positive (+) signal line. The FQP package has typically 0.2pF less capacitance than the MWP package, where the typical balance is 0.1pF except for L8 and L3, where the balance is 0.4pF.

Note: The master/slave function will not be included in future Unitrode terminators.

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UCC5510, 9-LINE MULTIMODE TERMINATOR FOR PLUGS AND CONNECTORS

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Applications](#)

| Parameter Name | UCC5510 |
|--|---------|
| Number of Lines | 9 |
| Driver Types Supported | LVD, SE |
| TERMPWR Voltage (max) (V) | 5.25 |
| TERMPWR Voltage (min) (V) | 3.0 |
| Integrated SPI-3 Mode Switching Filter/Delay | No |
| Process | Bi-CMOS |
| Active Negation Support | Yes |
| Channel Capacitance (pF) | 3 |
| Resistor Tolerance (ppm) | 500 |
| Typical Sink Current (mA) | 100 |
| Current Tolerance (%) | 4 |
| Single-Ended Termination Impedance (ohms) | 110 |
| Single-Ended Tolerance (%) | 7 |
| LVD Termination Impedance (ohms) | 105 |
| LVD Tolerance (%) | 5 |
| Commonmode Impedance (ohms) | 125 |
| Integrated TERMPWR Regulation | No |

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Features

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- 3pF Channel Capacitance

To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Datasheets

Full datasheet in Acrobat PDF: [slus332a.pdf](#) (47 KB)

Full datasheet in Zipped PostScript: [slus332a.psz](#) (35 KB)

Pricing/Samples/Availability

| <u>Orderable Device</u> | <u>Package</u> | <u>Pins</u> | <u>Temp (°C)</u> | <u>Status</u> | <u>Price/unit USD (100-999)</u> | <u>Pack Qty</u> | <u>Availability / Samples</u> |
|-------------------------|---------------------|-------------|------------------|---------------|-------------------------------------|-----------------|--------------------------------------|
| UCC5510MWP | DGK | 36 | 0 TO 70 | ACTIVE | 3.43 | 1 | Check stock or order |
| UCC5510MWP-TR | UTR | 36 | 0 TO 70 | OBSOLETE | | | |
| UCC5510MWPTR | DGK | 36 | 0 TO 70 | ACTIVE | 3.07 | 1 | Check stock or order |

Application Reports

- [COMPARING BUS SOLUTIONS](#) (SLLA067 - Updated: 03/06/2000)
- [ELECTROSTATIC DISCHARGE APPLICATION NOTE](#) (SSYA008 - Updated: 05/05/1999)
- [JITTER ANALYSIS](#) (SLLA075 - Updated: 03/31/2000)
- [THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS](#) (SZZA017A - Updated: 09/10/1999)

Table Data Updated on: 8/15/2000