Multimode SCSI 15 Line Terminator

FEATURES

- Auto Selection Single Ended (SE) or Low Voltage Differential (LVD) Termination
- Meets SCSI-1, SCSI-2, Ultra2 (SPI-2 LVD SCSI), Ultra3, Ultra160 (SPI-3) and Ultra320 (SPI-4) Standards
- 2.7V to 5.25V Operation
- Differential Failsafe Bias
- Thermal packaging for low junction temperature and better MTBF.

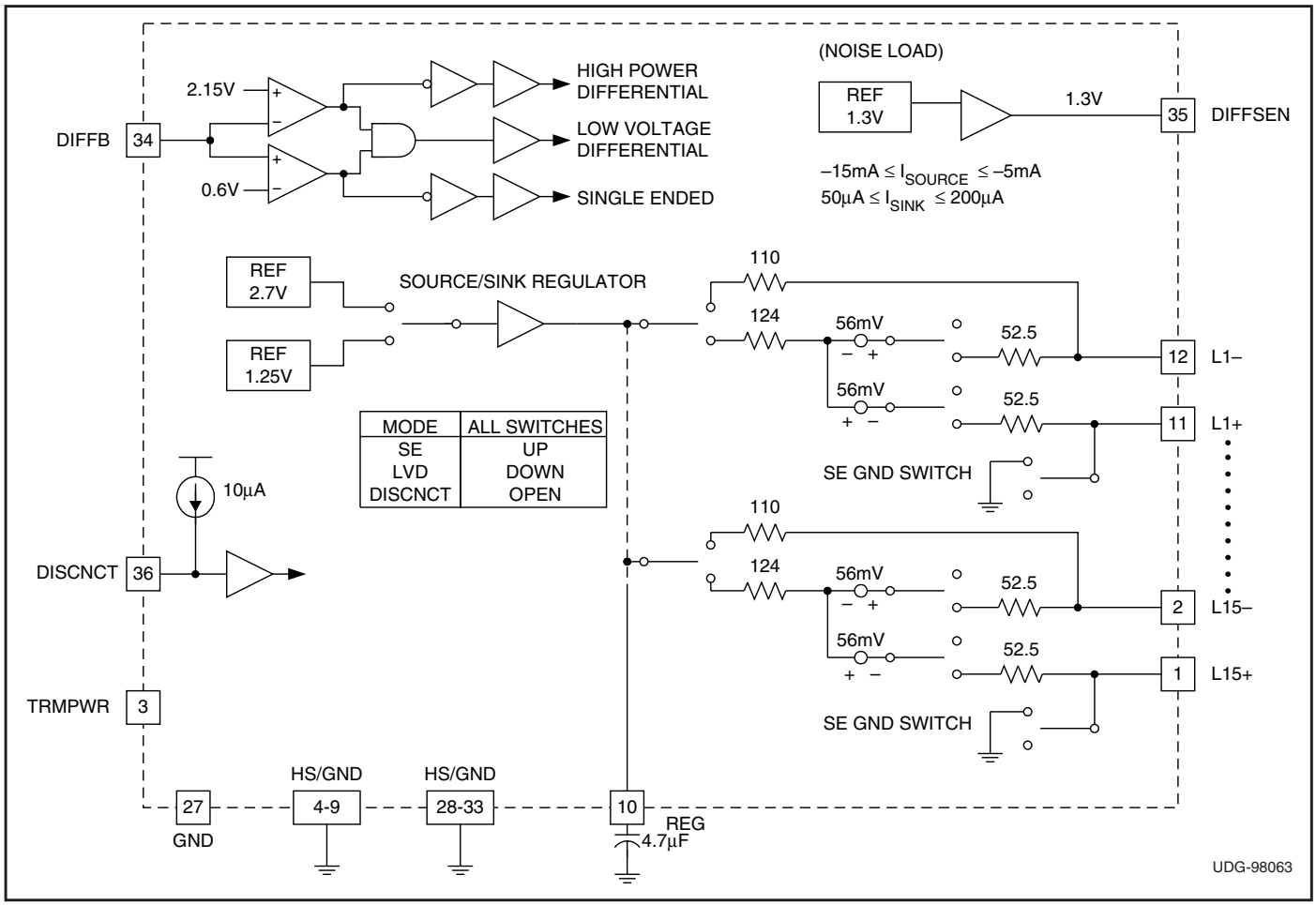
DESCRIPTION

The UCC5638 Multimode SCSI Terminator provides a smooth transition into the LVD SCSI Parallel Interface (SPI-2, SPI-3, SPI-4). It automatically senses the bus, via DIFFB, and switches the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5638 can not be used on a HVD, EIA485, differential SCSI bus. If the UCC5638 detects a HVD SCSI device, it switches to a high impedance state.

The Multimode terminator contains all functions required to terminate and auto detect and switch modes for SPI-2, SPI-3 and SPI-4 bus architectures. Single Ended and Differential impedances and currents are trimmed for maximum effectiveness. Fail Safe biasing is provided to insure signal integrity. Device/Bus type detection circuitry is integrated into the terminator to provide automatic switching of termination between single ended and LVD SCSI and a high impedance for HVD SCSI. The multimode function provides all the performance analog functions necessary to implement SPI-2 termination in a single monolithic device.

The UCC5638 is offered in a 48 pin LQFP package for a temperature range of 0°C to 70°C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

TRMPWR Voltage . . . . . +6V
Signal Line Voltage . . . . . 0V to 5V
Package Dissipation 2W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C
Recommended Operating Conditions . . . . . 2.7V to 5.25V

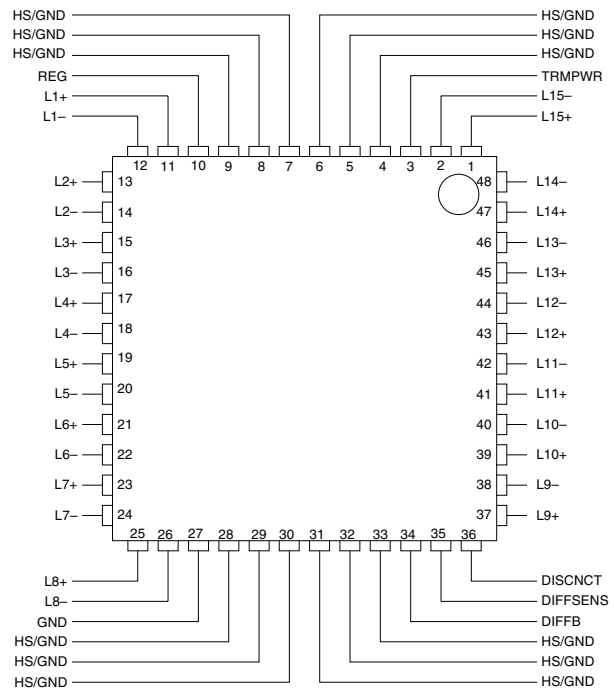
Currents are positive into negative out of the specified terminal.
Note: Consult Packaging Section of Databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS

TRMPWR Voltage . . . . . 2.7V to 5.25V
Temperature Ranges . . . . . 0°C to +70°C

CONNECTION DIAGRAMS

(TOP VIEW)
FQP Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR Supply Current Section					
TRMPWR Supply Current	LVD SCSI Mode		20	25	mA
	SE SCSI Mode		1.6	10	mA
	Disabled Terminator		250	400	µA
Regulator Section					
1.25V Regulator	LVD SCSI Mode	1.15	1.25	1.35	V
1.25V Regulator Source Current	V_{REG} = 0V	–375	–700	–1000	mA
1.25V Regulator Sink Current	V_{REG} = 3.3V	170	300	700	mA
1.3V Regulator	Diff Sense	1.2	1.3	1.4	V
1.3V Regulator Source Current	V_{REG} = 0V	–15		–5	mA
1.3V Regulator Sink Current	V_{REG} = 3.3V	50		200	µA
2.7V Regulator	SE SCSI Mode	2.5	2.7	3.0	V
2.7V Regulator Source Current	V_{REG} = 0V	–375	–700	–1000	mA
2.7V Regulator Sink Curren	V_{REG} = 3.3V	170	300	700	mA
Differential Termination Section					
Differential Impedance		100	105	110	Ω
Common Mode Impedence	(Note 2)	110	150	165	Ω
Differential Bias Voltage		100		125	mV
Common Mode Bias		1.15	1.25	1.35	V
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Single Ended Termination Section					
Impedance	$Z = (VL_X - 0.2V) / IL_X$, (Note 3)	102.3	110	117.7	Ω
Termination Current	Signal Level 0.2V, All Lines Low	–21	–24	–25.4	mA
	Signal Level 0.5V	–18		–22.4	mA
Output Leakage				400	nA
Output Capacitance	Single Ended Measurement to Ground (Note 1)			3	pF
Single Ended GND SE Impedance	I = 10mA		20	60	Ω
Disconnect and Diff Buffer Input Section					
DISCNCT Threshold		0.8		2.0	V
DISCNCT Input Current			10	30	μA
Diff Buffer Single Ended to LVD Threshold		0.5		0.7	V
Diff Buffer LVD to HPD Threshold		1.9		2.4	V
DIFFB Input Current		–10		10	μA

Note 1: *Ensured by design. Not 100% tested in production.*

Note 2: *Line+ (positive) tied to Line– (negative);* $\frac{1.2V}{\left[I_{(VCM\,max)} - I_{(VCM\,min)}\right]}$

Note 3: *VL_X= Output voltage for each terminator minus output pin (L1– through L15–) with each pin unloaded.*
IL_X = Output current for each terminator minus output pin (L1– through L15–) with the minus output pin forced to 0.2V.

PIN DESCRIPTIONS

DIFFB: Diff sense filter pin should be connected at a 4.7μF capacitor.

DIFFSENS: The SCSI bus Diff Sense line to detect what types of devices are connected to the SCSI bus.

DISCNCT: Disconnect pin shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.

Note: *In Disconnect Mode, the comparitor set powers down for low idle current.*

LINE*n*–: Signal line active line for single ended or negative line in differential applications for the SCSI bus.

LINE*n*+: Ground line for single ended or positive line for differential applications for the SCSI bus.

REG: Regulator bypass pin, must be connected to a 4.7μF capacitor.

TRMPWR: V_{IN} 2.7V to 5.25V supply, bypass near the terminator with a 4.7 μF capacitor to ground.

APPLICATION INFORMATION

The UCC5638 is a Multi-mode active terminator with selectable single ended (SE) and low voltage differential (LVD) SCSI termination integrated into a monolithic component. Mode selection is accomplished with the “diff sense" signal.

The diff sense signal is a three level signal, which is driven at each end of the bus by one active terminator. An LVD SCSI or multi-mode terminator drives the diff sense line to 1.3 V. If diff sense is at 1.3 V, then bus is in LVD SCSI mode. If a single ended SCSI device is plugged into the bus, the diff sense line is shorted to ground. With diff sense shorted to ground, the terminator changes to single ended mode to accommodate the SE device. If an HVD SCSI device is plugged in to the bus, the diff sense line is pulled high and the terminator shuts down.

The diff sense line is driven and monitored by the terminator through a 100ms to 300ms noise filter at the DIFFB input pin. A set of comparators, that allow for ground shifts, determine the bus status as follows. Any diff sense signal below 0.5V indicates single ended, between 0.7V and 1.9V is LVD SCSI and above 2.2V is HVD SCSI.

In the single ended mode, a multi-mode terminator has a 110Ω terminating resistor connected to a 2.7V termination voltage regulator. The 2.7V regulator is used on all Unitrode terminators designed for 3.3V systems. This requires the terminator to operate in specification down to 2.7V TRMPWR voltage to allow for the 3.3V supply tolerance, an unidirectional fusing device and cable drop. At each L+ pin, a ground driver drives the pin to ground, while in single ended mode. The ground driver is specially designed so it will not effect the capacitive balance of the bus when the device is in LVD SCSI or disconnect mode. The device requirements call for 0.5pF balance on the lines of a differential pair. The terminator capacitance has to be a small part of the capacitance imbalance.

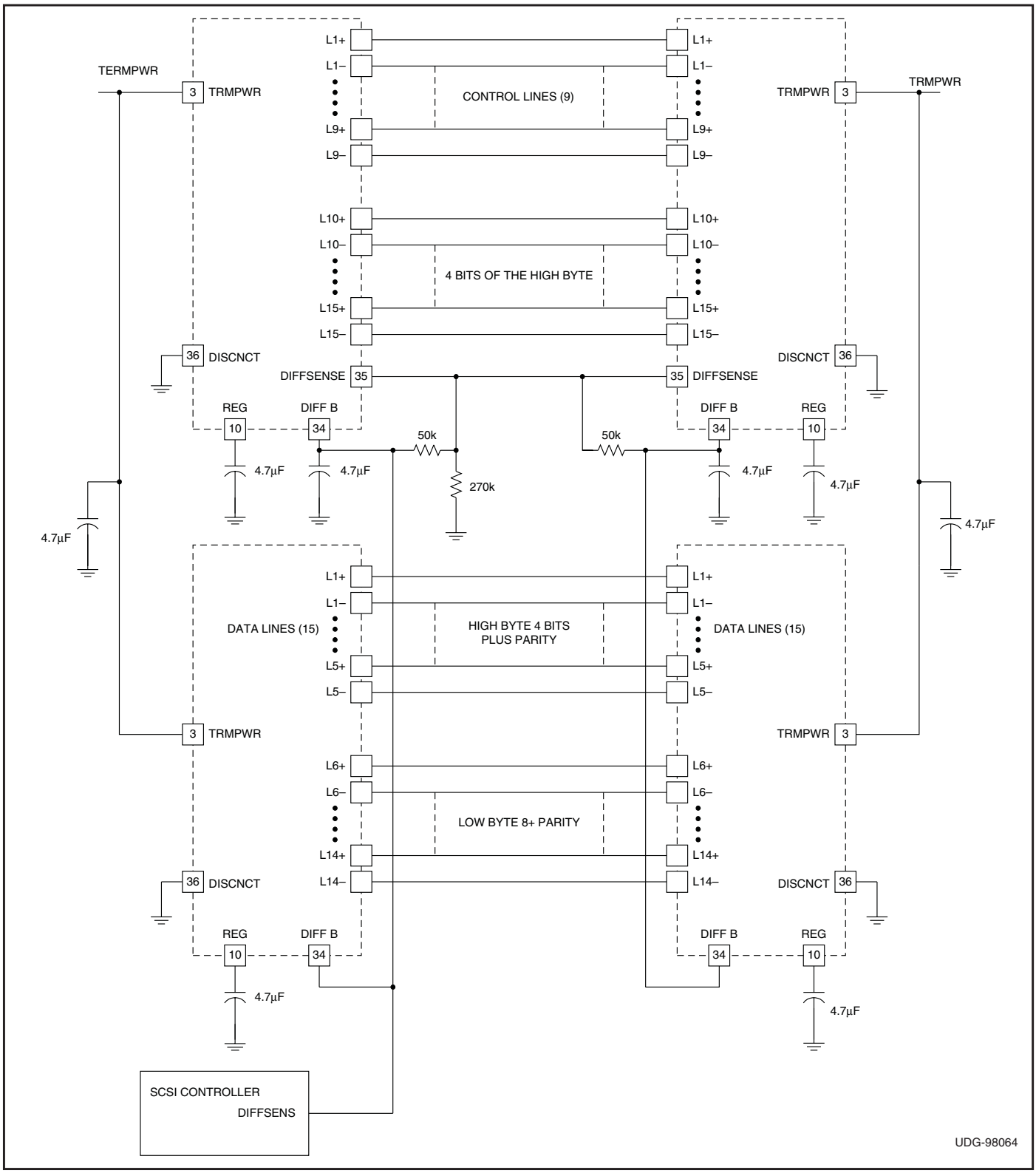
Layout is very critical for Ultra2, Ultra3, Ultra160 and Ultra320 systems. Multi-layer boards need to adhere to the 120Ω impedance standard, including connector and feed-through. This is normally done on the outer layers with 4 mil etch and 4 mil spacing between the runs within a pair, and a minimum of 8 mil spacing to the next pair. This spacing between the pairs reduces potential crosstalk. Beware of feed-throughs and each through hole connection adds a lot of capacitance. Standard power and ground plane spacing yields about 1pF to each plane. Each feed-through will add about 2.5pF to 3.5pF. Enlarging the clearance holes on both power and ground planes can reduce the capacitance and opening up the power and ground planes under the connector can reduce the capacitance for through hole connector applications. Microstrip technology is normally too low of impedance and should not be used. It is designed for 50Ω rather than 120Ω differential systems.

Capacitance balance is critical for Ultra2 and Ultra3/Ultra160. The balance capacitance standard is 0.5pF per line with the balance between pairs of 2pF. The components are designed with very tight balance, typically 0.1pF between pins in a pair and 0.3pF between pairs. Layout balance is critical, feed-throughs and etch length must be balanced, preferably no feed-throughs would be used. Capacitance for devices should be measured in the typical application, material and components above and below the circuit board effect the capacitance.

Multi-mode terminators need to consider power dissipation; the UCC5638 is offered in a power package with heat sink ground pins. These heat sink/ground pins are directly connected to the die mount paddle under the die and conduct heat from the die to reduce the junction temperature. These pins need to be connected to etch area or a feed-through per pin connecting to the ground plane layer on a multi-layer board.

In 3.3V TRMPWR systems, the UCC3912 should be used to replace the fuse and diode. This reduces the voltage drop, allowing for cable drop to the far end terminator. 3.3V battery systems normally have a 10% tolerance. The UCC3912 is 150mV drop under LVD SCSI loads, allowing 150mV drop in the cable system. All Unitrode LVD SCSI and multi-mode terminators are designed for 3.3V systems, operating down to 2.7V.

TYPICAL APPLICATION



Note: *A 220k resistor is added to ground to insure the transceivers will come up in single-ended mode when no terminator is enabled. The controller DIFFSENS ties to the DIFFB pin on the terminators, only one RC network should be on a device.*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5638FQPTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	UCC5638 FQP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

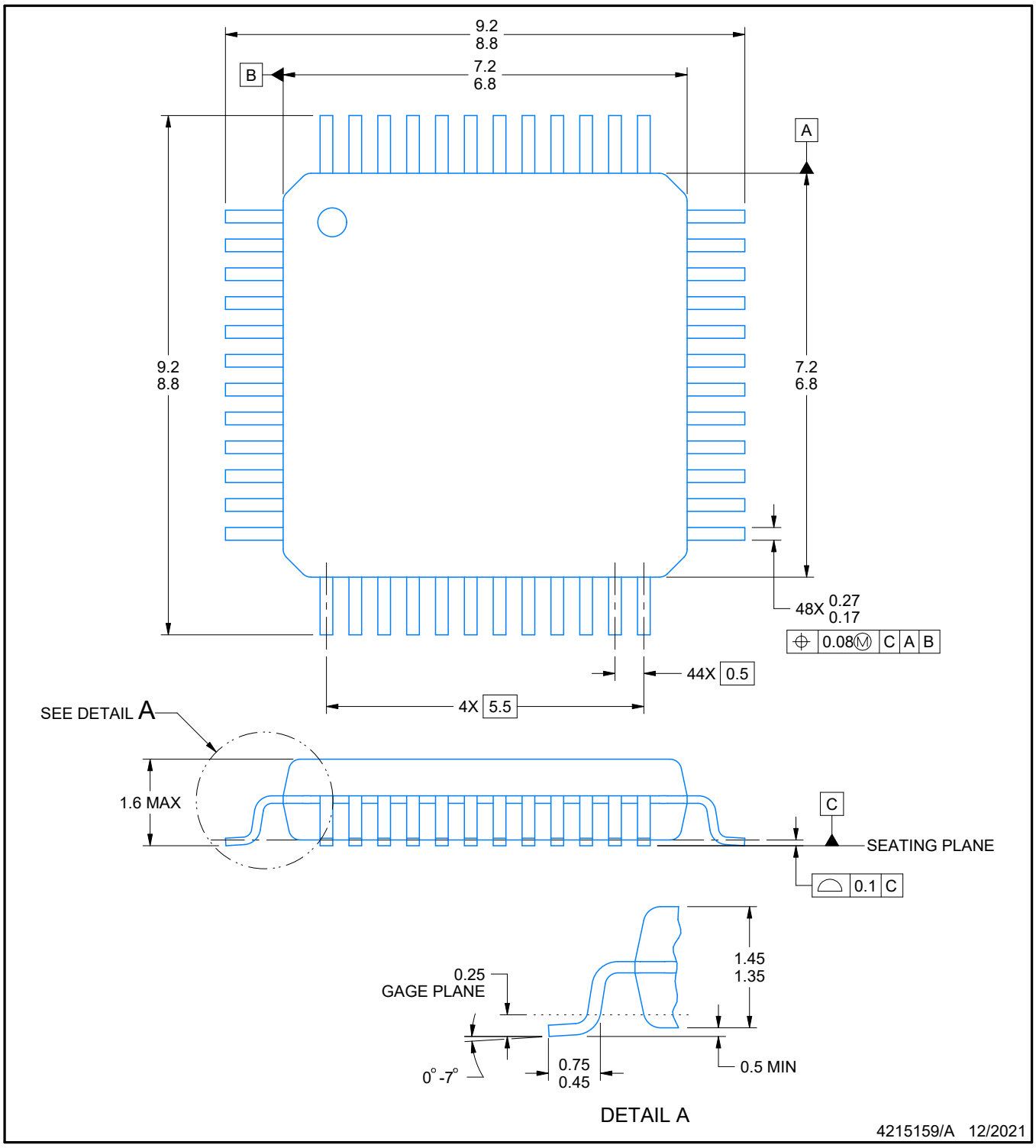
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PT0048A

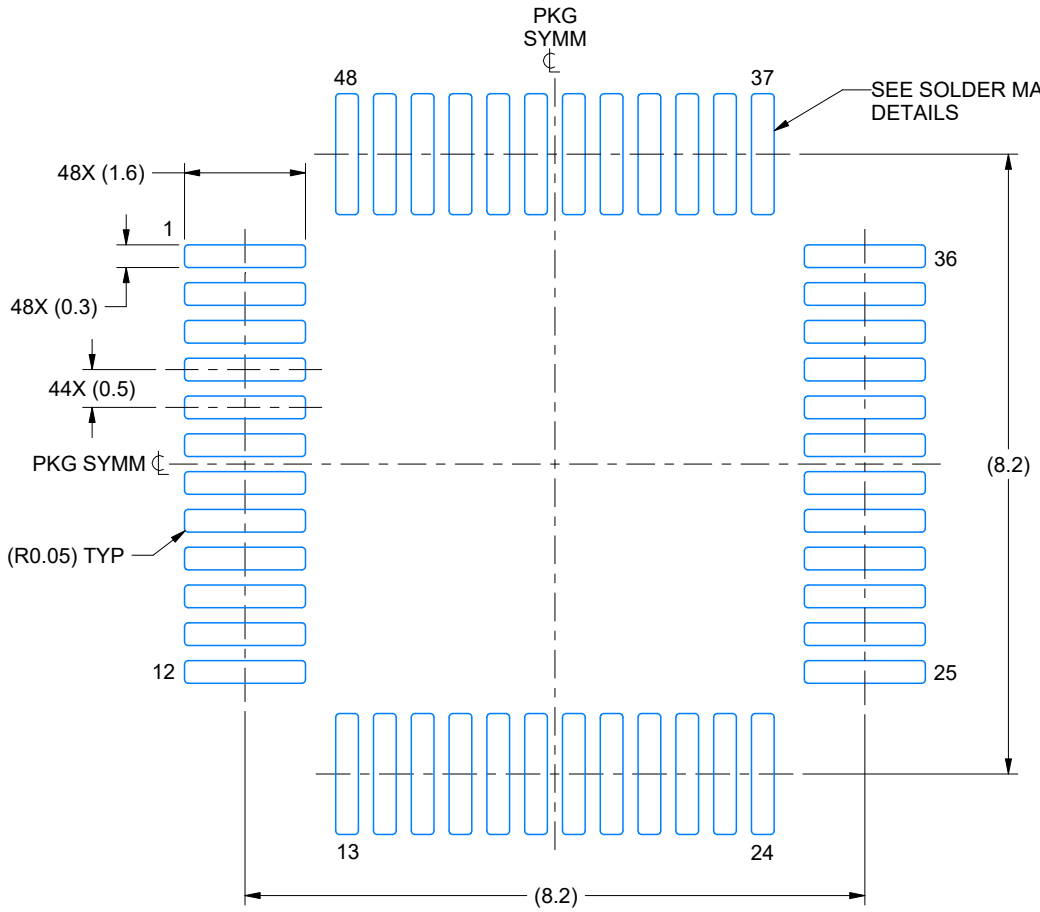
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

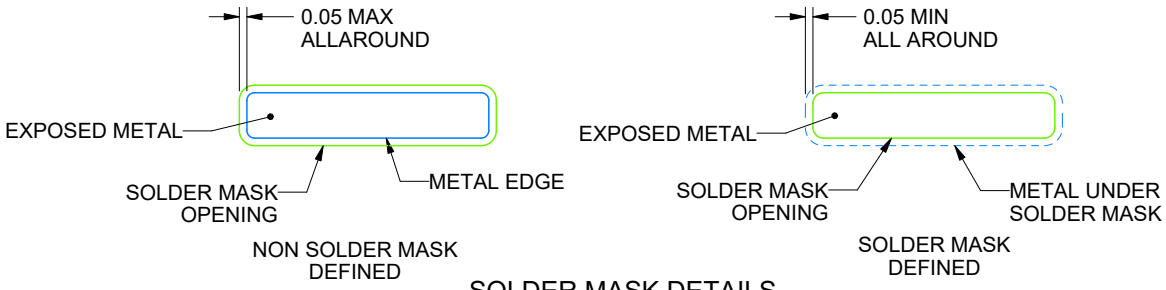


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

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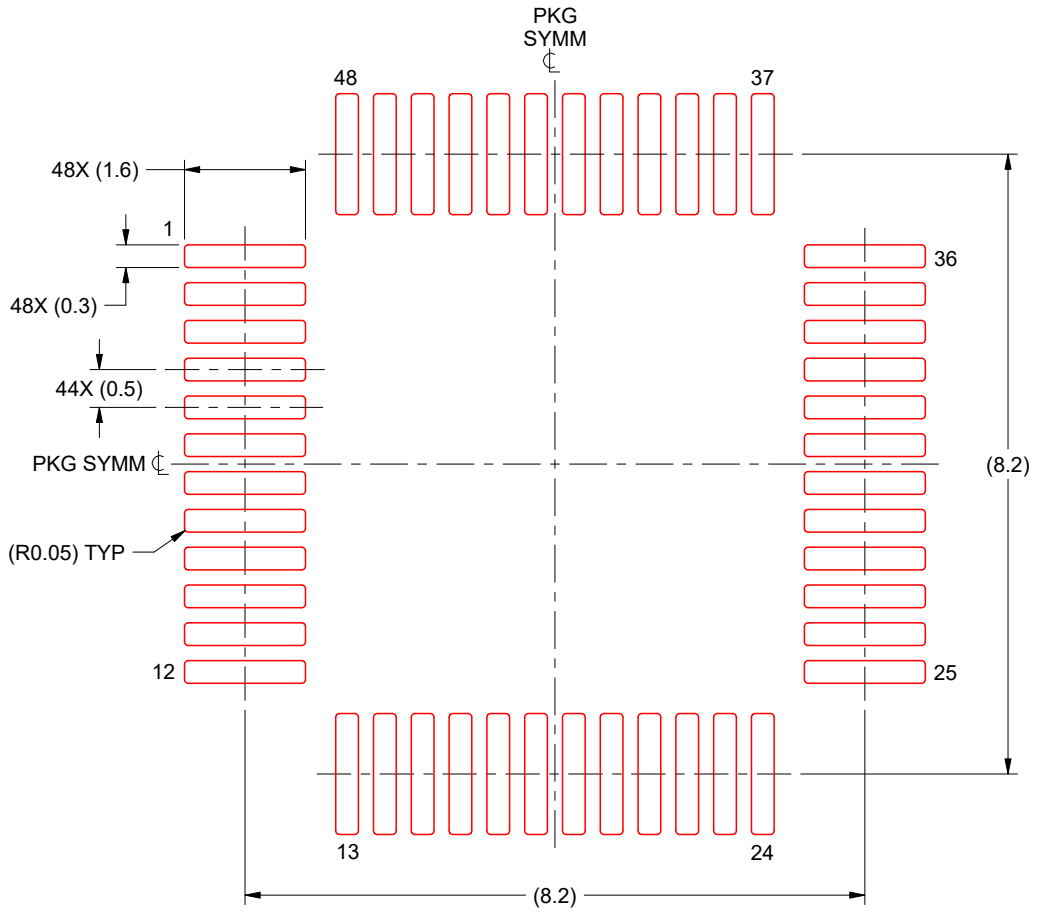
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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