



54F/74F353

Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

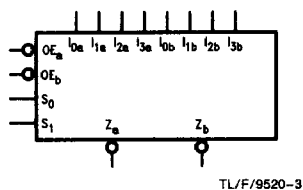
The 'F353 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (\overline{OE}) inputs, allowing the outputs to interface directly with bus-oriented systems.

Features

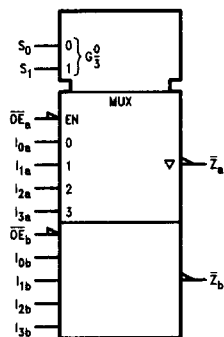
- Inverted version of 'F253
- Multifunction capability
- Separate enables for each multiplexer

Ordering Code: See Section 5

Logic Symbols

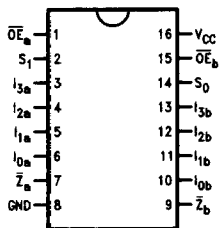


IEEE/IEC

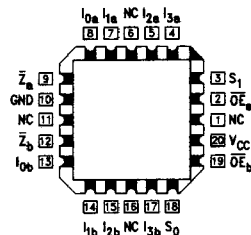


Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



Pin Assignment
for LCC



Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$I_{0a}-I_{3a}$	Side A Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
$I_{0b}-I_{3b}$	Side B Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
S_0, S_1	Common Select Inputs	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}_a	Side A Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}_b	Side B Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
Z_a, Z_b	TRI-STATE Outputs (Inverted)	150/40 (33.3)	-3 mA/24 mA (20 mA)

Functional Description

The 'F353 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a, \overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\begin{aligned}\overline{Z}_a &= \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + \\ &\quad I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0) \\ \overline{Z}_b &= \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + \\ &\quad I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)\end{aligned}$$

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	\overline{OE}	\overline{Z}
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.

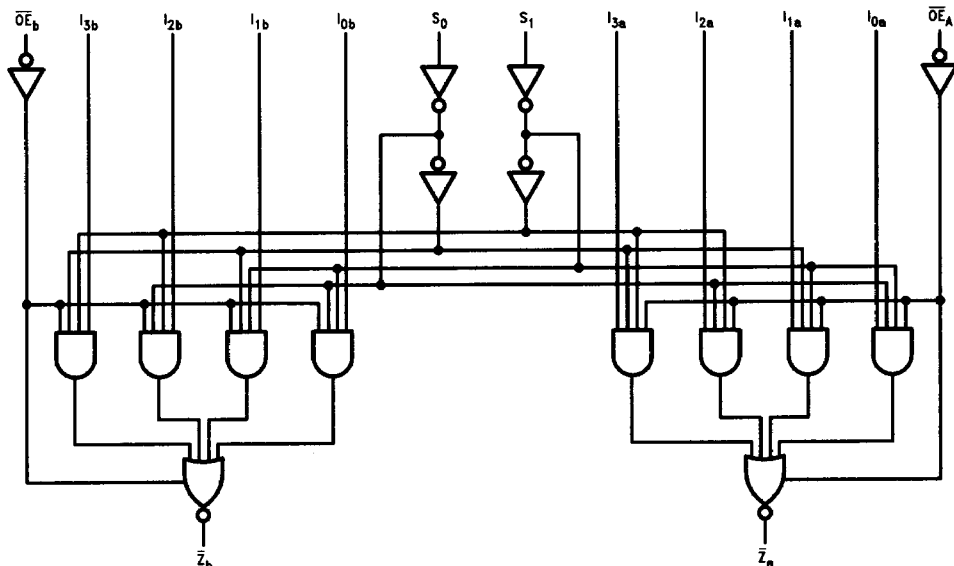
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



TL/F/9520-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	-0.5V to V _{CC}
Standard Output	-0.5V to +5.5V
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	-55°C to +125°C
Military	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Military	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current		9.3	14	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		13.3	20	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		15.0	23	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Min C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay S _n to \bar{Z}_n	4.0 3.5	8.0 6.5	11.0 8.5	3.5 3.0	14.0 11.0	3.5 3.0	12.5 9.5	ns	2-3
t _{PLH} t _{PHL}	Propagation Delay I _n to \bar{Z}_n	3.0 1.3	5.2 2.5	7.0 4.0	3.0 1.0	9.0 5.0	3.0 1.0	8.0 4.5	ns	2-3
t _{PZH} t _{PZL}	Output Enable Time	2.5 3.0	5.5 6.0	8.0 8.0	2.0 2.5	10.5 10.5	2.0 2.5	9.0 9.0	ns	2-5
t _{PHZ} t _{PLZ}	Output Disable Time	2.0 2.0	3.7 4.4	5.0 6.0	2.0 2.0	7.0 8.0	2.0 2.0	6.0 7.0		