



MM54HCT257/MM74HCT257 Quad 2-Channel TRI-STATE® Multiplexer

MM54HCT258/MM74HCT258 Quad 2-Channel TRI-STATE® Multiplexer (Inverted Output)

General Description

These Quad 2-to-1 line data selector/multiplexers utilize advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, these possess the ability to drive LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make these devices ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, A or B data is selected for the HCT257 while \bar{A} or \bar{B} data is selected for the HCT258.

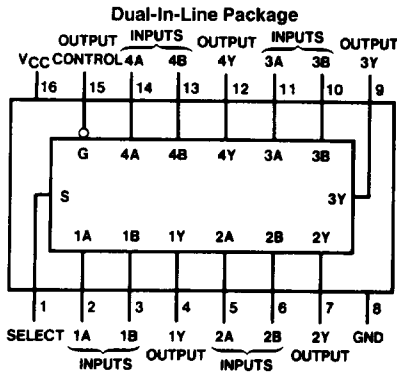
The 54HCT/74HCT logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family.

All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Power supply range: $5V \pm 10\%$
- Low quiescent current: 80 μA maximum (74HC Series)
- Completely TTL compatible
- TRI-STATE outputs for connection to system buses
- Added circuitry allows data input levels to float during TRI-STATE with no additional power consumption
- High output drive current: 60 mA minimum

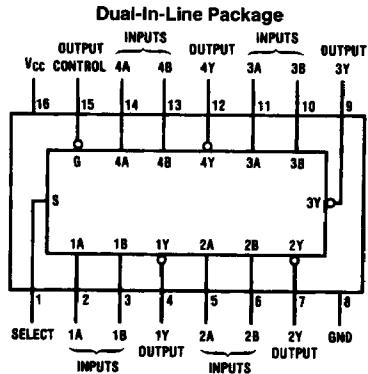
Connection Diagrams



TL/F/6121-1

Top View

Order Number MM54HCT257* or MM74HCT257*



TL/F/6121-2

Top View

Order Number MM54HCT258* or MM74HCT258*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

Output Control	Inputs		Output Y
	Select	A B	
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

Output Control	Inputs		Output Y
	Select	A B	
H	X	X X	Z
L	L	L X	H
L	L	H X	L
L	H	X L	H
L	H	X H	L

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-1.5V to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5V to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per Pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	-40	+85	°C
MM54HCT	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
$V_{CC} = 4.5V$			

DC Electrical Characteristics (Note 4) $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		74HCT	54HCT	Units
			Typ	Guaranteed Limits		$T_A = -40^\circ C$ to $85^\circ C$	
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			0.9	0.9	0.9	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	4.5	4.4	4.4	4.4	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA, $V_{CC} = 4.5V$ $ I_{OUT} \leq 7.2$ mA, $V_{CC} = 5.5V$	4.2	3.98 4.98	3.84 4.84	3.7 4.7	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA, $V_{CC} = 4.5V$	0.2	0.26	0.33	0.4	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 7.2$ mA, $V_{CC} = 5.5V$	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	$V_{OUT} = V_{CC}$ or GND $OC = V_{IH}$		± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		8.0	80	160	μA
		$V_{IN} = 2.4V$ or $0.5V$ (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25^\circ C$, $C_L=45\text{ pF}$, $t_r=t_f=6\text{ ns}$ (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay Select to any Output		16		ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay A or B to any Output		12		ns
t_{PZH} , t_{PZL}	Maximum Enable Time	$R_L = 1\text{ k}\Omega$	23		ns
t_{PHZ} , t_{PLZ}	Maximum Disable Time	$R_L = 1\text{ k}\Omega$ $C_L = 5\text{ pF}$	8		ns

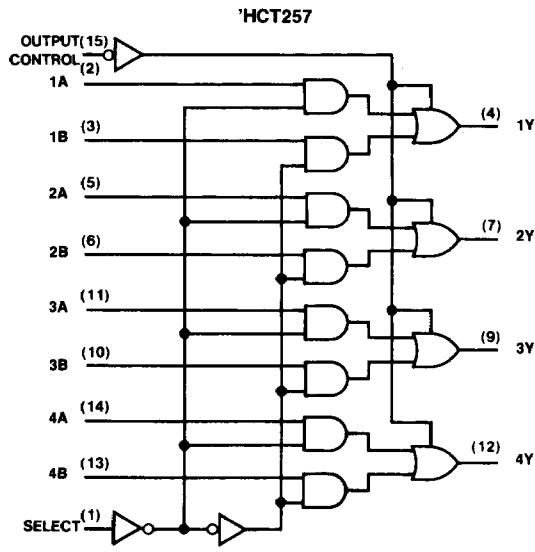
AC Electrical Characteristics $V_{CC}=5V \pm 10\%$, $t_r=t_f=6\text{ ns}$, $C_L=50\text{ pF}$ (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		74HCT $T_A = -40^\circ C$ to $+85^\circ C$		54HCT $T_A = -55^\circ C$ to $+125^\circ C$		Units
			Typ		Guaranteed Limits				
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Select to any Output		18	24	30		36		ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay, A or B to any Output		15	20	25		30		ns
t_{PZH} , t_{PZL}	Maximum Enable to any Output	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$		34	43		51		ns
t_{PHZ} , t_{PLZ}	Maximum Disable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	15	21	26		32		ns
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Times			12	15		18		ns
C_{PD}	Power Dissipation Capacitance (Note 5)		44						pF
C_{IN}	Maximum Input Capacitance		5	10	10		10		pF

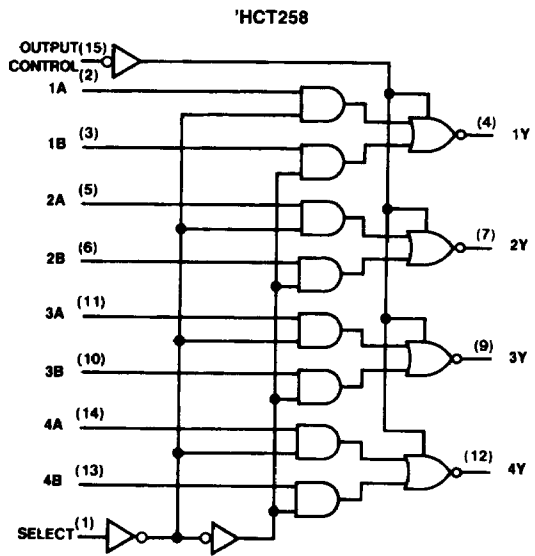
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams

MM54HCT257/MM74HCT257/MM54HCT258/MM74HCT258



TL/F/6121-3



TL/F/6121-4