

# 74F253

## Dual 4-Input Multiplexer with 3-STATE Outputs

### General Description

The 74F253 is a dual 4-input multiplexer with 3-STATE outputs. It can select two bits of data from four sources using common select inputs. The output may be individually switched to a high impedance state with a HIGH on the respective Output Enable (OE) inputs, allowing the outputs to interface directly with bus oriented systems.

### Features

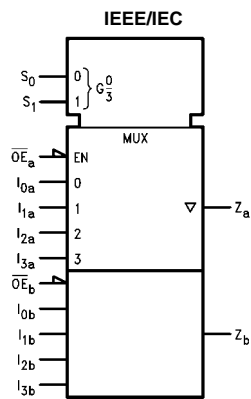
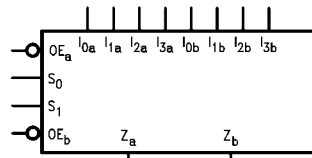
- Multifunction capability
- Non-inverting 3-STATE outputs

### Ordering Code:

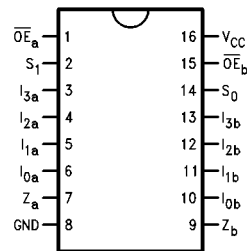
| Order Number | Package Number | Package Description   |
|--------------|----------------|---|
| 74F253SC     | M16A           | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| 74F253SJ     | M16D           | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide               |
| 74F253PC     | N16E           | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide       |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



74F253 Dual 4-Input Multiplexer with 3-STATE Outputs

## Unit Loading/Fan Out

| Pin Names         | Description                             | U.L.<br>HIGH/LOW | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
|-------------------|---|------------------|---|
| $I_{0a}-I_{3a}$   | Side A Data Inputs                      | 1.0/1.0          | 20 $\mu A$ /-0.6 mA                             |
| $I_{0b}-I_{3b}$   | Side B Data Inputs                      | 1.0/1.0          | 20 $\mu A$ /-0.6 mA                             |
| $S_0-S_1$         | Common Select Inputs                    | 1.0/1.0          | 20 $\mu A$ /-0.6 mA                             |
| $\overline{OE}_a$ | Side A Output Enable Input (Active LOW) | 1.0/1.0          | 20 $\mu A$ /-0.6 mA                             |
| $\overline{OE}_b$ | Side B Output Enable Input (Active LOW) | 1.0/1.0          | 20 $\mu A$ /-0.6 mA                             |
| $Z_a, Z_b$        | 3-STATE Outputs                         | 150/40(33.3)     | -3 mA/24 mA (20 mA)                             |

## Functional Description

This device contains two identical 4-input multiplexers with 3-STATE outputs. They select two bits from four sources selected by common Select inputs ( $S_0, S_1$ ). The 4-input multiplexers have individual Output Enable ( $\overline{OE}_a, \overline{OE}_b$ ) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot S_1 \cdot S_0)$$

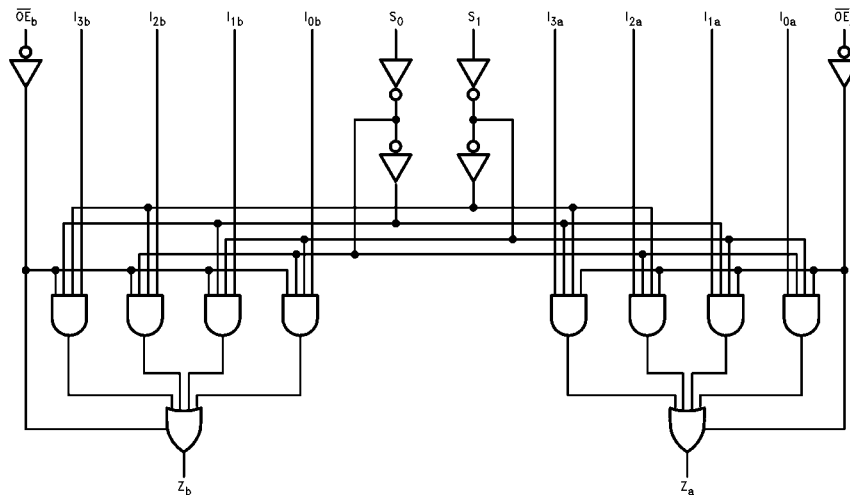
If the outputs of 3-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-STATE devices whose outputs are tied together are designed so that there is no overlap.

## Truth Table

| Select Inputs |       | Data Inputs |       |       |       | Output Enable   | Output |
|---------------|-------|-------------|-------|-------|-------|-----------------|--------|
| $S_0$         | $S_1$ | $I_0$       | $I_1$ | $I_2$ | $I_3$ | $\overline{OE}$ | $Z$    |
| X             | X     | X           | X     | X     | X     | H               | Z      |
| L             | L     | L           | X     | X     | X     | L               | L      |
| L             | L     | H           | X     | X     | X     | L               | H      |
| H             | L     | X           | L     | X     | X     | L               | L      |
| H             | L     | X           | H     | X     | X     | L               | H      |
| L             | H     | X           | X     | L     | X     | L               | L      |
| L             | H     | X           | X     | H     | X     | L               | H      |
| H             | H     | X           | X     | X     | L     | L               | L      |
| H             | H     | X           | X     | X     | H     | L               | H      |

Address inputs  $S_0$  and  $S_1$  are common to both sections.  
 H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

|  |                                      |
|--|--------------------------------------|
| Storage Temperature  | -65°C to +150°C                      |
| Ambient Temperature under Bias   | -55°C to +125°C                      |
| Junction Temperature under Bias  | -55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin                            | -0.5V to +7.0V                       |
| Input Voltage (Note 2)   | -0.5V to +7.0V                       |
| Input Current (Note 2)   | -30 mA to +5.0 mA                    |
| Voltage Applied to Output<br>in HIGH State (with V <sub>CC</sub> = 0V) |                                      |
| Standard Output  | -0.5V to V <sub>CC</sub>             |
| 3-STATE Output   | -0.5V to +5.5V                       |
| Current Applied to Output<br>in LOW State (Max)                        | twice the rated I <sub>OL</sub> (mA) |
| ESD Last Passing Voltage (Min)   | 4000V                                |

**Recommended Operating Conditions**

|                              |                |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C   |
| Supply Voltage               | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

| Symbol           | Parameter                         | Min  | Typ                      | Max          | Units | V <sub>CC</sub> | Conditions   |
|------------------|-----------------------------------|--|--------------------------|--------------|-------|-----------------|--|
| V <sub>IH</sub>  | Input HIGH Voltage                | 2.0  |                          |              | V     |                 | Recognized as a HIGH Signal  |
| V <sub>IL</sub>  | Input LOW Voltage                 |  |                          | 0.8          | V     |                 | Recognized as a LOW Signal   |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |  |                          | -1.2         | V     | Min             | I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub>  | Output HIGH Voltage               | 10% V <sub>CC</sub><br>10% V <sub>CC</sub><br>5% V <sub>CC</sub><br>5% V <sub>CC</sub> | 2.5<br>2.4<br>2.7<br>2.7 |              | V     | Min             | I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA<br>I <sub>OH</sub> = -1 mA<br>I <sub>OH</sub> = -3 mA |
| V <sub>OL</sub>  | Output LOW Voltage                | 10% V <sub>CC</sub>  |                          | 0.5          | V     | Min             | I <sub>OL</sub> = 24 mA  |
| I <sub>IH</sub>  | Input HIGH Current                |  |                          | 5.0          | μA    | Max             | V <sub>IN</sub> = 2.7V   |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test |  |                          | 7.0          | μA    | Max             | V <sub>IN</sub> = 7.0V   |
| I <sub>CEX</sub> | Output HIGH Leakage Current       |  |                          | 50           | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>   |
| V <sub>ID</sub>  | Input Leakage Test                | 4.75   |                          |              | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded  |
| I <sub>OD</sub>  | Output Leakage Circuit Current    |  |                          | 3.75         | μA    | 0.0             | V <sub>IOD</sub> = 150 mV<br>All Other Pins Grounded   |
| I <sub>IL</sub>  | Input LOW Current                 |  |                          | -0.6         | mA    | Max             | V <sub>IN</sub> = 0.5V   |
| I <sub>OZH</sub> | Output Leakage Current            |  |                          | 50           | μA    | Max             | V <sub>OUT</sub> = 2.7V  |
| I <sub>OZL</sub> | Output Leakage Current            |  |                          | -50          | μA    | Max             | V <sub>OUT</sub> = 0.5V  |
| I <sub>OS</sub>  | Output Short-Circuit Current      | -60<br>-100  |                          | -150<br>-225 | mA    | Max             | V <sub>OUT</sub> = 0V<br>V <sub>OUT</sub> = 0V   |
| I <sub>ZZ</sub>  | Bus Drainage Test                 |  |                          | 500          | μA    | 0.0V            | V <sub>OUT</sub> = V <sub>CC</sub>   |
| I <sub>CCH</sub> | Power Supply Current              |  | 11.5                     | 16           | mA    | Max             | V <sub>O</sub> = HIGH  |
| I <sub>CCL</sub> | Power Supply Current              |  | 16                       | 23           | mA    | Max             | V <sub>O</sub> = LOW   |
| I <sub>CCZ</sub> | Power Supply Current              |  | 16                       | 23           | mA    | Max             | V <sub>O</sub> = HIGH Z  |

## AC Electrical Characteristics

| Symbol    | Parameter           | $T_A = +25^\circ\text{C}$<br>$V_{CC} = 5.0\text{V}$<br>$C_L = 50\text{ pF}$ |     |      | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$<br>$V_{CC} = 5.0\text{V}$<br>$C_L = 50\text{ pF}$ |      | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$<br>$V_{CC} = 5.0\text{V}$<br>$C_L = 50\text{ pF}$ |      | Units |
|-----------|---------------------|---|-----|------|--|------|---|------|-------|
|           |                     | Min   | Typ | Max  | Min  | Max  | Min   | Max  |       |
| $t_{PLH}$ | Propagation Delay   | 4.5   | 8.5 | 11.5 | 3.5  | 15.0 | 4.5   | 13.0 | ns    |
| $t_{PHL}$ | $S_n$ to $Z_n$      | 3.0   | 6.5 | 9.0  | 2.5  | 11.0 | 3.0   | 10.0 |       |
| $t_{PLH}$ | Propagation Delay   | 3.0   | 5.5 | 7.0  | 2.5  | 9.0  | 3.0   | 8.0  | ns    |
| $t_{PHL}$ | $I_n$ to $Z_n$      | 2.5   | 4.5 | 6.0  | 2.5  | 8.0  | 2.5   | 7.0  |       |
| $t_{PZH}$ | Output Enable Time  | 3.0   | 6.0 | 8.0  | 2.5  | 10.0 | 3.0   | 9.0  | ns    |
| $t_{PZL}$ |                     | 3.0   | 6.0 | 8.0  | 2.5  | 10.0 | 3.0   | 9.0  |       |
| $t_{PHZ}$ | Output Disable Time | 2.0   | 3.7 | 5.0  | 2.0  | 6.5  | 2.0   | 6.0  | ns    |
| $t_{PLZ}$ |                     | 2.0   | 4.4 | 6.0  | 2.0  | 8.0  | 2.0   | 7.0  |       |

**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**

M16A (REV H)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

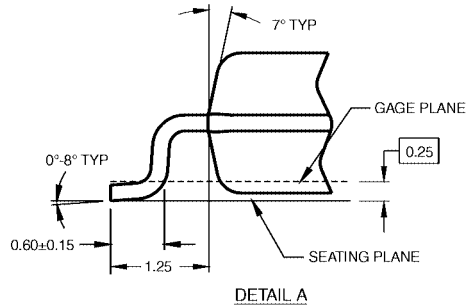
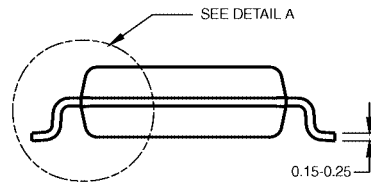


DIMENSIONS ARE IN MILLIMETERS

NOTES:

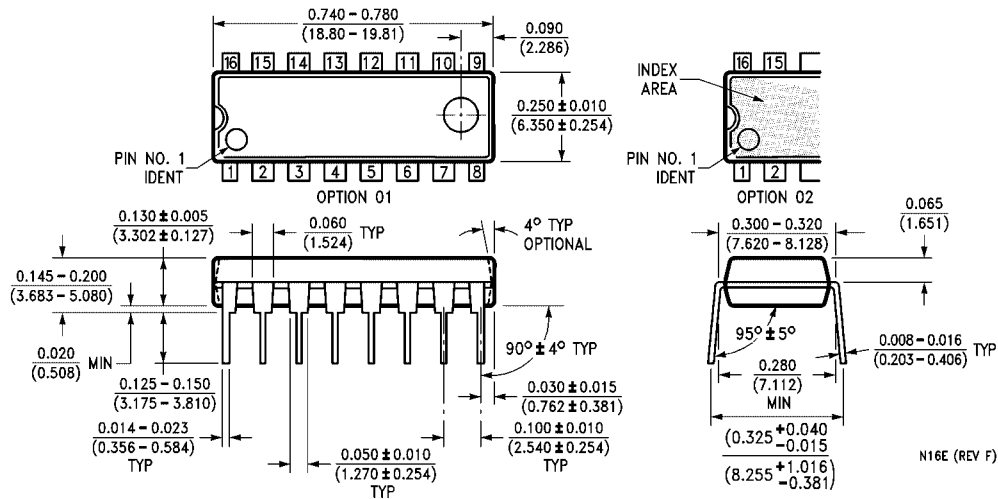
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)