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# DS90CP02

## 1.5 Gbps 2x2 LVDS Crosspoint Switch

### General Description

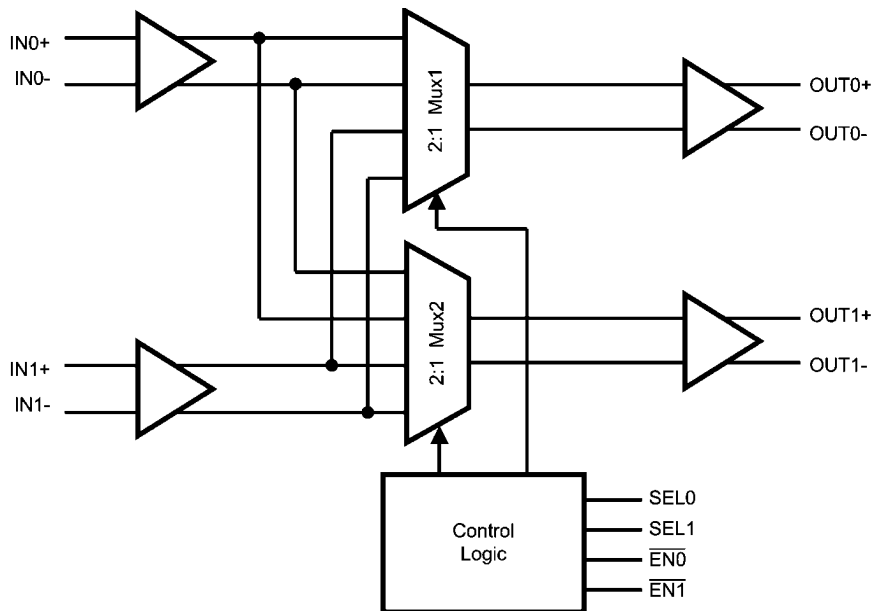
The DS90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output.

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

### Features

- 1.5 Gbps per channel
- Low power: 70 mA in dual repeater mode @ 1.5 Gbps
- Low output jitter
- Non-blocking architecture allows 1:2 splitter, 2:1 mux, crossover, and dual buffer configurations
- Flow-through pinout
- LVDS/BLVDS/CML/LVPECL inputs, LVDS Outputs
- Single 3.3V supply
- Separate control of inputs and outputs allows for power savings
- Industrial -40 to +85°C temperature range
- 28-lead LLP-28 space saving package

### Block Diagram



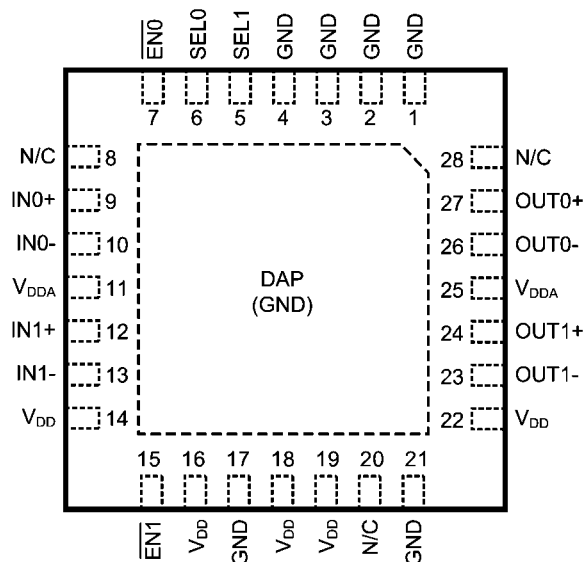
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FIGURE 1. DS90CP02 Block Diagram

## Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
<b>DIFFERENTIAL INPUTS COMMON TO ALL MUXES</b>			
IN0+	9	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
IN0-	10		
IN1+	12	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
IN1-	13		
<b>SWITCHED DIFFERENTIAL OUTPUTS</b>			
OUT0+	27	O, LVDS	Inverting and non-inverting differential outputs. OUT0± can be connected to any one pair IN0±, or IN1±. LVDS compatible .
OUT0-	26		
OUT1+	24	O, LVDS	Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN0±, or IN1±. LVDS compatible .
OUT1-	23		
<b>DIGITAL CONTROL INTERFACE</b>			
SEL0, SEL1	6 5	I, LVTTTL	Select Control Inputs
EN0, EN1	7 15	I, LVTTTL	Output Enable Inputs
N/C	8, 20, 28		Not Connected
<b>POWER</b>			
V <sub>DD</sub>	11, 14, 16, 18, 19, 22, 25	I, Power	V <sub>DD</sub> = 3.3V ±0.3V. At least 4 low ESR 0.01 μF bypass capacitors should be connected from V <sub>DD</sub> to GND plane.
GND	DAP, 1, 2, 3, 4, 17, 21	I, Power	Ground reference to LVDS and CMOS circuitry. For the LLP package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the LLP-28 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

## Connection Diagram



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LLP Top View  
DAP = GND

## Configuration Select Truth Table

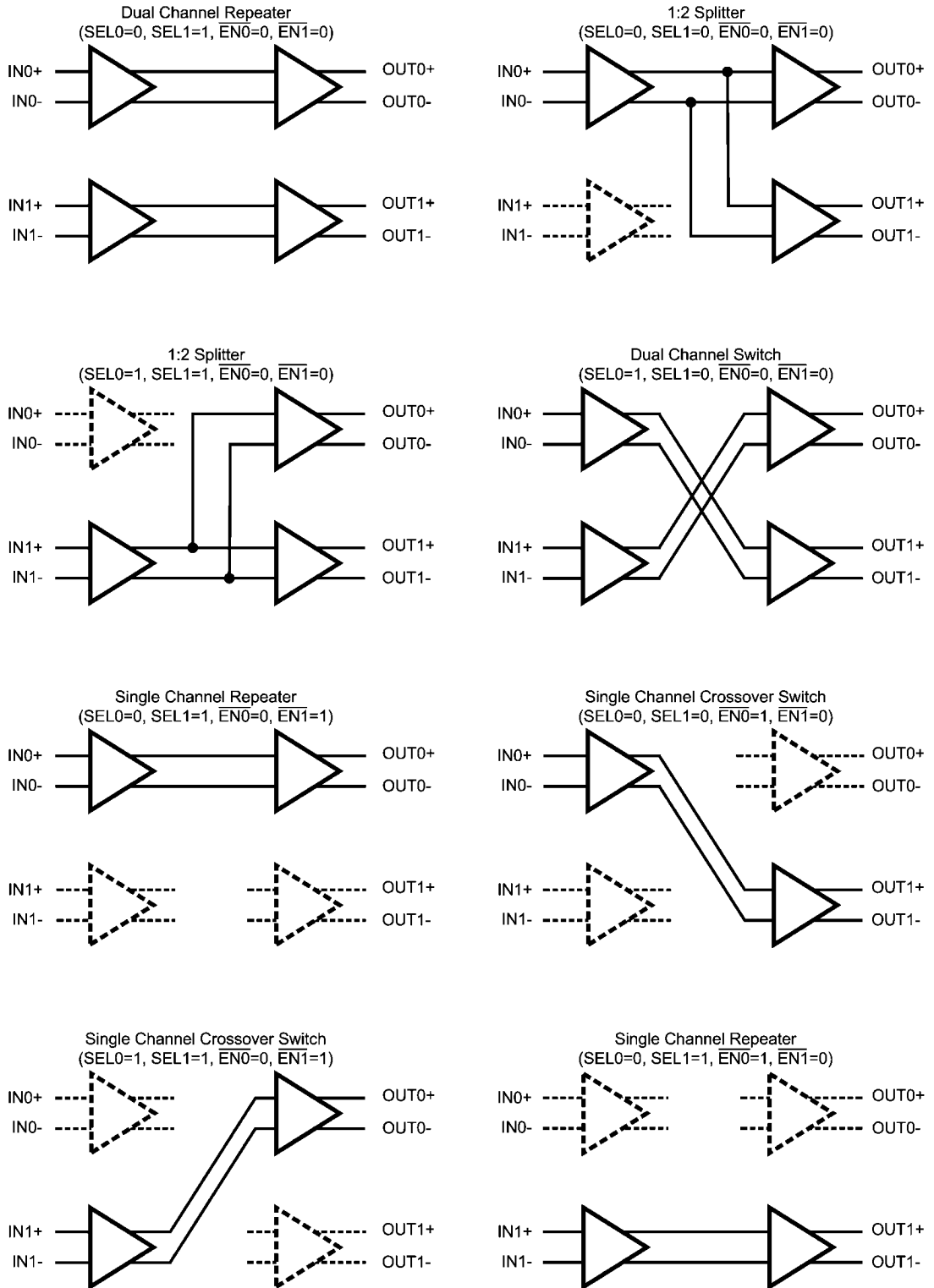
SEL0	SEL1	$\overline{EN0}$	$\overline{EN1}$	OUT0	OUT1	Mode
0	0	0	0	IN0	IN0	1:2 Splitter (IN1 powered down)
0	1	0	0	IN0	IN1	Dual Channel Repeater
1	0	0	0	IN1	IN0	Dual Channel Switch
1	1	0	0	IN1	IN1	1:2 Splitter (IN0 powered down)
0	1	0	1	IN0	PD	Single Channel Repeater (Channel 1 powered down)
1	1	0	1	IN1	PD	Single Channel Switch (IN0 and OUT1 powered down)
0	0	1	0	PD	IN0	Single Channel Switch (IN1 and OUT0 powered down)
0	1	1	0	PD	IN1	Single Channel Repeater (Channel 0 powered down)
X	X	1	1	PD	PD	Both Channels in Power Down Mode
0	0	0	1			Invalid State*
1	0	0	1			Invalid State*
1	0	1	0			Invalid State*
1	1	1	0			Invalid State*

PD = Power Down mode to minimize power consumption

X = Don't Care

\* Entering these states is not forbidden, however device operation is not defined in these states.

# Application Information



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FIGURE 2. DS90CP02 Configuration Select Decode

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{DD}$ )	-0.3V to +4.0V
CMOS Input Voltage	-0.3V to ( $V_{DD} + 0.3V$ )
LVDS Receiver Input Voltage	-0.3V to +3.6V
LVDS Driver Output Voltage	-0.3V to +3.6V
LVDS Output Short Circuit Current	40mA
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 4sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
LLP-28	4.31 W
Derating above 25°C	

LLP-28	34.5 mW/°C
Thermal Resistance, $\theta_{JA}$	
LLP-28	29°C/W
ESD Rating	
HBM, 1.5 k $\Omega$ , 100 pF	6.5 kV
EIAJ, 0 $\Omega$ , 200 pF	>250V

**Recommended Operating Conditions**

	Min	Typ	Max	Unit
Supply Voltage ( $V_{DD} - GND$ )	3.0	3.3	3.6	V
Receiver Input Voltage	0		3.6	V
Operating Free Air Temperature	-40	25	85	°C
Junction Temperature			150	°C

**Electrical Characteristics**

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
<b>LVTTTL DC SPECIFICATIONS (SEL0, SEL1, EN1, EN2)</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{DD}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$I_{IH}$	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	-10		+10	$\mu$ A
$I_{IL}$	Low Level Input Current	$V_{IN} = V_{SS}, V_{DD} = V_{DDMAX}$	-10		+10	$\mu$ A
$C_{IN1}$	Input Capacitance	Any Digital Input Pin to $V_{SS}$		3.5		pF
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA	-1.5	-0.8		V
<b>LVDS INPUT DC SPECIFICATIONS (IN0<math>\pm</math>, IN1<math>\pm</math>)</b>						
$V_{TH}$	Differential Input High Threshold (Note 3)	$V_{CM} = 0.8V$ or $1.2V$ or $3.55V$ , $V_{DD} = 3.6V$		0	100	mV
$V_{TL}$	Differential Input Low Threshold	$V_{CM} = 0.8V$ or $1.2V$ or $3.55V$ , $V_{DD} = 3.6V$	-100	0		mV
$V_{ID}$	Differential Input Voltage	$V_{CM} = 0.8V$ to $3.55V$ , $V_{DD} = 3.6V$	100			mV
$V_{CMR}$	Common Mode Voltage Range	$V_{ID} = 150$ mV, $V_{DD} = 3.6V$	0.05		3.55	V
$C_{IN2}$	Input Capacitance	IN+ or IN- to $V_{SS}$		3.5		pF
$I_{IN}$	Input Current	$V_{IN} = 3.6V$ , $V_{DD} = V_{DDMAX}$ or $0V$	-10		+10	$\mu$ A
		$V_{IN} = 0V$ , $V_{DD} = V_{DDMAX}$ or $0V$	-10		+10	$\mu$ A
<b>LVDS OUTPUT DC SPECIFICATIONS (OUT0<math>\pm</math>, OUT1<math>\pm</math>)</b>						
$V_{OD}$	Differential Output Voltage, 0% Pre-emphasis (Note 3)	$R_L = 100\Omega$ between OUT+ and OUT-	250	400	575	mV
$\Delta V_{OD}$	Change in $V_{OD}$ between Complementary States		-35		35	mV
$V_{OS}$	Offset Voltage (Note 4)		1.09	1.25	1.475	V
$\Delta V_{OS}$	Change in $V_{OS}$ between Complementary States		-35		35	mV
$I_{OS}$	Output Short Circuit Current, One Complementary Output	OUT+ or OUT- Short to GND		-60	-90	mA
$C_{OUT}$	Output Capacitance	OUT+ or OUT- to GND when TRI- STATE		5.5		pF

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
<b>SUPPLY CURRENT (Static)</b>						
$I_{CC0}$	Supply Current	All inputs and outputs enabled and active, terminated with differential load of $100\Omega$ between OUT+ and OUT-.		42	60	mA
$I_{CC1}$	Supply Current - one channel powered down	Single channel crossover switch or single channel repeater modes (1 channel active, one channel in power down mode)		22	30	mA
$I_{CC2}$	Supply Current - one input powered down	Splitter mode (One input powered down, both outputs active)		30	40	mA
$I_{CCZ}$	TRI-STATE Supply Current	Both input/output Channels in Power Down Mode		1.4	2.5	mA
<b>SWITCHING CHARACTERISTICS—LVDS OUTPUTS (Figures 3, 4)</b>						
$t_{LHT}$	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of $V_{OD}$ .	70	150	215	ps
$t_{HLT}$	Differential High to Low Transition Time		50	135	180	ps
$t_{PLHD}$	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% $V_{OD}$ between input to output.	0.5	2.4	3.5	ns
$t_{PHLD}$	Differential High to Low Propagation Delay		0.5	2.4	3.5	ns
$t_{SKD1}$	Pulse Skew	$ t_{PLHD} - t_{PHLD} $		55	120	ps
$t_{SKCC}$	Output Channel to Channel Skew	Difference in propagation delay ( $t_{PLHD}$ or $t_{PHLD}$ ) among all output channels in Splitter mode (any one input to all outputs).	0	130	315	ps
$t_{JIT}$	Jitter (Note 5)	RJ - Clock Pattern 750 MHz (Note 6)		1.4	2.5	psrms
		DJ - K28.5 Pattern 1.5 Gbps (Note 7)		42	75	psp-p
		TJ - PRBS 2 <sup>23</sup> -1 Pattern 1.5 Gbps (Note 8)		93	126	psp-p
$t_{ON}$	LVDS Output Enable Time	Time from $\overline{ENx}$ to OUT± change from TRI-STATE to active.	50	110	150	ns
$t_{OFF}$	LVDS Output Disable Time	Time from $\overline{ENx}$ to OUT± change from active to TRI-STATE.		5	12	ns
$t_{SW}$	LVDS Switching Time SELx to OUT±	Time from configuration select (SELx) to new switch configuration effective for OUT±.		110	150	ns

**Note 1:** "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

**Note 2:** Typical parameters are measured at  $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$ . They are for reference purposes, and are not production-tested.

**Note 3:** Differential output voltage  $V_{OD}$  is defined as  $ABS(OUT+ - OUT-)$ . Differential input voltage  $V_{ID}$  is defined as  $ABS(IN+ - IN-)$ .

**Note 4:** Output offset voltage  $V_{OS}$  is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

**Note 5:** Jitter is not production tested, but guaranteed through characterization on a sample basis.

**Note 6:** Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage =  $V_{ID} = 500mV$ , 50% duty cycle at 750MHz,  $t_r = t_f = 50ps$  (20% to 80%).

**Note 7:** Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage =  $V_{ID} = 500mV$ , K28.5 pattern at 1.5 Gbps,  $t_r = t_f = 50ps$  (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).

**Note 8:** Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage =  $V_{ID} = 500mV$ , 2<sup>23</sup>-1 PRBS pattern at 1.5 Gbps,  $t_r = t_f = 50ps$  (20% to 80%).

# Timing Diagrams

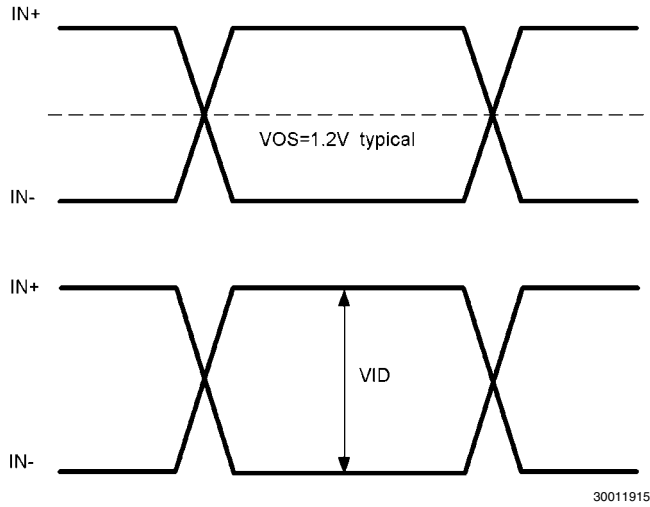


FIGURE 3. LVDS Signals

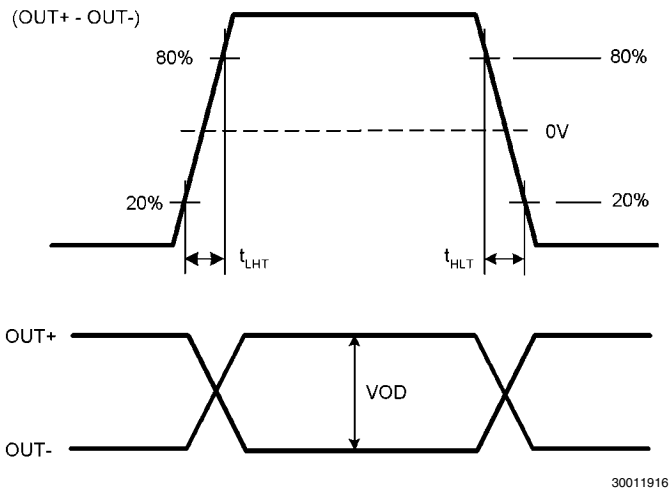


FIGURE 4. LVDS Output Transition Time

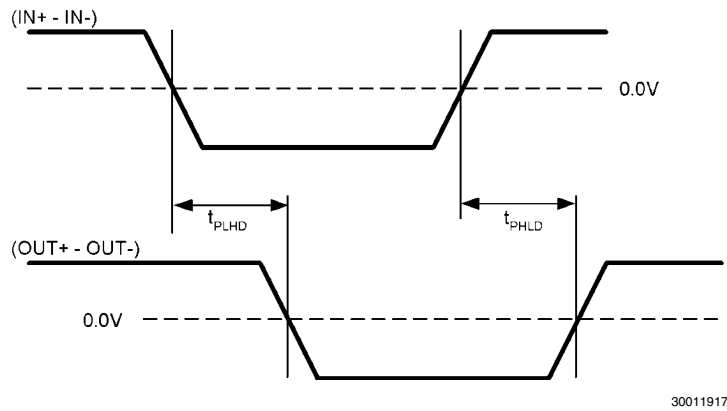


FIGURE 5. LVDS Output Propagation Delay



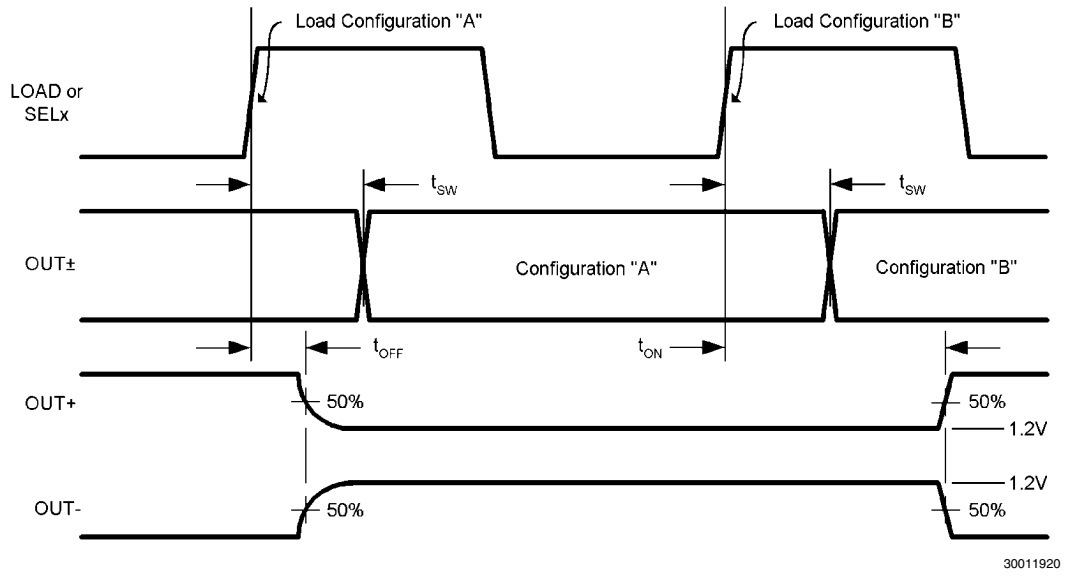
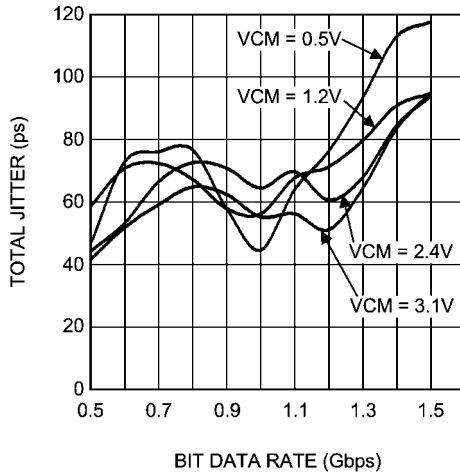


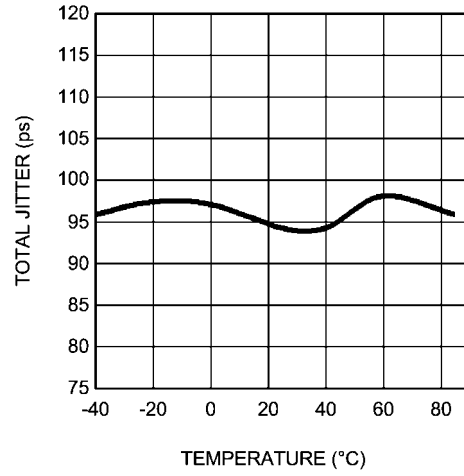
FIGURE 6. Configuration and Output Enable/Disable Timing

# Typical Performance

Total Jitter ( $T_J$ ) vs. Bit Data Rate



Total Jitter ( $T_J$ ) vs. Temperature



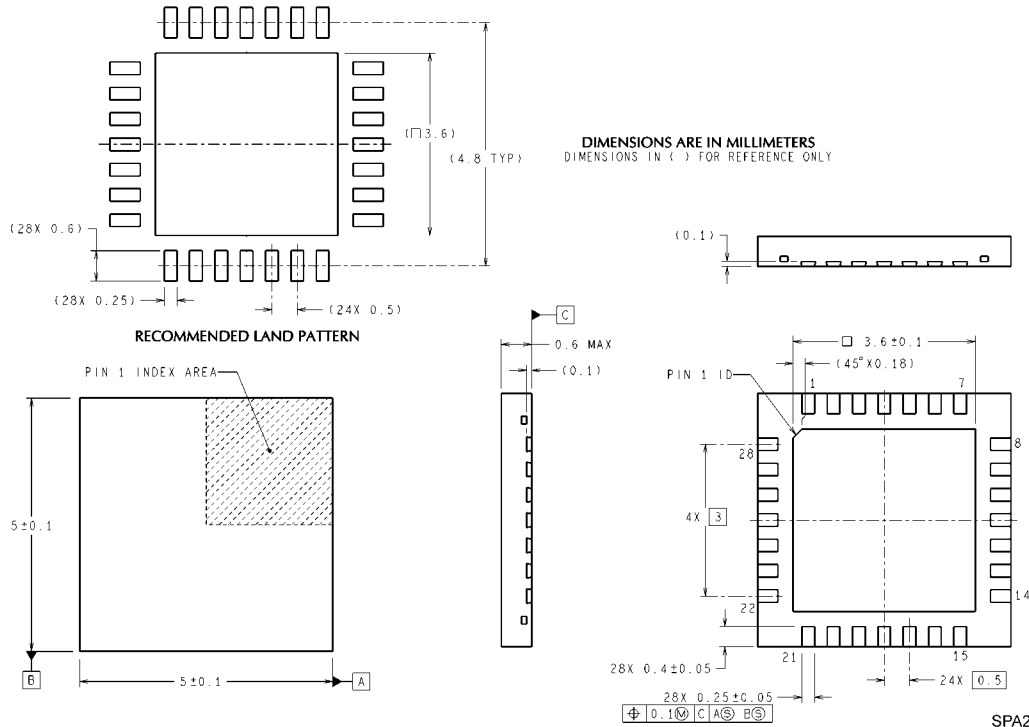
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Total Jitter measured at 0V differential while running a PRBS 2<sup>23</sup>-1 pattern in single channel repeater mode.  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$ ,  $V_{ID} = 0.5V$

30011943

Total Jitter measured at 0V differential while running a PRBS 2<sup>23</sup>-1 pattern in dual channel repeater mode.  $V_{CC} = 3.3V$ ,  $V_{ID} = 0.5V$ ,  $V_{CM} = 1.2V$ , 1.5 Gbps data rate

**Physical Dimensions** inches (millimeters) unless otherwise noted



SPA28A (Rev A)

**LLP, Plastic, QUAD,**  
**Order Number DS90CP02SP (1000 piece Tape and Reel),**  
**DS90CP02SPX (4500 piece Tape and Reel)**  
**NS Package Number SPA28A**

# Notes

## Notes

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LED Lighting	<a href="http://www.national.com/led">www.national.com/led</a>	Feedback/Support	<a href="http://www.national.com/feedback">www.national.com/feedback</a>
Voltage Reference	<a href="http://www.national.com/vref">www.national.com/vref</a>	Design Made Easy	<a href="http://www.national.com/easy">www.national.com/easy</a>
PowerWise® Solutions	<a href="http://www.national.com/powerwise">www.national.com/powerwise</a>	Solutions	<a href="http://www.national.com/solutions">www.national.com/solutions</a>
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