



Integrated Device Technology, Inc.

OCTAL 2:1 MULTIPLEXER BUS SWITCH

IDT74FST3390
IDT74FST32390
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Low switch on-resistance:
FST3xxx – 5Ω
FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- Available in 28-pin QSOP, SOIC and TSSOP

DESCRIPTION:

The FST3390/32390 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external

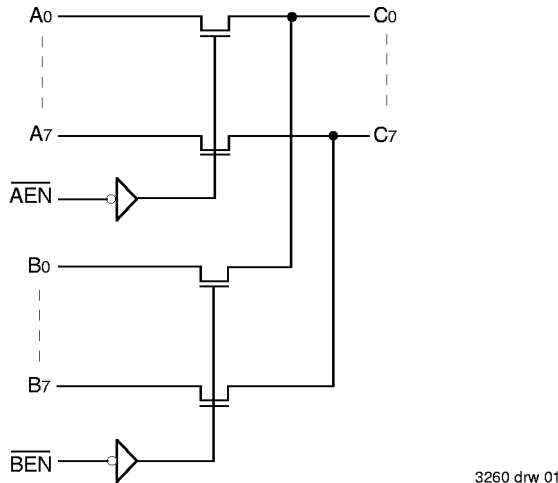
driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32390 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

The FST3390 and FST32390 are 8-bit TTL-compatible 2:1 bus multiplexers. $\overline{\text{AEN}} = 0$ connects port A to port C and $\overline{\text{BEN}} = 0$ connects port B to port C. This device can be used to connect ports A & B to a common bus on port C or to broadcast data on port C to both ports A and B.

FUNCTIONAL BLOCK DIAGRAM

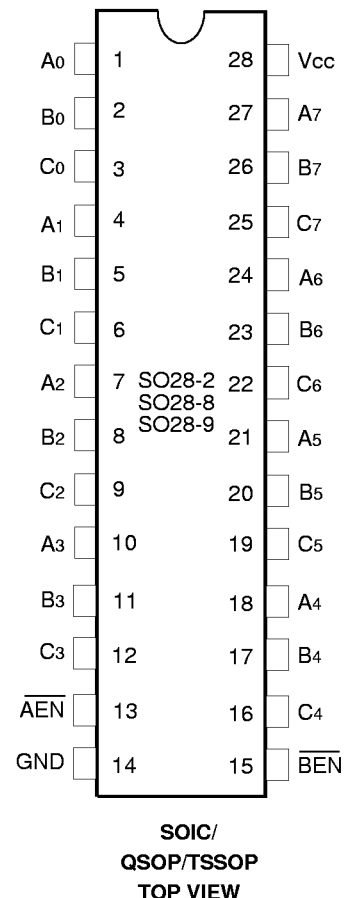


PIN DESCRIPTION

Pin Names	I/O	Description
A0-7	I/O	Bus A
B0-7	I/O	Bus B
C0-7	I/O	Bus C
$\overline{\text{AEN}}, \overline{\text{BEN}}$	I	Bus Switch Enable (Active LOW)

3260 tbl 01

PIN CONFIGURATION



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGES

AUGUST 1996

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	Maximum Continuous Channel Current	128	mA

NOTES:

3260 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC}, Control and Switch terminals.

FUNCTION TABLE

AEN	BEN	A	B	Description
H	H	Off	Off	Disconnect
L	H	On	Off	A to C
H	L	Off	On	B to C
L	L	On	On	A, B to C

3260 tbl 03

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions ⁽²⁾	Typ.	Unit
C _{IN}	Control Input Capacitance		4	pF
C _{I/O}	Switch Input/Output Capacitance	Switch Off		pF

NOTES:

3260 tbl 04

- Capacitance is characterized but not tested
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V	
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V	
I _{IH}	Input HIGH Current	V _{CC} = Max. V _I = V _{CC}	—	—	±1	μA	
I _{IL}	Input LOW Current		V _I = GND	—	—		±1
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = Max. V _O = V _{CC}	—	—	±1	μA	
I _{OZL}			V _O = GND	—	—		±1
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾	—	300	—	mA	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V	
R _{ON}	Switch On Resistance ⁽⁴⁾	V _{CC} = Min., V _{IN} = 0.0V I _{ON} = 30mA	3xxx	5	7	Ω	
			32xxx	17	28		40
		V _{CC} = Min., V _{IN} = 2.4V I _{ON} = 15mA	3xxx	—	10	15	Ω
			32xxx	20	35	48	
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V	—	—	±1	μA	
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _I = GND or V _{CC}	—	0.1	3	μA	

NOTES:

3260 Ink 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	1.5	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	30	40	μA/ MHz/ Switch
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open Enable Pin Toggling (8 Switches Toggling) f _i = 10MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	2.4	3.2	mA
			V _{IN} = 3.4 V _{IN} = GND	—	2.7	4.0	

NOTES:

3260 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD}$ (f_iN)
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_i = Input Frequency
 N = Number of Switches toggling at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Description	Condition ⁽¹⁾	Min. ⁽²⁾	Typ.	3390	32390	Unit
					Max.		
t _{PLH} t _{PHL}	Data Propagation Delay A, B to/from C ^(3,4)	C _L = 50pF R _L = 500Ω	—	—	0.25	1.25	ns
t _{PZH} t _{PZL}	Switch Turn on Delay AEN/BEN to A, B, C		1.5	—	6.5	7.5	ns
t _{PHZ} t _{PLZ}	Switch Turn off Delay AEN, BEN to A, B, C ⁽³⁾		1.5	—	5.5	5.5	ns
Q _C	Charge Injection ^(5,6)		—	1.5	—	—	pC

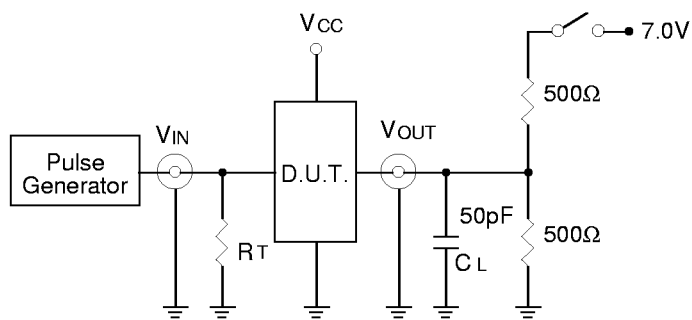
NOTES:

3260 tbl 07

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
- Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3260 Ink 03

SWITCH POSITION

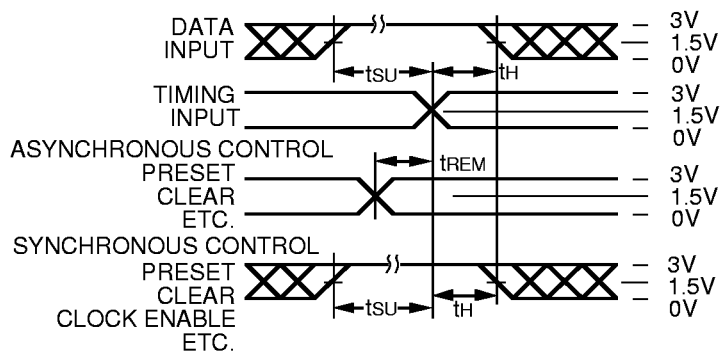
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

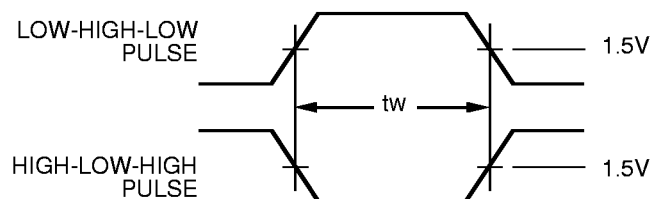
3260 Ink 08

SET-UP, HOLD AND RELEASE TIMES



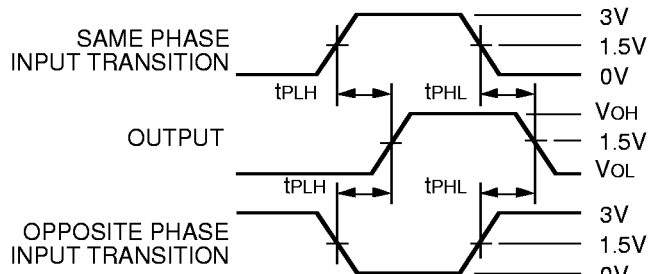
3260 Ink 04

PULSE WIDTH



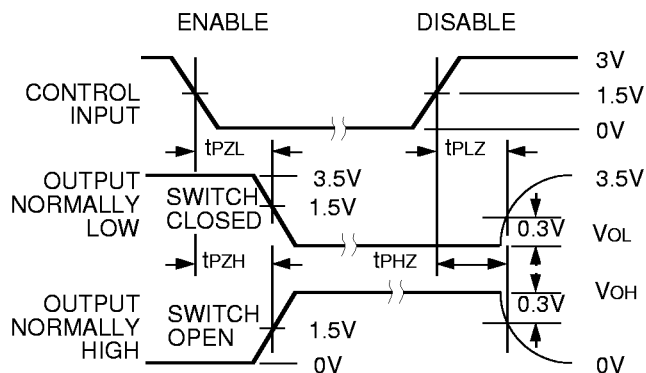
3260 Ink 05

PROPAGATION DELAY



3260 Ink 06

ENABLE AND DISABLE TIMES

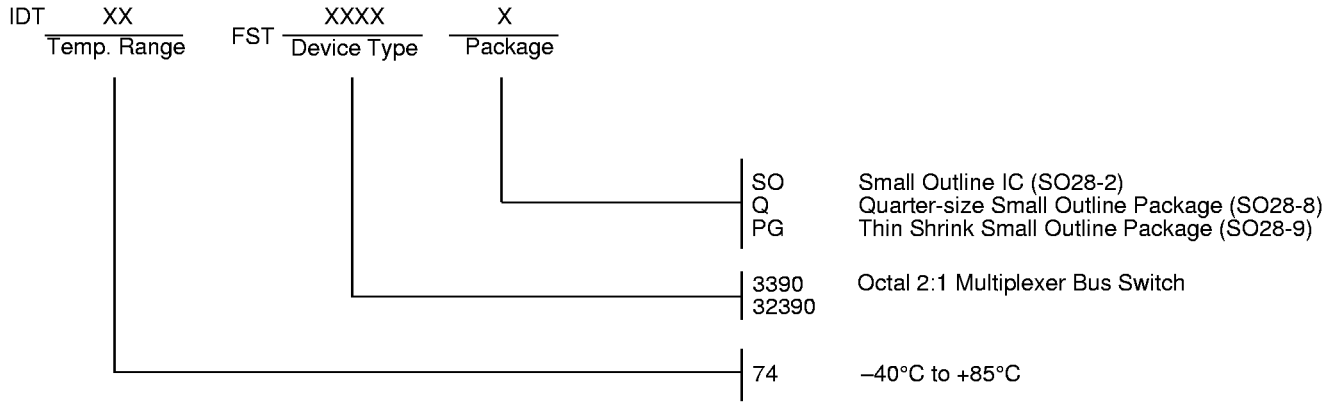


3260 Ink 07

NOTES:

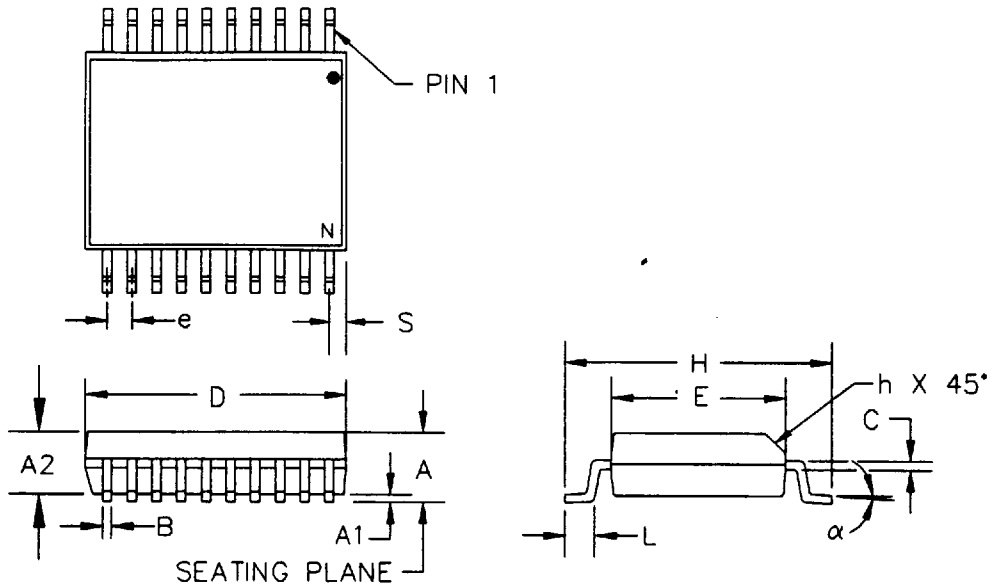
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns

ORDERING INFORMATION



3260 drw 08

QUARTER SIZE OUTLINE PACKAGE



NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. D & E REF DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" PER SIDE.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003" AT SEATING PLANE.

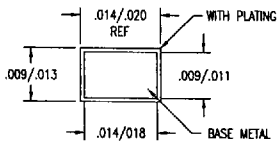
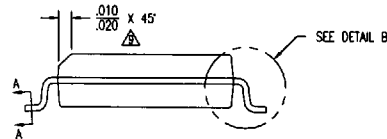
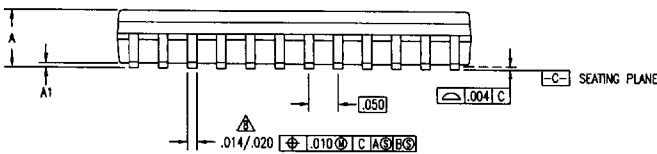
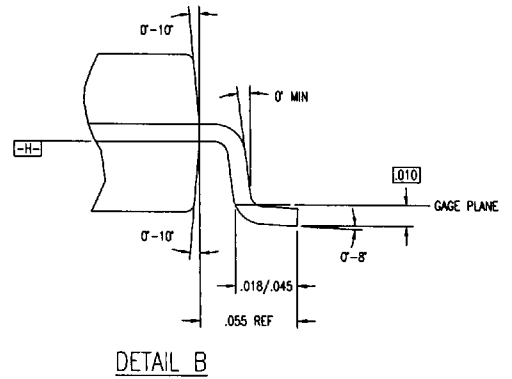
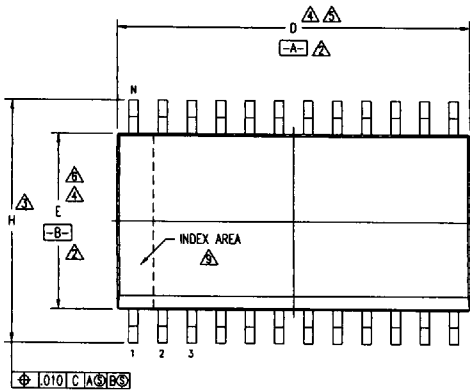
16-28 LEAD QSOP (.150" BODY WIDTH)

DWG #	S016-7		S020-8		S024-8		S028-8	
No. OF LD	16		20		24		28	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.068	.061	.068	.061	.068	.061	.068
A1	.004	.0098	.004	.0098	.004	.0098	.004	.0098
A2	.055	.061	.055	.061	.055	.061	.055	.061
B	.0078	.0122	.0078	.0122	.0078	.0122	.0078	.0122
C	.0075	.0098	.0075	.0098	.0075	.0098	.0075	.0098
D	.189	.196	.337	.344	.337	.344	.386	.393
e	.025 BSC		.025 BSC		.025 BSC		.025 BSC	
E	.150	.157	.150	.157	.150	.157	.150	.157
H	.230	.244	.230	.244	.230	.244	.230	.244
h	.010	.016	.010	.016	.010	.016	.010	.016
L	.016	.035	.016	.035	.016	.035	.016	.035
S	.002	.007	.050	.055	.025	.030	.025	.030
α	0°	8°	0°	8°	0°	8°	0°	8°


PACKAGE DIAGRAM OUTLINES

SOIC

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27843	06	REDRAW TO JEDEC FORMAT	03/15/95	



SECTION A-A

TOLERANCES UNLESS SPECIFIED		 Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 492-8874 TWR: 910-338-2070	
DECIMAL	ANGULAR	±	
XXX±			
XXXX±			
XXXX±			
APPROVALS	DATE	TITLE	PS PACKAGE OUTLINE
DRAWN	03/15/95	.300" BODY WIDTH SOIC	
CHECKED		.050" PITCH	
SIZE	DRAWING No.		REV
C	PSC-4007		06
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES


SOIC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

SYMBOL	DWG # S016-1				DWG # S018-1				DWG # S020-2				DWG # S024-2				DWG # S028-2			
	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE	JEDEC VARIATION			NOTE
	AA				AB				AC				AD				AE			
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104	
A1	.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012	
D	.403	.408	.413	4,5	.447	.454	.462	4,5	.497	.504	.511	4,5	.600	.607	.614	4,5	.700	.706	.712	4,5
E	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6
H	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3
N	16				18				20				24				28			

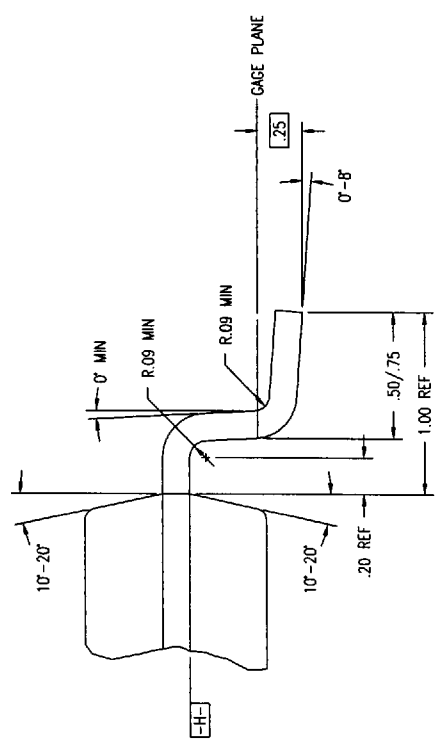
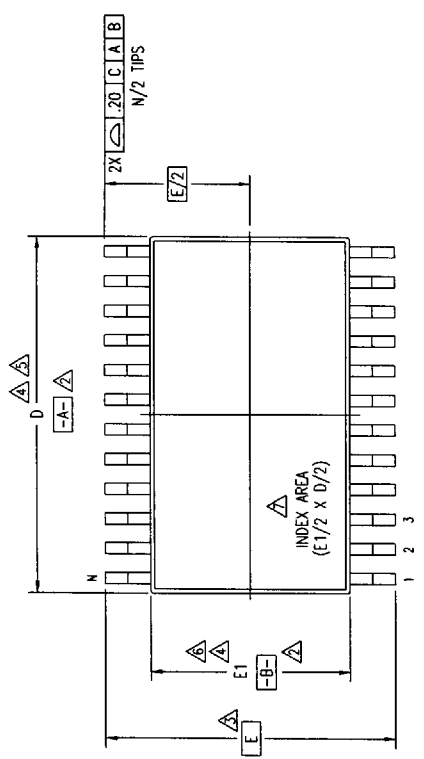
NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- △ DATUMS [-A-] AND [-B-] TO BE DETERMINED AT DATUM PLANE [-H-]
- △ DIMENSION H TO BE DETERMINED AT SEATING PLANE [-C-]
- △ DIMENSIONS D AND E ARE TO BE DETERMINED AT DATUM PLANE [-H-]
- △ DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- △ DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- △ LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- △ THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- 10 ALL DIMENSIONS ARE IN INCHES
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-013, VARIATION AA, AB, AC, AD & AE

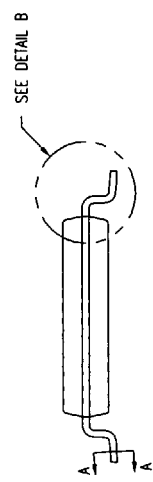
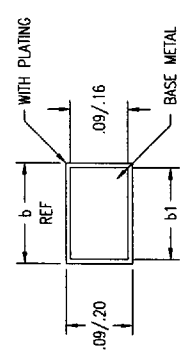
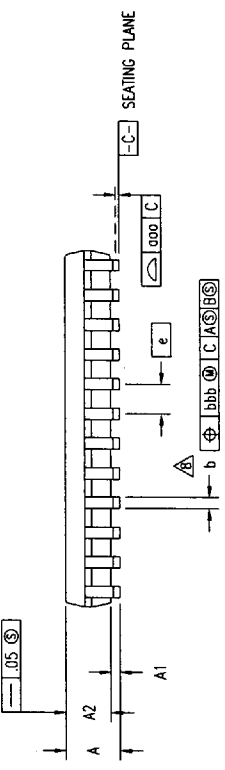
TOLERANCES UNLESS SPECIFIED		 Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 482-8874 TWR: 910-338-2070
DECIMAL	ANGULAR	
XXX±	±	
XXXX±		
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>dt</i>	03/15/98	PS PACKAGE OUTLINE
CHECKED		.300" BODY WIDTH SOIC
		.050" PITCH
		SIZE C DRAWING No. PSC-4007
		REV 06
DO NOT SCALE DRAWING		

4825771 0021977 67T

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
28794	00	INITIAL RELEASE	04/01/96	T. VU
29022	01	DELETE 4B & 56 LD	06/20/96	



DETAIL B

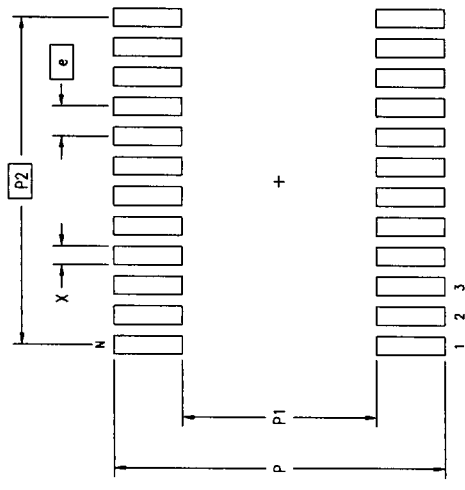


SEE DETAIL B

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX±	INTEGRATED DEVICE TECHNOLOGY, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8116 FAX: (408) 492-8874 TWM: 910-338-2070	TITLE PG PACKAGE OUTLINE	
		DATE 01/15/96	4.4 mm BODY WIDTH TSSOP .65 mm LEAD PITCH
APPROVALS DRAWN JY CHECKED	DRAWING No. PSC-4056	SIZE C	REV 01
DO NOT SCALE DRAWING			SHEET 1 OF 2

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
28794	00	INITIAL RELEASE	04/01/96	T. VU
28022	01	DELETE 48 & 56 LD	06/20/96	

LAND PATTERN DIMENSIONS



SYMBOL	JEDEC VARIATION AC			JEDEC VARIATION AD			JEDEC VARIATION AE			N	T	E
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX			
A	.05	-	1.20	.05	-	.15	.05	-	1.20			
A1	.80	1.00	1.05	.80	1.00	1.05	.80	1.00	1.05			
A2	6.40	6.50	6.60	7.70	7.80	7.90	9.60	9.70	9.80	4.5		4.5
D	6.40 BSC			6.40 BSC			6.40 BSC			3		3
E	4.30	4.40	4.50	4.30	4.40	4.50	4.30	4.40	4.50	4.6		4.6
E1	.65 BSC			.65 BSC			.65 BSC					
e	.19	-	.30	.19	-	.30	.19	-	.30			
b1	.19	.22	.25	.19	.22	.25	.19	.22	.25			
ooo	-	-	.10	-	-	.10	-	-	.10			
bbb	-	-	.10	-	-	.10	-	-	.10			
N	20			24			28					

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AC, AD & AE

	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40
P2	5.85 BSC	7.15 BSC	7.15 BSC	8.45 BSC		
X	.30	.50	.30	.50	.30	.50
e	.65 BSC	.65 BSC	.65 BSC	.65 BSC		
N	20		24		28	

Integrated Device Technology, Inc.
 2875 Stender Way, Santa Clara, CA 95054
 PHONE: (408) 727-6116
 FAX: (408) 492-8674 TWR: 910-338-2070

TOLERANCES UNLESS SPECIFIED
 DECIMAL ANGULAR
 XXX± ±
 XXXXX± ±

APPROVALS DATE 01/15/96
 DRAWN BY
 CHECKED

TITLE PC PACKAGE OUTLINE
 4.4 mm BODY WIDTH TSSOP
 .65 mm LEAD PITCH

SIZE C
 DRAWING NO. PSC-4056
 REV 01

DO NOT SCALE DRAWING SHEET 2 OF 2

126-A