High Speed CMOS 8-Bit Universal Shift Register

QS54/74FCT299T

FEATURES/BENEFITS

- Pin and function compatible to the 74F299 74FCT299 and 74ALS299
- CMOS power levels: <7.5 mW static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883
- I_{OL} = 48 mA Com., 32 mA Mil.
- Standard and A speed grades with 7.2 ns t_{PD} for A

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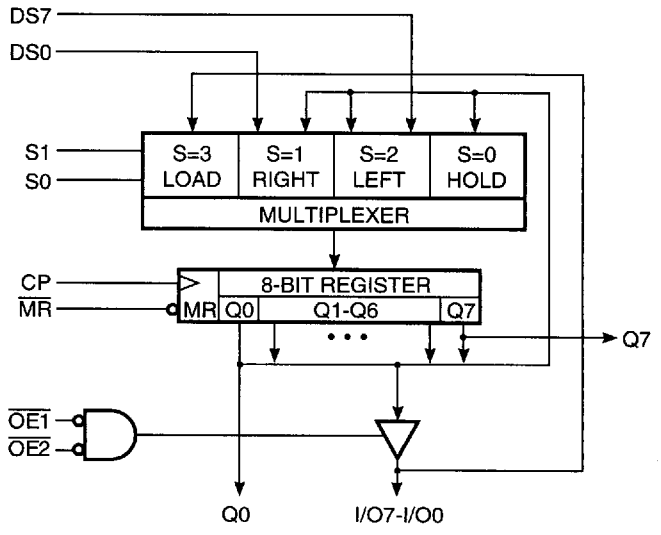
DESCRIPTION

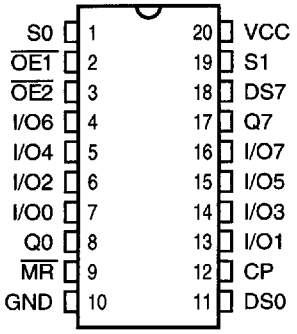
The QSFCT299T is a high-speed CMOS 8-bit universal shift register. The contents of the 8-bit register may be loaded from a bus, shifted left or right, or gated to the bus. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001).

FUNCTIONAL BLOCK DIAGRAM

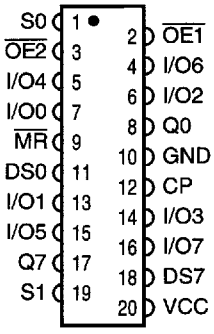


PIN CONFIGURATIONS (All Pins Top View)

DIP, SOIC, QSOP, HQSOP



ZIP



PIN DESCRIPTION

Name	I/O	Description
I/O7-I/O0	I/O	Data I/O Bus
S1, S0	I	Function Select
CP	I	Clock
Q7, Q0	O	Shift Out
DS7, DS0	I	Shift In
$\overline{OE1}$, $\overline{OE2}$	I	Output Enables
$\overline{MR}$	I	Master Reset

FUNCTION TABLE

Inputs				Outputs			
$\overline{MR}$	S1	S0	CP	Q7	Q6-Q1	Q0	Function
L	X	X	X	L	LLLLLL	L	Reset
H	L	L	↑	Q7	Q6-Q1	Q0	Hold Data
H	L	H	↑	DS7	Q7-Q2	Q1	Shift Right
H	H	L	↑	Q6	Q5-Q0	DS0	Shift Left
H	H	H	↑	I/O7	I/O6-1	I/O0	Load

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with V_{IN} < 0	–20 mA
DC Output Diode Current with V_{OUT} < 0	–50 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SOIC	QSOP	PDIP	ZIP	Unit
1-3, 9, 11, 12, 18, 19	4	4	5	7	pF
8, 17	6	6	7	9	pF
4-7, 13-16	8	8	9	10	pF

Note: Capacitance is characterized but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = Max., freq = 0 0V ≤ V_{IN} ≤ 0.2V or Vcc-0.2V ≤ V_{IN} ≤ Vcc	—	1.5	mA
ΔIcc	Supply Current per Input @ TTL HIGH	Vcc = Max., V_{IN} = 3.4V, freq = 0[2]	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	Vcc = Max., Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or Vcc[3,4]	—	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. Ic can be computed using the above parameters as explained in the Technical Overview section.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military T_A = –55°C to 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	Vcc = Max., $0 \le V_{IN} < V_{CC}$	—	—	5	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	Vcc = Max., $0 \le V_{IN} \le V_{CC}$	—	—	5	µA
I_{OS}	Short Circuit Current	Vcc = Max., V_{OUT} = GND(2,3)	–60	—	—	mA
V_{IC}	Input Clamp Voltage	Vcc = Min., I_{IN} = –18 mA, T_A = 25°C(3)	—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	Vcc = Min. I_{OH} = –12 mA (MIL) I_{OH} = –15 mA (COM)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage	Vcc = Min. I_{OL} = 32 mA (MIL) I_{OL} = 48 mA (COM)	— —	— —	0.50 0.50	V

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted and the duration is ≤1 second.
3. These parameters are guaranteed by design but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5% Military T_A = −55°C to 125°C, Vcc = 5.0V ± 10%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]		299 Min	299 Max	299A Min	299A Max	Unit
t_{CPQ}	Propagation Delay CP to Qi	COM	2	10	2	7.2	ns
		MIL	2	14	2	9.5	
t_{CPI}	Propagation Delay CP to I/O	COM	2	12	2	7.2	ns
		MIL	2	12	2	9.5	
t_{MRQ}	Propagation Delay $\overline{MR}$ to Qi	COM	2	10	2	7.2	ns
		MIL	2	10.5	2	9.5	
t_{MRI}	Propagation Delay $\overline{MR}$ to I/O	COM	2	15	2	8.7	ns
		MIL	2	15	2	11.5	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O	COM	1.5	11	1.5	6.5	ns
		MIL	1.5	15	1.5	7.5	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O	COM[2]	1.5	7	1.5	5.5	ns
		MIL[2]	1.5	9	1.5	6.5	
$t_{S0,1}$	Setup Time S0, S1 to CP	COM	7.5		3.5		ns
		MIL	7.5		4.0		
$t_{H0,1}$	Hold Time S0, S1 to CP	COM	1		1		ns
		MIL	1		1		
t_S	Setup Time I/O or DSn to CP	COM	5.5		4.0		ns
		MIL	5.5		4.5		
t_H	Hold Time I/O or DSn to CP	COM	1.5		1.5		ns
		MIL	1.5		1.5		
t_{WCP}	CP Pulse Width HIGH or LOW	COM[2]	7		5		ns
		MIL[2]	7		6		
t_{WMR}	$\overline{MR}$ Pulse Width LOW	COM[2]	7		5		ns
		MIL[2]	7		6		
t_{REM}	Recovery Time $\overline{MR}$ to CP	COM	7		5		ns
		MIL	7		6		

Notes:
1. Minimums guaranteed but not tested. For all parameters except t_S, t_H, and t_{REM}.
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.