

TC74VHC164F, TC74VHC164FN, TC74VHC164FT, TC74VHC164FK

8-Bit Shift Register (S-IN, P-OUT)

The TC74VHC164 is an advanced high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding CLEAR input.

Two serial data inputs (A, B) are provided so that one may be used as a data enable.

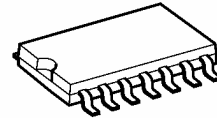
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

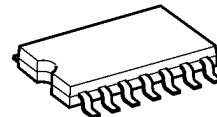
- High speed: $f_{max} = 175$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (opr) = 2$ to 5.5 V
- Low noise: $V_{OLP} = 0.8$ V (max)
- Pin and function compatible with 74ALS164

Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74VHC164F

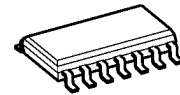


SOP14-P-300-1.27A



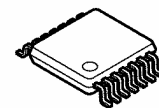
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TC74VHC164FN



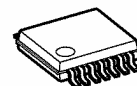
SOL14-P-150-1.27

TC74VHC164FT



TSSOP14-P-0044-0.65A

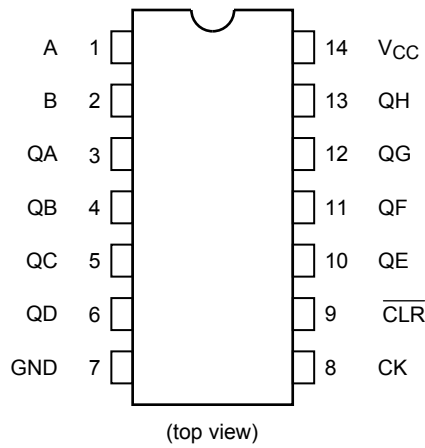
TC74VHC164FK



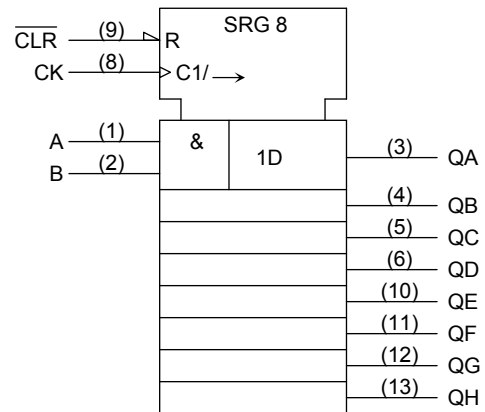
VSSOP14-P-0030-0.50

Weight	
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOP14-P-300-1.27	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)
VSSOP14-P-0030-0.50	: 0.02 g (typ.)

Pin Assignment



IEC Logic Symbol



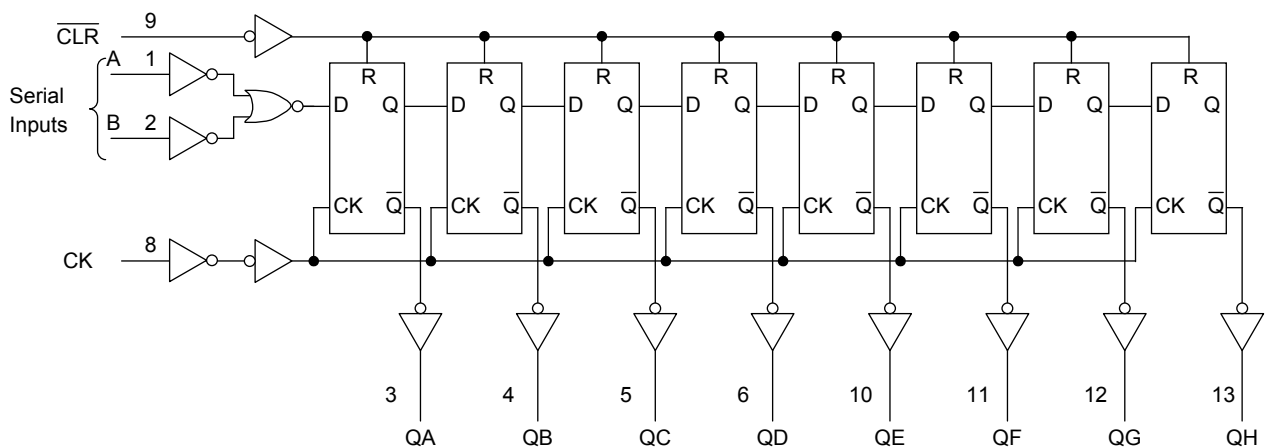
Truth Table

Inputs				Outputs			
$\overline{\text{CLR}}$	CK	Serial IN		QA	QB	...	QH
		A	B				
L	X	X	X	L	L	...	L
H		X	X	No Change			
H		L	X	L	QA _n	...	QG _n
H		X	L	L	QA _n	...	QG _n
H		H	H	H	QA _n	...	QG _n

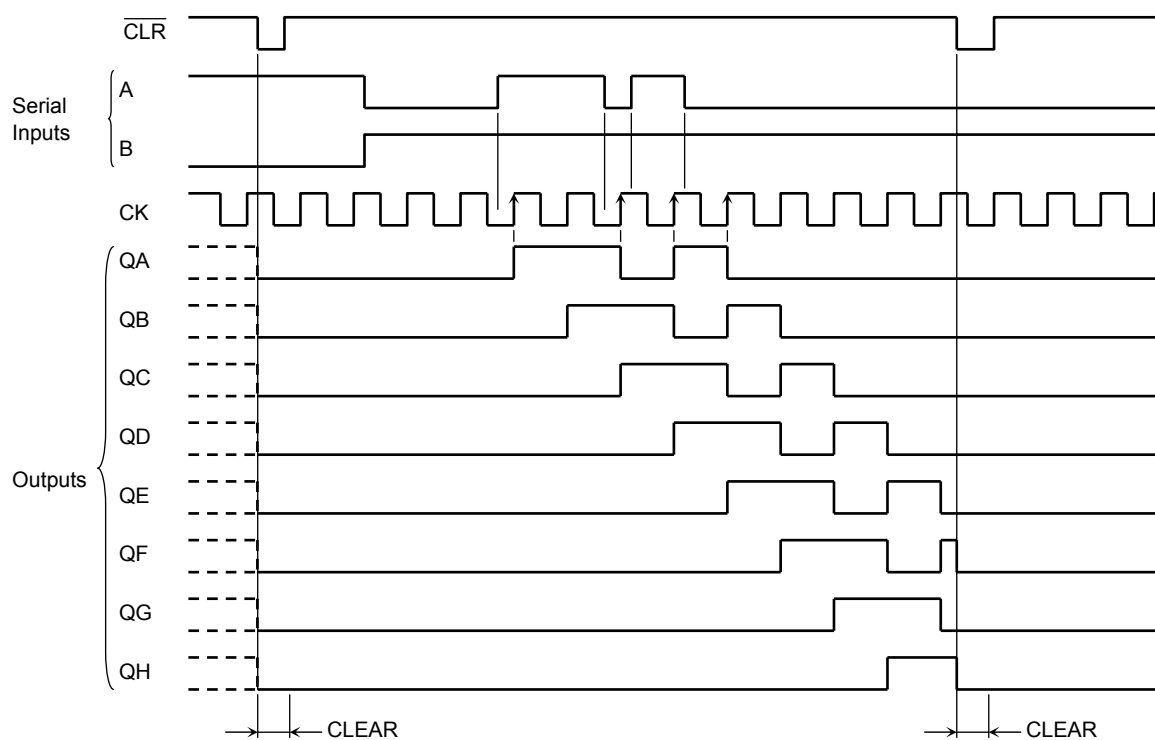
X: Don't care

QA_n to QG_n: The level of QA to QG, respectively, before the most recent positive edge of the clock.

System Diagram



Timing Chart



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to 85°C		Unit	
				Min	Typ.	Max	Min	Max		
High-level input voltage	V_{IH}	—	2.0 3.0 to 5.5	1.50 $V_{CC} \times 0.7$	— —	— —	1.50 $V_{CC} \times 0.7$	— —	V	
Low-level input voltage	V_{IL}	—	2.0 3.0 to 5.5	— —	— —	0.50 $V_{CC} \times 0.3$	— —	0.50 $V_{CC} \times 0.3$	V	
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			$I_{OH} = -4$ mA	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			$I_{OL} = 4$ mA	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
Input leakage current	I_{IN}	$V_{IN} = 5.5$ V or GND	0 to 5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	μA	

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V _{CC} (V)	Typ. / Limit		
Minimum pulse width (CK)	$t_w(L)$	—	3.3 ± 0.3	— / 5.0	5.0	ns
	$t_w(H)$		5.0 ± 0.5	— / 5.0	5.0	
Minimum pulse width ($\overline{\text{CLR}}$)	$t_w(L)$	—	3.3 ± 0.3 / 5.0 ± 0.5	— / 5.0	5.0 / 5.0	ns
Minimum set-up time	t_s	—	3.3 ± 0.3	— / 5.0	6.0	ns
			5.0 ± 0.5	— / 4.5	4.5	
Minimum hold time	t_h	—	3.3 ± 0.3	— / 0.0	0.0	ns
			5.0 ± 0.5	— / 1.0	1.0	
Minimum removal time ($\overline{\text{CLR}}$)	t_{rem}	—	3.3 ± 0.3	— / 2.5	2.5	ns
			5.0 ± 0.5	— / 2.5	2.5	

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	C _L (pF)	Min / Typ. / Max	Min / Max		
Propagation delay time (CK-Q)	t_{pLH}	—	3.3 ± 0.3	15	— / 8.4 / 12.8	1.0	15.0	ns
				50	— / 10.9 / 16.3	1.0	18.5	
	5.0 ± 0.5		15	— / 5.8 / 9.0	1.0	10.5		
			50	— / 7.3 / 11.0	1.0	12.5		
Propagation delay time ($\overline{\text{CLR}}-Q$)	t_{pHL}	—	3.3 ± 0.3	15	— / 8.3 / 12.8	1.0	15.0	ns
				50	— / 10.8 / 16.3	1.0	18.5	
			5.0 ± 0.5	15	— / 5.2 / 8.6	1.0	10.0	
				50	— / 6.7 / 10.6	1.0	12.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	80 / 125	—	65	MHz
				50	50 / 75	—	45	
			5.0 ± 0.5	15	125 / 175	—	105	
				50	85 / 115	—	75	
Input capacitance	C _{IN}	—	—	4 / 10	—	10	pF	
Power dissipation capacitance	C _{PD}	(Note)	—	76	—	—	—	pF

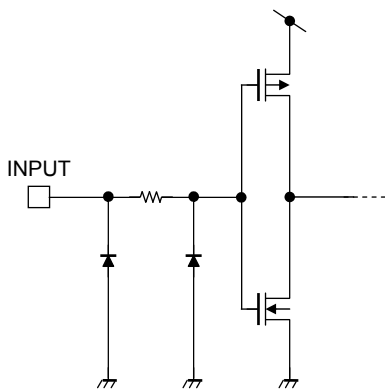
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

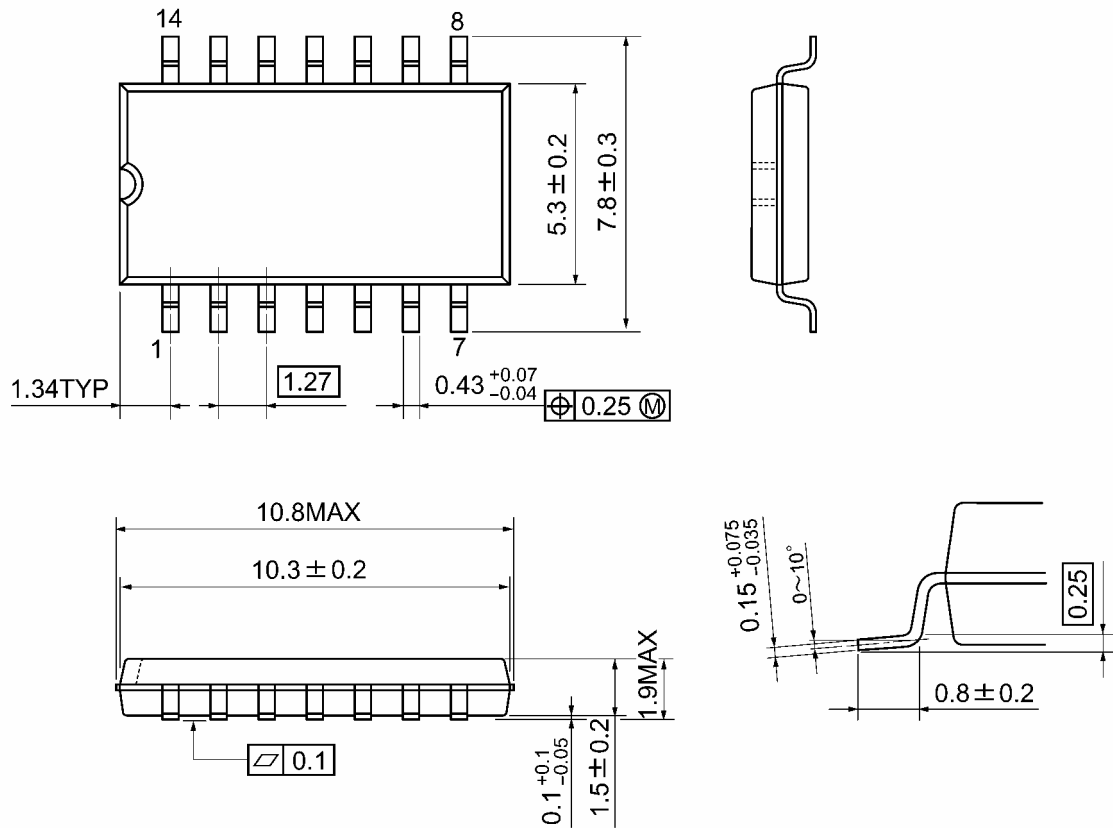
Characteristics	Symbol	Test Condition	Ta = 25°C		Unit
			V _{CC} (V)	Typ. / Max	
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.5 / 0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.5 / -0.8	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	— / 3.5	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	— / 1.5	V

Input Equivalent Circuit

Package Dimensions

SOP14-P-300-1.27A

Unit: mm

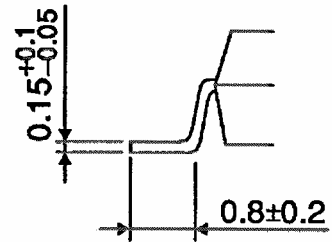
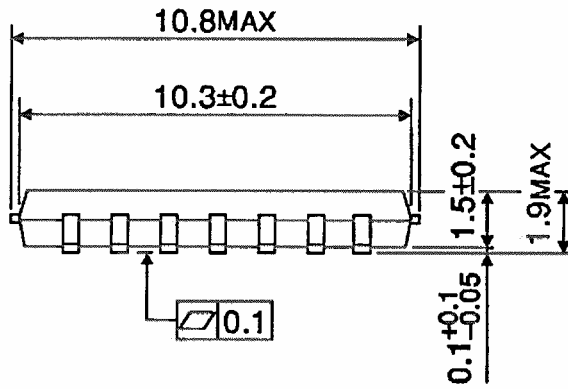
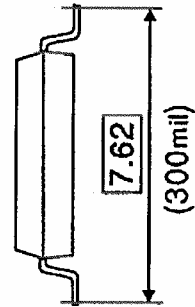
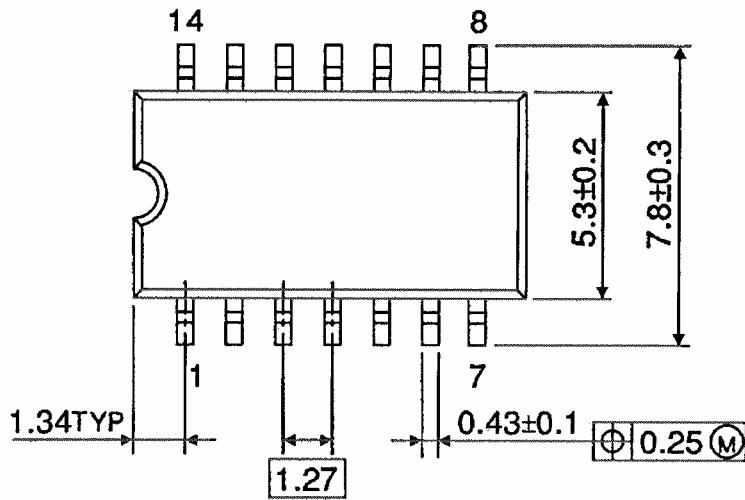


Weight: 0.18 g (typ.)

Package Dimensions

SOP14-P-300-1.27

Unit : mm

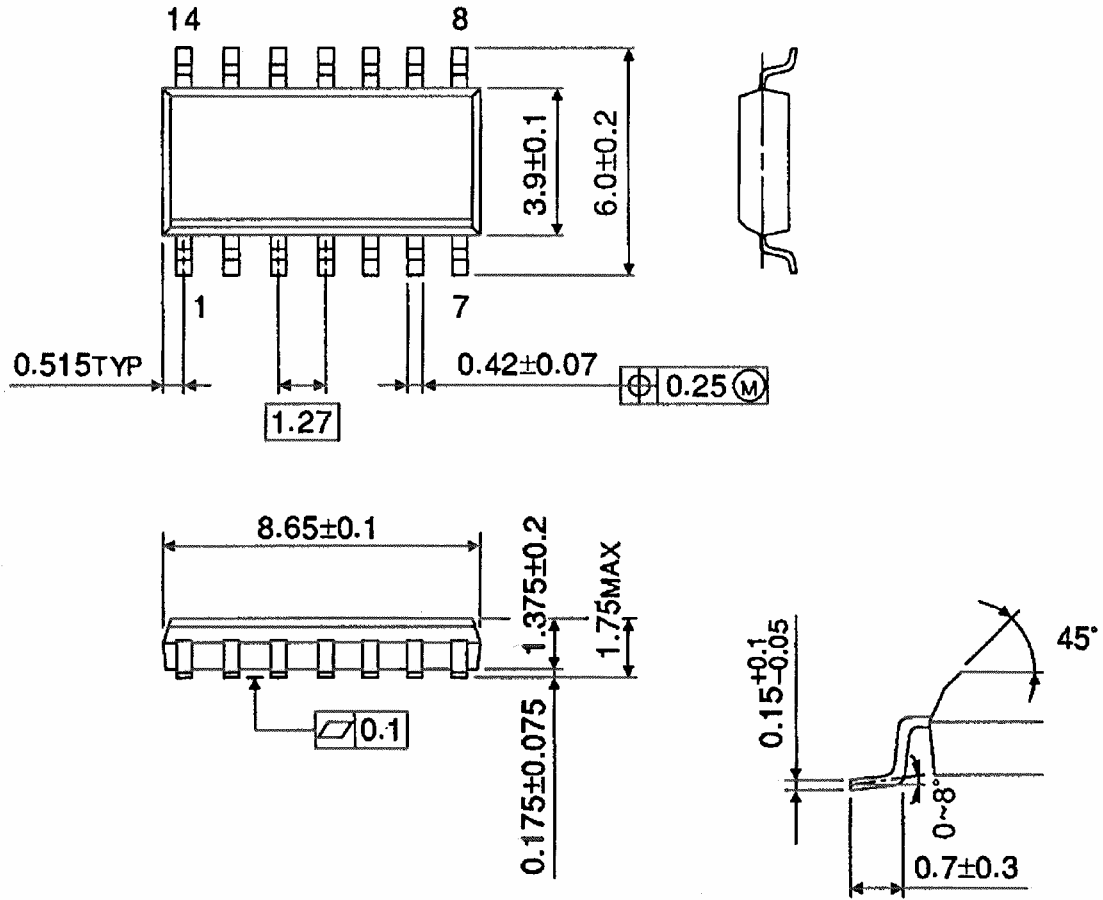


Weight: 0.18 g (typ.)

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



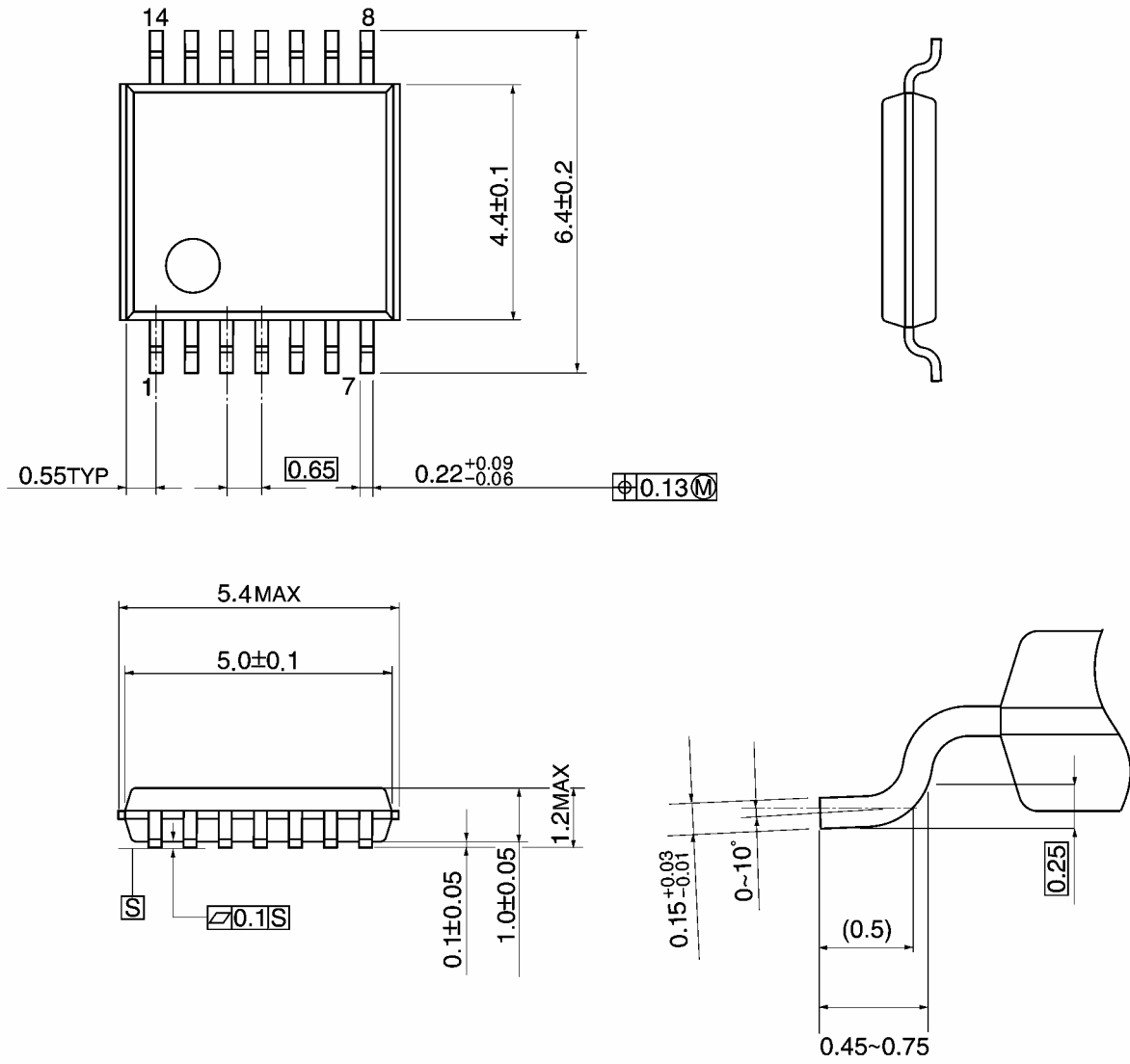
Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm

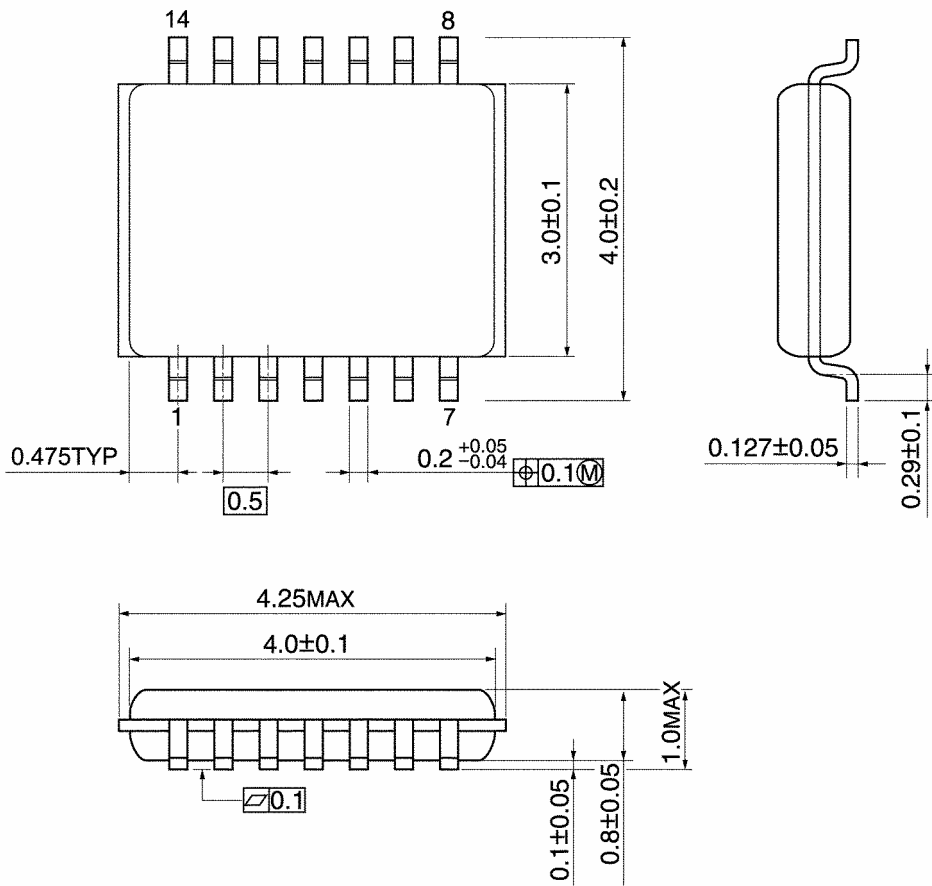


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

Note: Lead (Pb)-Free Packages**SOP14-P-300-1.27A SOL14-P-150-1.27 TSSOP14-P-0044-0.65A VSSOP14-P-0030-0.50****RESTRICTIONS ON PRODUCT USE**

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