



CY74FCT821T
CY74FCT823T
CY74FCT825T

8-/9-/10-Bit Bus Interface Registers

Features

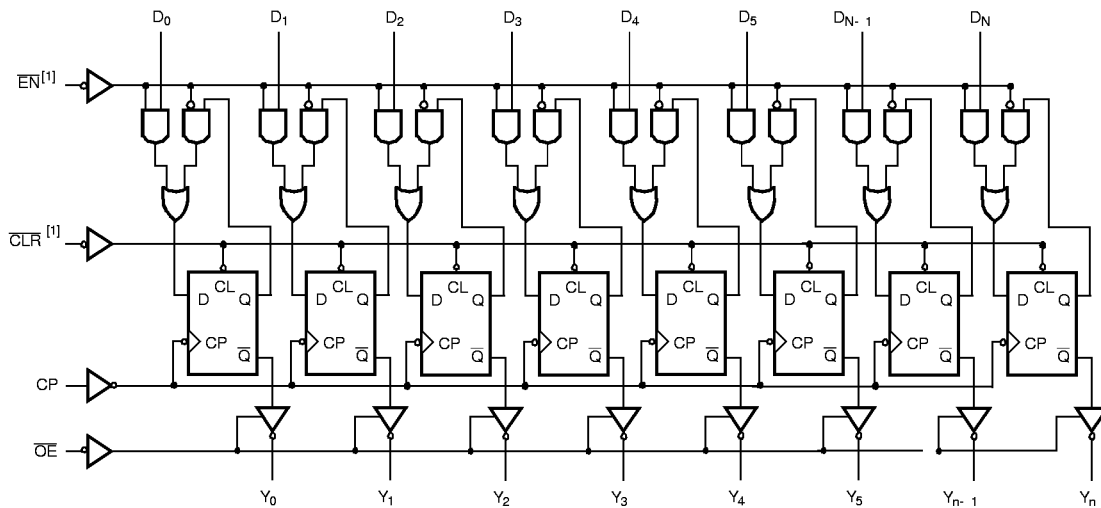
- Function, pinout and drive compatible with FCT, F, and Am29821/23/25 logic
- FCT-C speed at 6.0 ns max.
FCT-B speed at 7.5 ns max.
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V
- Sink current 64 mA
Source current 32 mA
- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Buffered common clock enable (EN) and asynchronous clear input (CLR)
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$

Functional Description

These bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT821T is a buffered, 10-bit wide version of the popular FCT374 function. The FCT823T is a 9-bit wide buffered register with clock enable (EN) and clear (CLR) ideal for parity bus interfacing in high-performance microprogrammed systems. The FCT825T is an 8-bit buffered register with all the FCT823T controls plus multiple enables ($\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$) to allow multiuser control of the interface, e.g., CS, DMA, and RD/WR. They are ideal for use as an output port requiring high I_{OL}/I_{OH} .

These devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state and are designed with a power-off disable feature to allow for live insertion of boards.

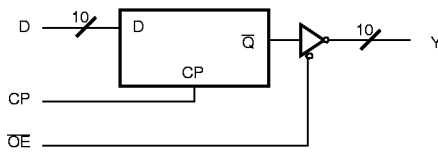
Logic Block Diagram



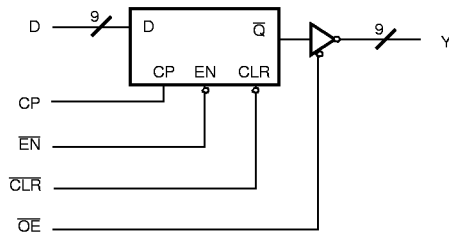
Note:
 1. Not on FCT821.

Logic Diagrams

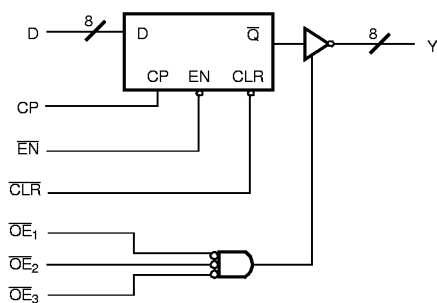
FCT821T (10-Bit Register)



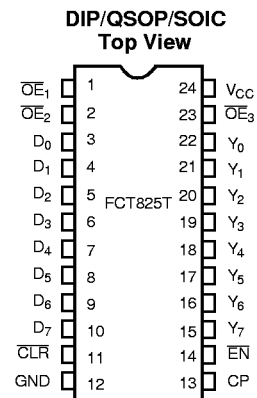
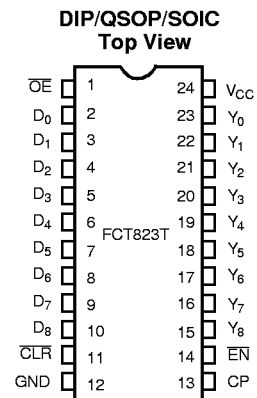
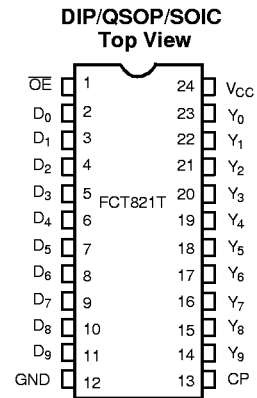
FCT823T (9-Bit Register)



FCT825T (8-Bit Register)



Pin Configurations





Pin Description

Name	I/O	Description
D	I	The D flip-flop data inputs.
$\overline{\text{CLR}}$	I	When $\overline{\text{CLR}}$ is LOW and $\overline{\text{OE}}$ is LOW, the Q outputs are LOW. When $\overline{\text{CLR}}$ is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y	O	The register three-state outputs.
EN	I	Clock Enable. When $\overline{\text{EN}}$ is LOW, data on the D input is transferred to the Q output on the LOW-to-HIGH clock transition. When $\overline{\text{EN}}$ is HIGH, the Q outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output Control. When $\overline{\text{OE}}$ is HIGH, the Y outputs are in the high-impedance state. When $\overline{\text{OE}}$ is LOW, the TRUE register data is present at the Y outputs.

Function Table^[2]

Inputs					Internal Outputs		Function
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	EN	D	CP	Q	Y	
H	H	L	L	J	L	Z	High Z
H	H	L	H	J	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	J	L	Z	Load
H	H	L	H	J	H	Z	
L	H	L	L	J	L	L	
L	H	L	H	J	H	H	

Maximum Ratings^[3,4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W
Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	All	-40°C to +85°C	5V ± 5%

Notes:

- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, J = LOW-to-HIGH Transition, Z = HIGH Impedance.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -32 mA	2.0			V
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -15 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 64 mA		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Hysteresis ^[6]	All inputs		0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			5	μA
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = 2.7V			±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = 0.5V			±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V			10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} = Max., V _{OUT} = 0.0V	-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} = 0V, V _{OUT} = 4.5V			±1	μA

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Notes:

- Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.



Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC}=\text{Max.}, V_{IN}\leq 0.2V, V_{IN}\geq V_{CC}-0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}, V_{IN}=3.4V$, ^[8] $f_1=0$, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[9]	$V_{CC}=\text{Max.}$, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}=\overline{EN}=\text{GND}$, $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current ^[10]	$V_{CC}=\text{Max.}$, $f_0=10$ MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5$ MHz, $\overline{OE}=\overline{EN}=\text{GND}$, $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	0.7	1.4	mA
		$V_{CC}=\text{Max.}$, $f_0=10$ MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at $f_1=5$ MHz, $\overline{OE}=\overline{EN}=\text{GND}$, $V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	1.2	3.4	mA
		$V_{CC}=\text{Max.}$, $f_0=10$ MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=2.5$ MHz, $\overline{OE}=\overline{EN}=\text{GND}$, $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$	1.6	3.2 ^[11]	mA
		$V_{CC}=\text{Max.}$, $f_0=10$ MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at $f_1=2.5$ MHz, $\overline{OE}=\overline{EN}=\text{GND}$, $V_{IN}=3.4V$ or $V_{IN}=\text{GND}$	3.9	12.2 ^[11]	mA

Notes:

8. Per TTL driven input ($V_{IN}=3.4V$); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN}=3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



Switching Characteristics Over the Operating Range^[12]

Param.	Description	Test Load	CY74FCT821AT CY74FCT823AT CY74FCT825AT		CY74FCT821BT CY74FCT823BT CY74FCT825BT		CY74FCT821CT CY74FCT823CT CY74FCT825CT		Unit	Fig. No. ^[13]
			Commercial		Commercial		Commercial			
			Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay CP to Y, (\overline{OE} =LOW)	C _L =50 pF R _L =500Ω		10.0		7.5		6.0	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay CP to Y, (\overline{OE} =LOW) ^[6]	C _L =300 pF R _L =500Ω		20.0		15.0		12.5	ns	1, 5
t _{PLH}	Propagation Delay \overline{CLR} to Y	C _L =50 pF R _L =500Ω		14.0		9.0		8.0	ns	1, 5
t _{PZH} t _{PZL}	Output Enable Time \overline{OE} to Y	C _L =50 pF R _L =500Ω		12.0		8.0		7.0	ns	1, 7, 8
t _{PZH} t _{PZL}	Output Enable Time \overline{OE} to Y ^[6]	C _L =300 pF R _L =500Ω		23.0		15.0		12.5	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time \overline{OE} to Y ^[6]	C _L =5 pF R _L =500Ω		7.0		6.5		6.0	ns	1, 7, 8
t _{PHZ} t _{PHL}	Output Disable Time \overline{OE} to Y	C _L =50 pF R _L =500Ω		8.0		7.5		6.5	ns	1, 7, 8
t _{SU}	Data to CP, Set-Up Time	C _L =50 pF R _L =500Ω	4.0		3.0		3.0		ns	4
t _H	Data to CP, Hold Time		2.0		1.5		1.5		ns	4
t _{SU}	Enable \overline{EN} to CP, Set-Up Time		4.0		3.0		3.0		ns	4
t _H	Enable \overline{EN} to CP, Hold Time		2.0		0.0		0.0		ns	4
t _{REM}	Clear Recovery Time, \overline{CLR} to CP		6.0		6.0		6.0		ns	6
t _W	Clock Pulse Width		7.0		6.0		6.0		ns	5
t _W	\overline{CLR} Pulse Width LOW		6.0		6.0		6.0		ns	5

Notes:

- 12. Minimum limits are guaranteed but not tested on Propagation Delays.
- 13. See "Parameter Measurement Information."



Ordering Information—FCT821T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY74FCT821CTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT821CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY74FCT821BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821BTSOC	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY74FCT821ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT821ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT821ATSOC	S13	24-Lead (300-Mil) Molded SOIC	

Ordering Information—FCT823T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY74FCT823CTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT823CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
7.5	CY74FCT823BTPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
10.0	CY74FCT823ATPC	P13/13A	24-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT823ATQC	Q13	24-Lead (150-Mil) QSOP	
	CY74FCT823ATSOC	S13	24-Lead (300-Mil) Molded SOIC	

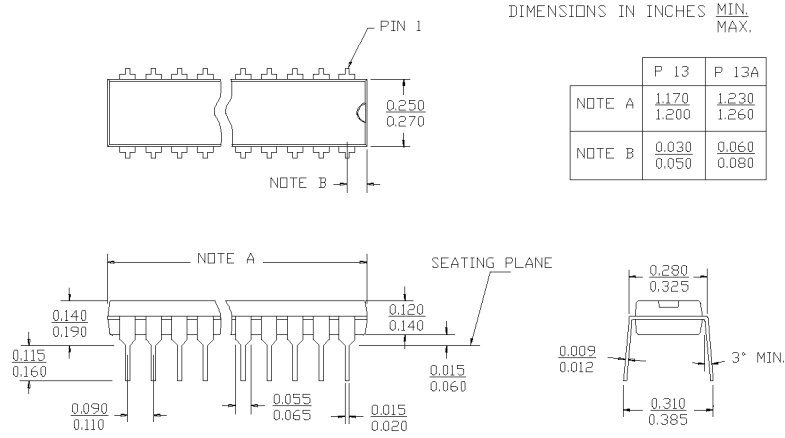
Ordering Information—FCT825T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
6.0	CY74FCT825CTQC	Q13	24-Lead (150-Mil) QSOP	Commercial
	CY74FCT825CTSOC	S13	24-Lead (300-Mil) Molded SOIC	
10.0	CY74FCT825ATSOC	S13	24-Lead (300-Mil) Molded SOIC	Commercial

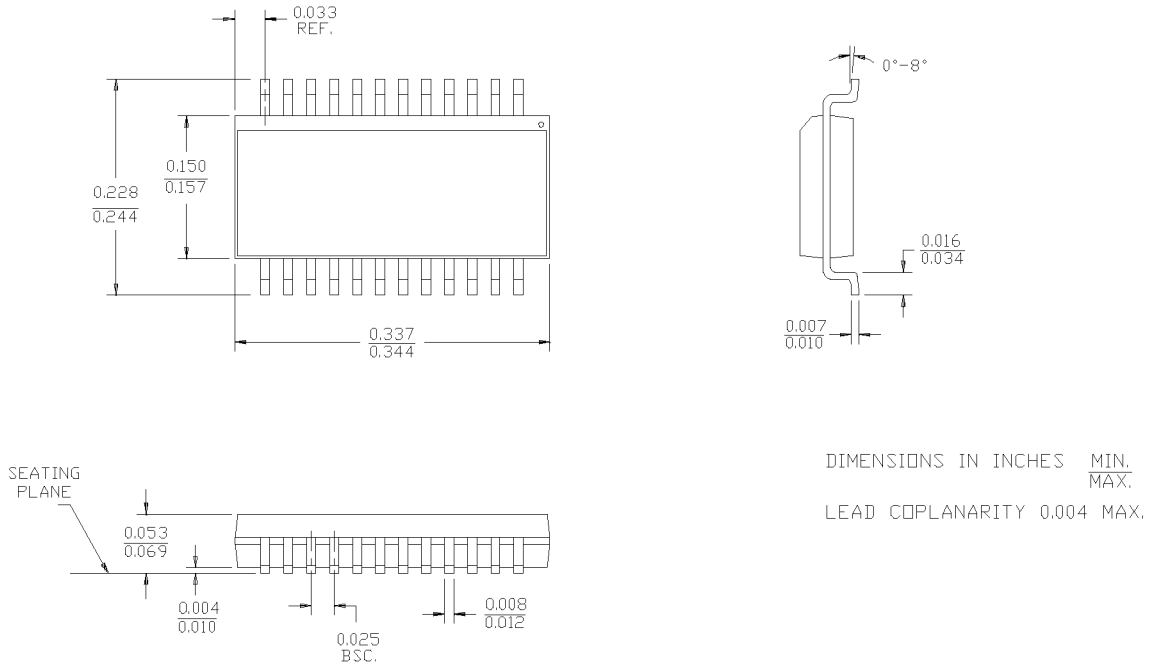
Document #: 38-00282-B

Package Diagrams

24-Lead (300-Mil) Molded DIP P13/P13A



24-Lead Quarter Size Outline Q13





Package Diagrams (continued)

24-Lead (300-Mil) Molded SOIC S13

