

## DM74S299 3-STATE 8-Bit Universal Shift/Storage Registers

### General Description

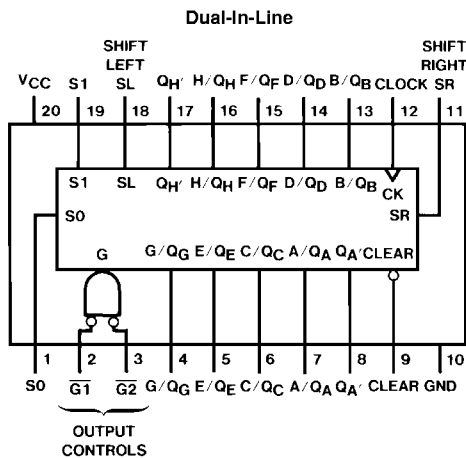
This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the 3-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

### Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
  - Hold (Store)    Shift Left
  - Shift Right    Load Data
- 3-STATE outputs drive bus lines directly
- Can be cascaded for N-bit word lengths
- Operates with outputs enabled or at high Z
- Guaranteed shift (clock) frequency 50 MHz
- Typical power dissipation 700 mW

### Connection Diagram



DS006485-1

Order Number DM74S299N  
See Package Number N20A

## Absolute Maximum Ratings (Note 1)

Supply Voltage  
Input Voltage

7V  
5.5V

Operating Free Air Temperature Range

DM74S  
Storage Temperature Range

0°C to +70°C  
-65°C to +150°C

## Recommended Operating Conditions

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	DM74S299			Units
		Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8	V
I <sub>OH</sub>	High Level Output Current (Q <sub>A</sub> thru Q <sub>H</sub> )			-6.5	mA
	High Level Output Current (Q <sub>A'</sub> , Q <sub>H'</sub> )			-0.5	
I <sub>OL</sub>	Low Level Output Current (Q <sub>A</sub> thru Q <sub>H</sub> )			20	mA
	High Level Output Current (Q <sub>A'</sub> , Q <sub>H'</sub> )			6	
f <sub>CLK</sub>	Clock Frequency (Note 3)	0	70	50	MHz
f <sub>CLK</sub>	Clock Frequency (Note 4)	0	60	40	MHz
t <sub>w</sub>	Pulse Width (Note 6)	Clock High	10		ns
		Clock Low	10		
		Clear Low	10		
t <sub>su</sub>	Setup Time (Notes 5, 6)	Select	15↑		ns
		Data High	7↑		
		Data Low	5↑		
t <sub>H</sub>	Hold Time (Notes 5, 6)	5↑			ns
t <sub>REL</sub>	Clear Release Time (Note 6)	10↑			ns
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

**Note 3:** C<sub>L</sub> = 15 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

**Note 4:** C<sub>L</sub> = 50 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

**Note 5:** Data includes the two serial inputs and the eight input/output data lines.

**Note 6:** T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max Q <sub>A</sub> thru Q <sub>H</sub>	2.4	3.2		V
		V <sub>IL</sub> = Max, V <sub>IH</sub> = Min Q <sub>A'</sub> , Q <sub>H'</sub>	2.7	3.4		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.5	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 2.7V			100	μA
		A thru H, S0, S1			50	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max V <sub>I</sub> = 0.5V			-2	mA
		Clock, Clear			-0.5	
		S0, S1			-0.25	
		Other				

## Electrical Characteristics (Continued)

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
$I_{OZH}$	Off-State Output Current with High Level Output Voltage Applied ( $Q_A$ thru $Q_H$ )	$V_{CC} = \text{Max}$ , $V_O = 2.4V$ $V_{IH} = \text{Min}$ , $V_{IL} = \text{Max}$			100	$\mu A$
$I_{OZL}$	Off-State Output Current with Low Level Output Voltage Applied ( $Q_A$ thru $Q_H$ )	$V_{CC} = \text{Max}$ , $V_O = 0.5V$ $V_{IH} = \text{Min}$ , $V_{IL} = \text{Max}$			-250	$\mu A$
$I_{OS}$	Short Circuit Output Current ( $Q_A$ thru $Q_H$ )	$V_{CC} = \text{Max}$ (Note 8)	-40		-100	mA
	Short Circuit Output Current ( $Q_A$ , $Q_H$ )	$V_{CC} = \text{Max}$ (Note 8)	-20		-100	
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$		140	225	mA

Note 7: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ .

Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics

at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$ (Note 10)				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency	(Note 11)	50		40		MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output (Note 10)	Clock to $Q_A$ or $Q_H$		20		22	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output (Note 10)	Clock to $Q_A$ or $Q_H$		20		23	ns
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to $Q_A$ thru $Q_H$				21	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to $Q_A$ thru $Q_H$				21	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output (Note 10)	Clear to $Q_A$ or $Q_H$		21		24	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clear to $Q_A$ thru $Q_H$				24	ns
$t_{PZH}$	Output Enable Time to High Level Output	$\overline{G}1, \overline{G}2$ to $Q_A$ thru $Q_H$				18	ns
$t_{PZL}$	Output Enable Time to Low Level Output	$\overline{G}1, \overline{G}2$ to $Q_A$ thru $Q_H$				18	ns
$t_{PHZ}$	Output Disable Time to High Level Output (Note 9)	$\overline{G}1, \overline{G}2$ to $Q_A$ thru $Q_H$		12			ns
$t_{PLZ}$	Output Disable Time to Low Level Output (Note 9)	$\overline{G}1, \overline{G}2$ to $Q_A$ thru $Q_H$		12			ns

Note 9:  $C_L = 5\text{ pF}$ .

Note 10:  $R_L = 1K\Omega$  for delays measured to  $Q_A$  and  $Q_H$ .

Note 11: For testing  $f_{MAX}$  all outputs are loaded simultaneously.

## Function Table

Mode	Inputs						Inputs/Outputs								Outputs			
	Clear	Function Select		Output Control		Clock	Serial		A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A</sub> '	Q <sub>H</sub> '
		S1	S0	$\overline{G1}^\dagger$	$\overline{G2}^\dagger$		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
	H	X	X	L	L	L	X	X	Q <sub>A0</sub>	Q <sub>B0</sub>	Q <sub>C0</sub>	Q <sub>D0</sub>	Q <sub>E0</sub>	Q <sub>F0</sub>	Q <sub>G0</sub>	Q <sub>H0</sub>	Q <sub>A0</sub>	Q <sub>H0</sub>
Shift Right	H	L	H	L	L	↑	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
	H	L	H	L	L	↑	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	↑	H	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	H	Q <sub>Bn</sub>	H
	H	H	L	L	L	↑	L	X	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	Q <sub>Hn</sub>	L	Q <sub>Bn</sub>	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected

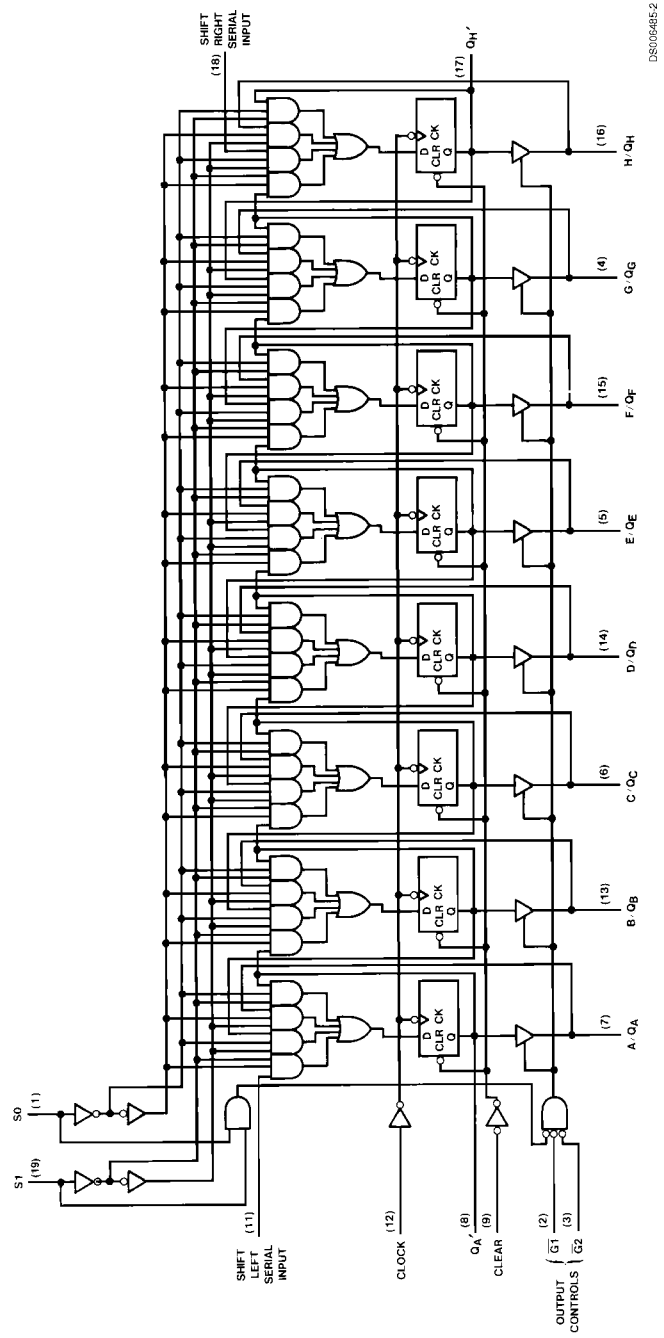
a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

Q<sub>A0</sub>...Q<sub>H0</sub> = The output logic level of Q<sub>x</sub> before the indicated input conditions were established.

H = high level, L = low logic level, X = either low or high logic level

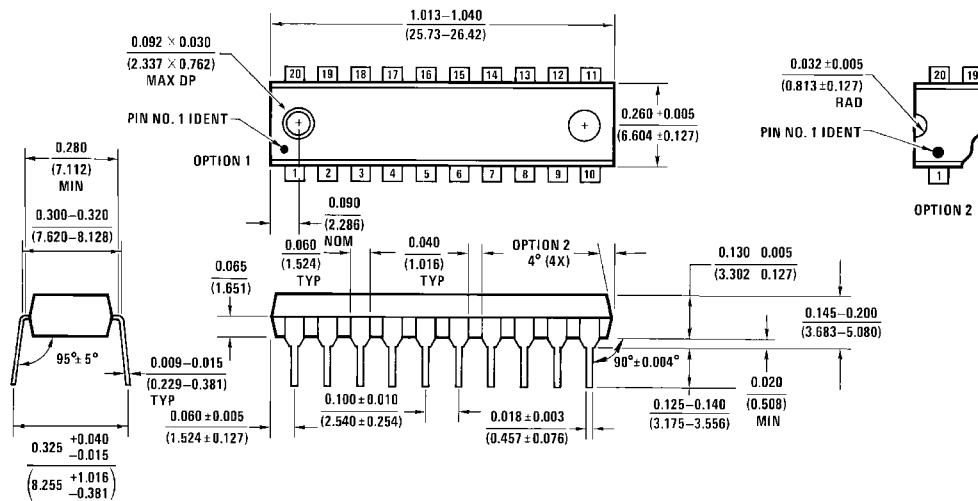
Q<sub>An</sub>...Q<sub>Hn</sub> = The output logic level before the active transition (↑) of the clock input.

# Logic Diagram



DS006485-2

**Physical Dimensions** inches (millimeters) unless otherwise noted



N20A (REV G)

**20-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74S299N**  
**Package Number N20A**

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation  
 Americas  
 Customer Response Center  
 Tel: 1-888-522-5372

Fairchild Semiconductor Europe  
 Fax: +49 (0) 1 80-530 85 86  
 Email: europe.support@nsc.com  
 Deutsch Tel: +49 (0) 8 141-35-0  
 English Tel: +44 (0) 1 793-85-68-56  
 Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.  
 13th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: +852 2737-7200  
 Fax: +852 2314-0061

National Semiconductor Japan Ltd.  
 Tel: 81-3-5620-6175  
 Fax: 81-3-5620-6179

www.fairchildsemi.com