

## 74F194 4-Bit Bidirectional Universal Shift Register

### General Description

The 74F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 74F194 is similar in operation to the 74F195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

### Features

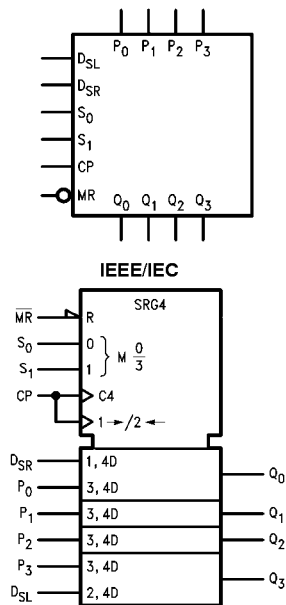
- Typical shift frequency of 150 MHz
- Asynchronous master reset
- Hold (do nothing) mode
- Fully synchronous serial or parallel data transfers

### Ordering Code:

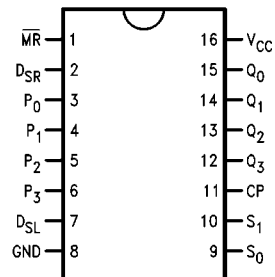
Order Number	Package Number	Package Description
74F194SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F194SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F194PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I <sub>IH</sub> /I <sub>IL</sub> Output I <sub>OH</sub> /I <sub>OL</sub>
S <sub>0</sub> , S <sub>1</sub>	Mode Control Inputs	1.0/1.0	20 μA/-0.6 mA
P <sub>0</sub> -P <sub>3</sub>	Parallel Data Inputs	1.0/1.0	20 μA/-0.6 mA
D <sub>SR</sub>	Serial Data Input (Shift Right)	1.0/1.0	20 μA/-0.6 mA
D <sub>SL</sub>	Serial Data Input (Shift Left)	1.0/1.0	20 μA/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA
$\overline{\text{MR}}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
Q <sub>0</sub> -Q <sub>3</sub>	Parallel Outputs	50/33.3	-1 mA/20 mA

### Functional Description

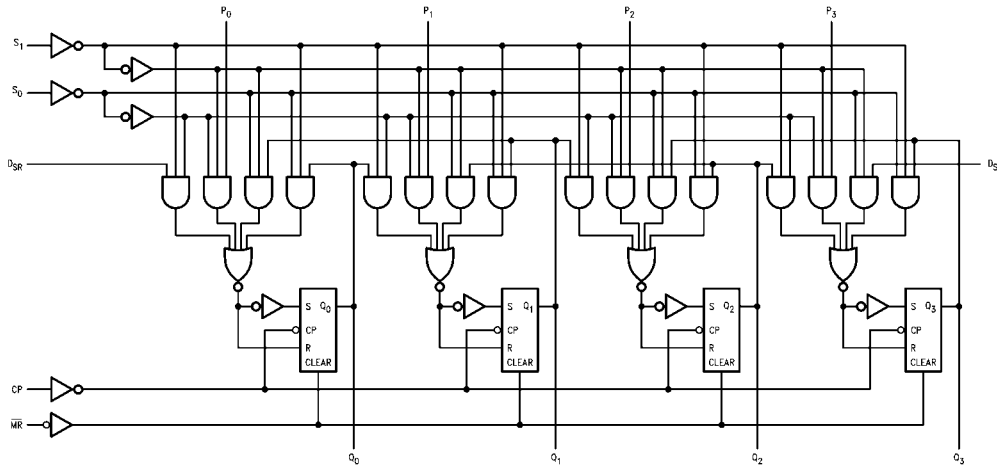
The 74F194 contains four edge-triggered D-type flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S<sub>0</sub>, S<sub>1</sub>) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P<sub>0</sub>-P<sub>3</sub>) and Serial data (D<sub>SR</sub>, D<sub>SL</sub>) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ( $\overline{\text{MR}}$ ) overrides all other inputs and forces the outputs LOW.

### Mode Select Table

Operating Mode	Inputs						Outputs			
	$\overline{\text{MR}}$	S <sub>1</sub>	S <sub>0</sub>	D <sub>SR</sub>	D <sub>SL</sub>	P <sub>n</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>
Shift Left	H	h	l	X	l	X	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	L
	H	h	l	X	h	X	q <sub>1</sub>	q <sub>2</sub>	q <sub>3</sub>	H
Shift Right	H	l	h	l	X	X	L	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
	H	l	h	h	X	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>
Parallel Load	H	h	h	X	X	p <sub>n</sub>	p <sub>0</sub>	p <sub>1</sub>	p <sub>2</sub>	p <sub>3</sub>

H (h) = HIGH Voltage Level  
 L (l) = LOW Voltage Level  
 p<sub>n</sub> (q<sub>n</sub>) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.  
 X = Immaterial

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEx</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		33	46	mA	Max	

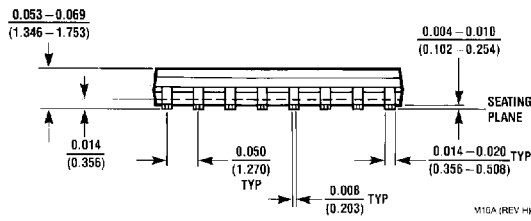
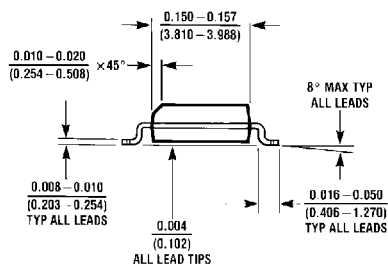
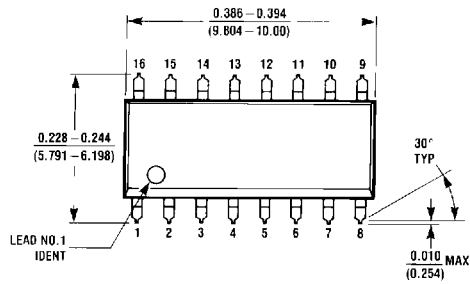
### AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>MAX</sub>	Maximum Shift Frequency	105	150		90		90		MHz
t <sub>PLH</sub>	Propagation Delay	3.5	5.2	7.0	3.0	8.5	3.5	8.0	ns
t <sub>PHL</sub>	CP to Q <sub>n</sub>	3.5	5.5	7.0	3.0	8.5	3.5	8.0	
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns

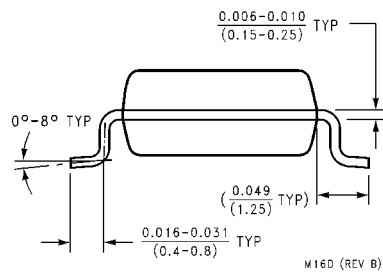
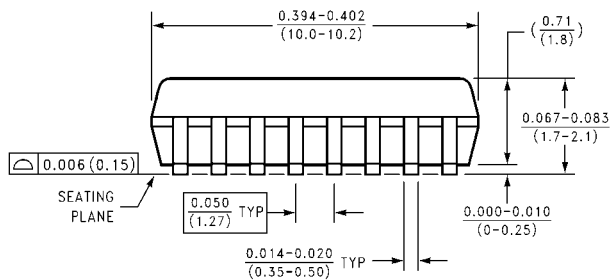
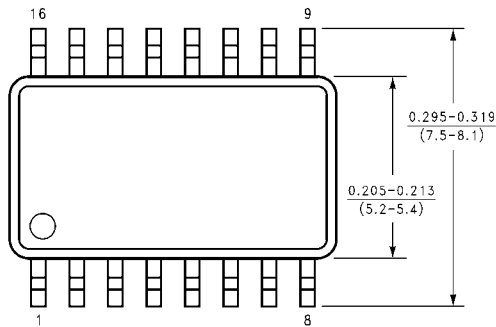
### AC Operating Requirements

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	4.0		6.0		4.0		ns
t <sub>S</sub> (L)	P <sub>n</sub> or D <sub>SR</sub> or D <sub>SL</sub> to CP	4.0		4.0		4.0		
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	1.0		1.5		1.0		
t <sub>H</sub> (L)	P <sub>n</sub> or D <sub>SR</sub> or D <sub>SL</sub> to CP	0		1.0		1.0		ns
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	10.0		10.5		11.0		
t <sub>S</sub> (L)	S <sub>n</sub> to CP	8.0		8.0		8.0		
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0		0		0		ns
t <sub>H</sub> (L)	S <sub>n</sub> to CP	0		0		0		
t <sub>W</sub> (H)	CP Pulse Width, HIGH	5.0		5.5		5.5		ns
t <sub>W</sub> (L)	MR Pulse Width, LOW	5.0		5.0		5.0		ns
t <sub>REC</sub>	Recovery Time MR to CP	9.0		9.0		11.0		ns

**Physical Dimensions** inches (millimeters) unless otherwise noted

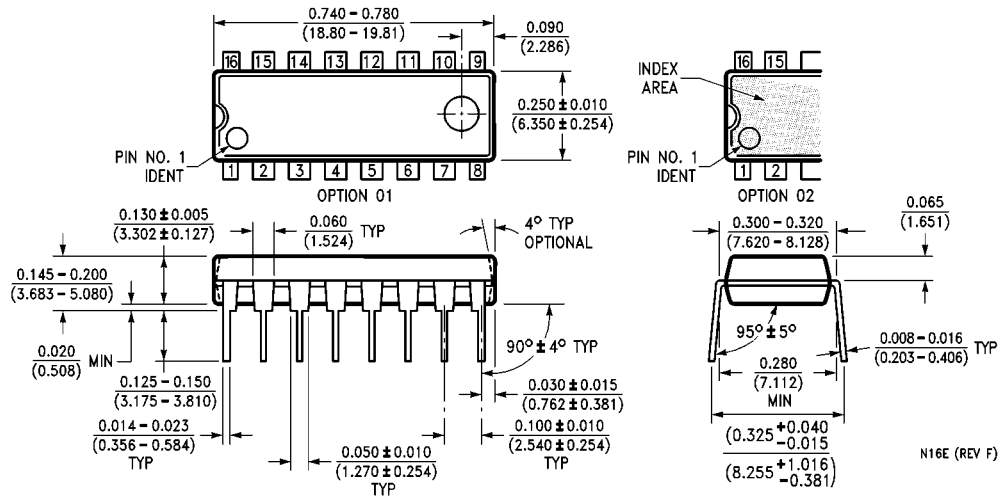


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E**

N16E (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)