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National Semiconductor

54LS299/DM74LS299
8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

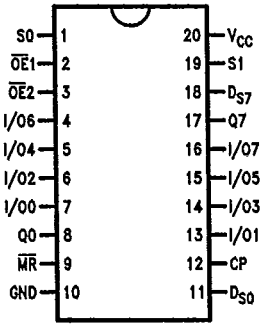
The 'LS299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, load and store
- Separate shift right serial input and shift left serial input for easy cascading
- TRI-STATE outputs for bus oriented applications

Connection Diagram

Dual-In-Line Package



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Order Number 54LS299DMQB, 54LS299FMQB, 54LS299LMQB, DM74LS299WM or DM74LS299N
See NS Package Number E20A, J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D_{S0}	Serial Data Input for Right Shift
D_{S7}	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}1$, $\overline{OE}2$	TRI-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q0–Q7	Serial Outputs

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS299			DM74LS299			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW S0 or S1 to CP	24 24			24 24			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW S0 or S1 to CP	5 5			0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	15 15			10 10			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP	5 5			0 0			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	15 15			15 15			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	10			10			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.55	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	Inputs			0.1	mA
			Sn			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Sn			40	μA
			Inputs			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Sn			−0.8	mA
			Inputs			−0.4	mA

Electrical Characteristics (Continued)

Over recommended operating free air temperature range (unless otherwise noted) T-46-09-05

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, $\overline{OE}$ = 4.5V				60	mA
I_{OZH}	TRI-STATE Output Off Current High	V_{CC} = V_{CCH} V_{OZH} = 2.7V				40	μA
I_{OZL}	TRI-STATE Output Off Current Low	V_{CC} = V_{CCH} V_{OZL} = 0.4V				−400	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

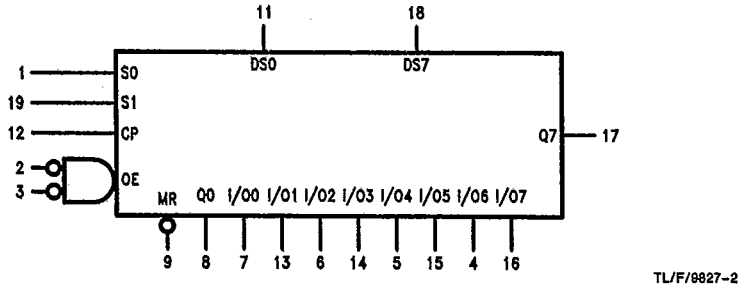
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2 kΩ C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Input Frequency	35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q0 or Q7		26 28	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 35	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q0 or Q7		28	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		35	ns
t_{PZH} t_{PZL}	Output Enable Time		18 25	ns
t_{PHZ} t_{PLZ}	Output Disable Time		15 20	ns

Logic Symbol



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V_{CC} = Pin 20
GND = Pin 10

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Functional Description

The 'LS299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S0 and S1, as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}1$ or $\overline{OE}2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{MR}$	S1	S0	CP	
L	X	X	X	Asynchronous Reset; Q0–Q7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $D_{S0} \rightarrow Q0$, $Q0 \rightarrow Q1$, etc.
H	H	L	⌐	Shift Left; $D_{S7} \rightarrow Q7$, $Q7 \rightarrow Q6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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Logic Diagram