Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

National Semiconductor

February 1988

MM54C195/MM74C195 4-Bit Registers

General Description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible:

Parallel Load

Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control of input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K, D, or T-type flip flop as shown in the truth table.

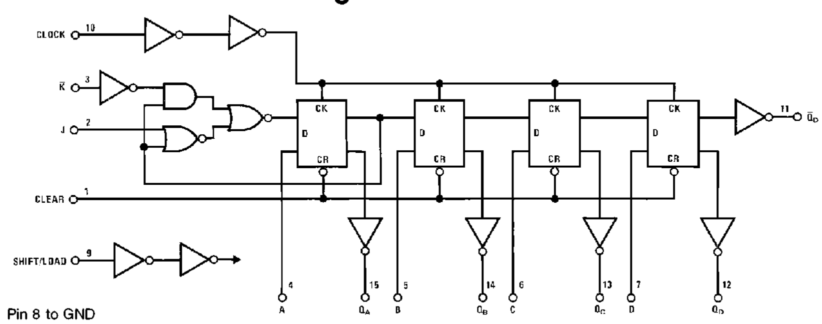
Features

- Medium speed operation — 8.5 MHz (typ.) with 10V supply and 50 pF load
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 100 nW (typ.)
- Tenth power TTL compatible — Drive 2 LPTTL loads
- Supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and K inputs to first stage
- Complementary outputs from last stage
- Positive-edge triggered clocking
- Diode clamped inputs to protect against static charge

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

Schematic and Connection Diagrams

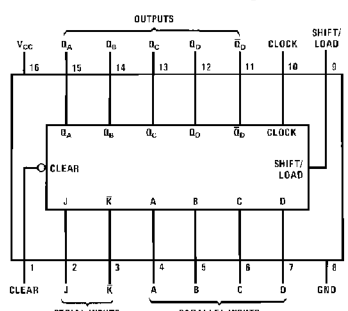


Pin 8 to GND

Pin 16 to V_{CC}

TL/F/5902–1

Dual-In-Line Package



TL/F/5902–2

Top View

Order Number MM54C195 or MM74C195

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin	$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature Range	
MM54C195	$-55°C$ to $+125°C$
MM74C195	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -360\mu A$ 74C $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = 360\mu A$ 74C $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V$, $V_{IN(1)} = 5V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		150 75	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clear to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		150 50	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$		80 35	200 70	ns ns
t_S	Time Prior to Clock Pulse that Shift/Load must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$		110 60	150 90	ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$		−10 −5.0	0 0	ns ns
t_W	Minimum Clear Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5V$ $V_{CC} = 10V$		100 50	200 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		90 40	130 60	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	5.0 2.0			μs μs
f_{MAX}	Maximum Input Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.0 5.5	3.0 8.5		MHz MHz
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Truth Table

Inputs AT t_n		Outputs AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

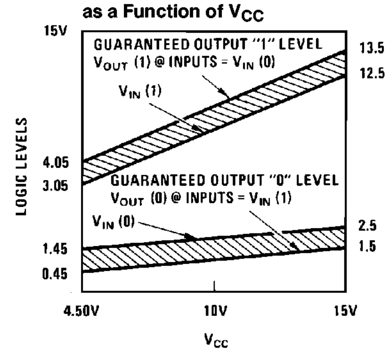
Note: H = High Level, L = Low Level

t_n = bit time before clock pulse

t_{n+1} = bit time after clock pulse

Q_{An} = State of Q_A at t_n

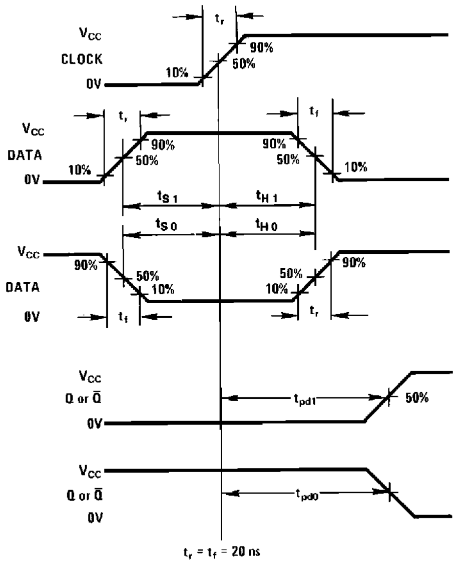
Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5902-3

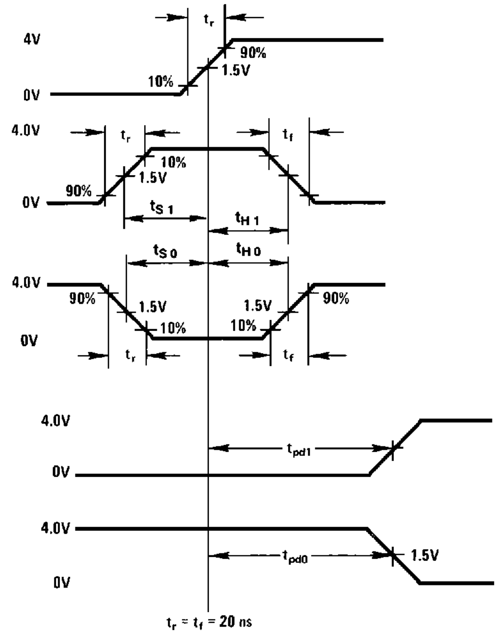
Switching Time Waveforms

CMOS to CMOS



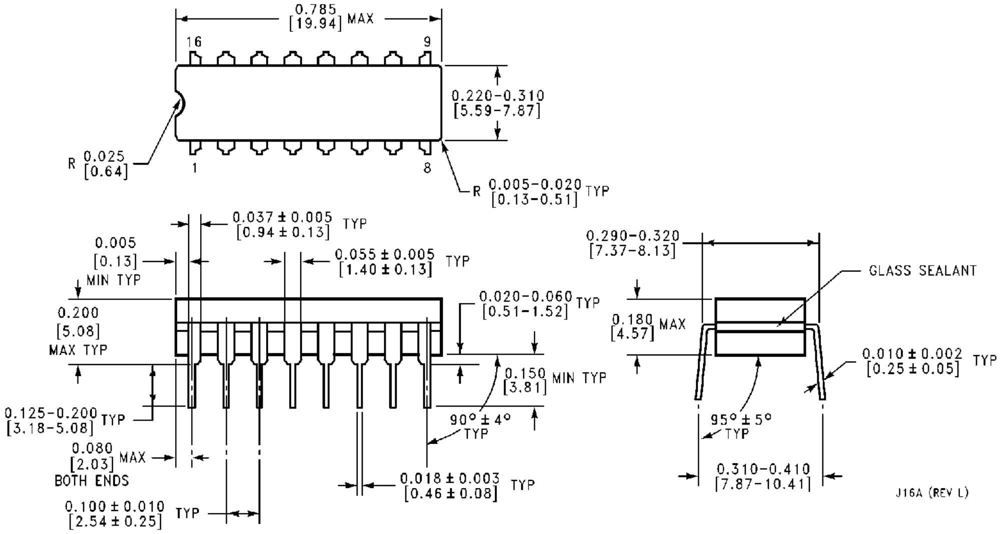
TL/F/5902–4

TTL to CMOS



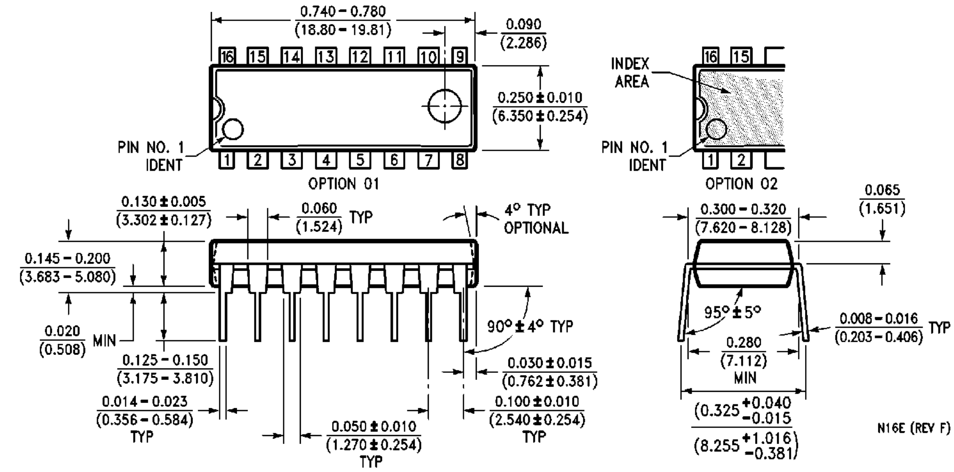
TL/F/5902–5

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C195J or MM74C195J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM54C195N or MM74C195N
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408