# SN74LV595A 8-Bit Shift Registers With 3-State Output Registers

## 1 Features

- 2-V to 5.5-V $V_{CC}$ operation
- Maximum $t_{pd}$ of 7.1 ns at 5 V
- Typical $V_{OLP}$ (output ground bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (output $V_{OH}$ undershoot) > 2.3 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Support mixed-mode voltage operation on all ports
- 8-bit serial-in, parallel-out shift
- $I_{off}$ supports live insertion, partial power-down mode, and back-drive protection
- Shift register has direct clear
- Latch-up performance exceeds 250 mA per JESD 17

## 2 Applications

- Output expansion
- LED matrix control
- 7-segment display control

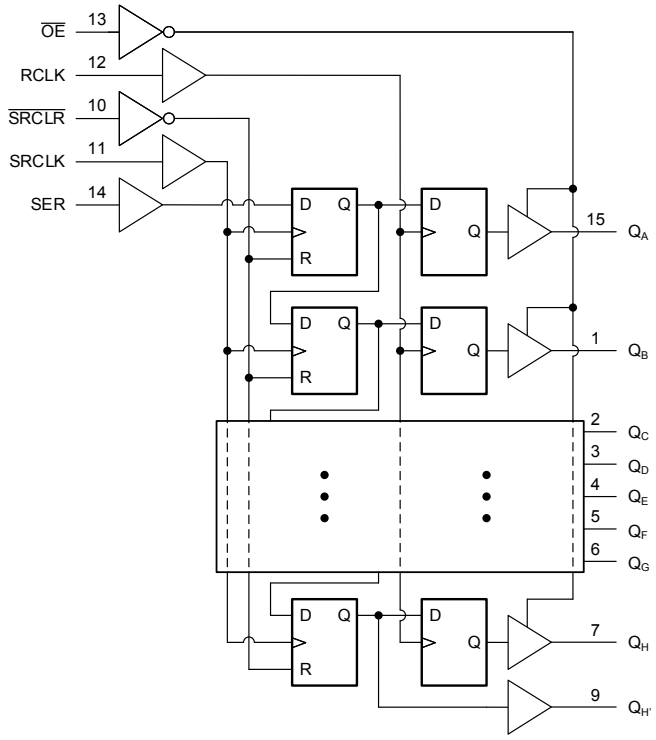
## 3 Description

The SN74LV595A device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered.

**Package Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LV595A | RGY (VQFN, 16) | 4.00 mm × 3.50 mm |
| | PW (TSSOP, 16) | 5.00 mm × 4.40 mm |
| | NS (SO ,16) | 10.20 mm × 5.30 mm |
| | D (SOIC, 16) | 9.00 mm × 3.90 mm |
| | BQB (WQFN, 16) | 3.60 mm × 2.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Logic Diagram (Positive Logic)**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision R (June 2022) to Revision S (November 2022) | Page |
|---|---|
| • Changed the status of the data sheet from: *Advanced Information* to: *Production Data* | 1 |

## 5 Pin Configuration and Functions

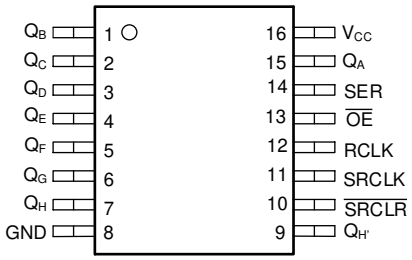



**Figure 5-1. D, DW, or PW Package, 16-Pin SOIC, SOP or TSSOP (Top View)**

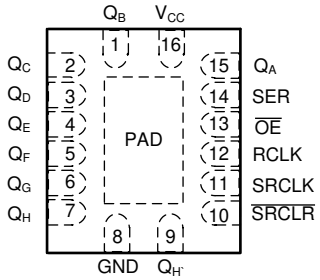



**Figure 5-2. BQB or RGY Package, 16-Pin WQFN or VQFN (Transparent Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 8 | G | Ground Pin |
| $\overline{OE}$ | 13 | I | Output Enable Pin. Active LOW |
| $Q_A$ | 15 | O | $Q_A$ Output |
| $Q_B$ | 1 | O | $Q_B$ Output |
| $Q_C$ | 2 | O | $Q_C$ Output |
| $Q_D$ | 3 | O | $Q_D$ Output |
| $Q_E$ | 4 | O | $Q_E$ Output |
| $Q_F$ | 5 | O | $Q_F$ Output |
| $Q_G$ | 6 | O | $Q_G$ Output |
| $Q_H$ | 7 | O | $Q_H$ Output |
| $Q_{H'}$ | 9 | O | $Q_{H'}$ Output |
| RCLK | 12 | I | RCLK Input |
| SER | 14 | I | SER Input |
| SRCLK | 11 | I | SRCLK Input |
| $\overline{SRCLR}$ | 10 | I | $\overline{SRCLR}$ Input |
| $V_{CC}$ | 16 | P | Power Pin |
| Thermal Pad | | — | Thermal Pad[2] |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power
(2) RGY and BQB package only

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range applied in the high or low state(2) (3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±35 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±70 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Machine Model (MM), per JEDEC specification | ±200 | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | –2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | –8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | –16 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 16 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LV595A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | D | DB | NS | PW | RGY | BQB | |
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 80.2 | 97.8 | 79.4 | 106.1 | 39.5 | 85.9 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 40.3 | 48.1 | 35.8 | 40.8 | 50.5 | 82.4 | |
| $R_{θJB}$ | Junction-to-board thermal resistance | 38.0 | 48.5 | 40.2 | 51.1 | 17.1 | 55.6 | |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 9.0 | 10.0 | 5.5 | 3.8 | 0.9 | 9.4 | |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 37.7 | 47.9 | 39.9 | 50.6 | 17.2 | 55.6 | |
| $R_{θJC(bot)}$ | Junction-to-case (bottom) thermal resistance | — | — | — | — | 5.9 | 33.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | –40°C to 85°C | | | –40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | | $I_{OH}$ = –50 µA | 2 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | | V |
| | | $I_{OH}$ = –2 mA | 2.3 V | 2 | | | 2 | | | |
| | $Q_{H'}$ | $I_{OH}$ = –6 mA | 3 V | 2.48 | | | 2.45 | | | |
| | $Q_A$ –$Q_H$ | $I_{OH}$ = –8 mA | | 2.48 | | | 2.45 | | | |
| | $Q_{H'}$ | $I_{OH}$ = –12 mA | 4.5 V | 3.8 | | | 3.7 | | | |
| | $Q_A$–$Q_H$ | $I_{OH}$ = –16 mA | | 3.8 | | | 3.7 | | | |
| $V_{OL}$ | | $I_{OL}$ = 50 µA | 2 V to 5.5 V | | | 0.1 | | | 0.1 | V |
| | | $I_{OL}$ = 2 mA | 2.3 V | | | 0.4 | | | 0.4 | |
| | $Q_{H'}$ | $I_{OL}$ = 6 mA | 3 V | | | 0.44 | | | 0.5 | |
| | $Q_A$–$Q_H$ | $I_{OL}$ = 8 mA | | | | 0.44 | | | 0.5 | |
| | $Q_{H'}$ | $I_{OL}$ = 12 mA | 4.5 V | | | 0.55 | | | 0.6 | |
| | $Q_A$–$Q_H$ | $I_{OL}$ = 16 mA | | | | 0.55 | | | 0.6 | |
| $I_I$ | $V_I$ = 5.5 V or GND | | 0 V to 5.5 V | | | ±1 | | | ±1 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND | $Q_A$ – $Q_H$ | 5.5 V | | | ±5 | | | ±5 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 5.5 V | | | 20 | | | 20 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 0 to 5.5 V | | 0 V | | | 5 | | | 5 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 3.5 | | | 3.5 | | pF |

## 6.6 Timing Requirements, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

| | | | $T_A$ = 25°C | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | SRCLK high or low | 7 | | 7.5 | | 8.5 | | ns |
| | | RCLK high or low | 7 | | 7.5 | | 8.5 | | |
| | | $\overline{SRCLR}$ low | 6 | | 6.5 | | 7.5 | | |
| $t_{su}$ | Setup time | SER before SRCLK↑ | 5.5 | | 5.5 | | 6.5 | | ns |
| | | SRCLK↑ before RCLK↑(1) | 8 | | 9 | | 10 | | |
| | | $\overline{SRCLR}$ low before RCLK↑ | 8.5 | | 9.5 | | 10.5 | | |
| | | $\overline{SRCLR}$ high (inactive) before SRCLK↑ | 4 | | 4 | | 5 | | |
| $t_h$ | Hold time | SER after SRCLK↑ | 1.5 | | 1.5 | | 2.5 | | ns |

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

## 6.7 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

| | | | $T_A$ = 25°C | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | SRCLK high or low | 5.5 | | 5.5 | | 6.5 | | ns |
| | | RCLK high or low | 5.5 | | 5.5 | | 6.5 | | |
| | | $\overline{SRCLR}$ low | 5 | | 5 | | 6 | | |
| $t_{su}$ | Setup time | SER before SRCLK↑ | 3.5 | | 3.5 | | 4.5 | | ns |
| | | SRCLK↑ before RCLK↑(1) | 8 | | 8.5 | | 9.5 | | |
| | | $\overline{SRCLR}$ low before RCLK↑ | 8 | | 9 | | 10 | | |
| | | $\overline{SRCLR}$ high (inactive) before SRCLK↑ | 3 | | 3 | | 4 | | |
| $t_h$ | Hold time | SER after SRCLK↑ | 1.5 | | 1.5 | | 2.5 | | ns |

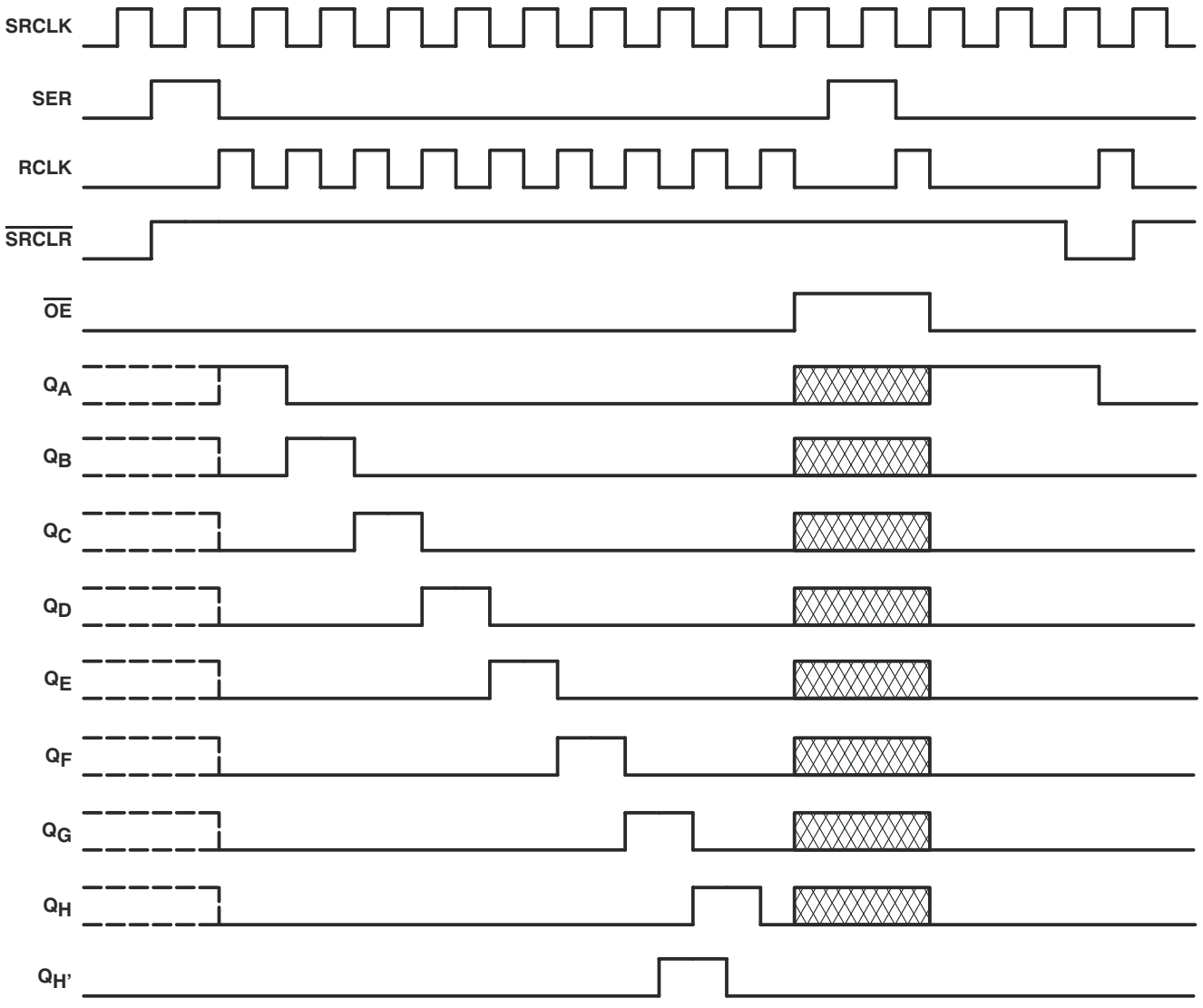
(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

## 6.8 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

| | | | $T_A$ = 25°C | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | SRCLK high or low | 5 | | 5 | | 6 | | ns |
| | | RCLK high or low | 5 | | 5 | | 6 | | |
| | | $\overline{SRCLR}$ low | 5.2 | | 5.2 | | 6.2 | | |
| $t_{su}$ | Setup time | SER before SRCLK↑ | 3 | | 3 | | 4 | | ns |
| | | SRCLK↑ before RCLK↑(1) | 5 | | 5 | | 6 | | |
| | | $\overline{SRCLR}$ low before RCLK↑ | 5 | | 5 | | 6 | | |
| | | $\overline{SRCLR}$ high (inactive) before SRCLK↑ | 2.5 | | 2.5 | | 3.5 | | |
| $t_h$ | Hold time | SER after SRCLK↑ | 2 | | 2 | | 3 | | ns |

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.




NOTE: ▨ implies that the output is in 3-State mode.

**Figure 6-1. Timing Diagram**

## 6.9 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 65 | 80 | | 45 | | 45 | | MHz |
| | | | $C_L$ = 50 pF | 60 | 70 | | 40 | | 40 | | |
| $t_{PLH}$ | RCLK | $Q_A$– $Q_H$ | $C_L$ = 15 pF | | 8.4 | 14.2 | 1 | 15.8 | 1 | 16.8 | ns |
| $t_{PHL}$ | | | | | 8.4 | 14.2 | 1 | 15.8 | 1 | 16.8 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | | | 9.4 | 19.6 | 1 | 22.2 | 1 | 23.2 | |
| $t_{PHL}$ | | | | | 9.4 | 19.6 | 1 | 22.2 | 1 | 23.2 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | | | 8.7 | 14.6 | 1 | 16.3 | 1 | 17.3 | |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 8.2 | 13.9 | 1 | 15 | 1 | 16 | |
| $t_{PZL}$ | | | | | 10.9 | 18.1 | 1 | 20.3 | 1 | 21.3 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 8.3 | 13.7 | 1 | 15.6 | 1 | 16.6 | |
| $t_{PLZ}$ | | | | | 9.2 | 15.2 | 1 | 16.7 | 1 | 17.7 | |
| $t_{PLH}$ | RCLK | $Q_A$– $Q_H$ | $C_L$ = 50 pF | | 11.2 | 17.2 | 1 | 19.3 | 1 | 21.3 | ns |
| $t_{PHL}$ | | | | | 11.2 | 17.2 | 1 | 19.3 | 1 | 21.3 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | | | 13.1 | 22.5 | 1 | 25.5 | 1 | 27.5 | |
| $t_{PHL}$ | | | | | 13.1 | 22.5 | 1 | 25.5 | 1 | 27.5 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | | | 12.4 | 18.8 | 1 | 21.1 | 1 | 23.1 | |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 10.8 | 17 | 1 | 18.3 | 1 | 20.3 | |
| $t_{PZL}$ | | | | | 13.4 | 21 | 1 | 23 | 1 | 25 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 12.2 | 18.3 | 1 | 19.5 | 1 | 21.5 | |
| $t_{PLZ}$ | | | | | 14 | 20.9 | 1 | 22.6 | 1 | 24.6 | |

## 6.10 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 80 | 120 | | 70 | | 70 | | MHz |
| | | | $C_L$ = 50 pF | 55 | 105 | | 50 | | 50 | | |
| $t_{PLH}$ | RCLK | $Q_A$– $Q_H$ | $C_L$ = 15 pF | | 6 | 11.9 | 1 | 13.5 | 1 | 14.5 | ns |
| $t_{PHL}$ | | | | | 6 | 11.9 | 1 | 13.5 | 1 | 14.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | | | 6.6 | 13 | 1 | 15 | 1 | 16 | |
| $t_{PHL}$ | | | | | 6.6 | 13 | 1 | 15 | 1 | 16 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | | | 6.2 | 12.8 | 1 | 13.7 | 1 | 14.7 | |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 6 | 11.5 | 1 | 13.5 | 1 | 14.5 | |
| $t_{PZL}$ | | | | | 7.8 | 11.5 | 1 | 13.5 | 1 | 14.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 6.1 | 14.7 | 1 | 15.2 | 1 | 16.2 | |
| $t_{PLZ}$ | | | | | 6.3 | 14.7 | 1 | 15.2 | 1 | 16.2 | |
| $t_{PLH}$ | RCLK | $Q_A$– $Q_H$ | $C_L$ = 50 pF | | 7.9 | 15.4 | 1 | 17 | 1 | 19 | ns |
| $t_{PHL}$ | | | | | 7.9 | 15.4 | 1 | 17 | 1 | 19 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | | | 9.2 | 16.5 | 1 | 18.5 | 1 | 20.5 | |
| $t_{PHL}$ | | | | | 9.2 | 16.5 | 1 | 18.5 | 1 | 20.5 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | | | 9 | 16.3 | 1 | 17.2 | 1 | 19.2 | |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 7.8 | 15 | 1 | 17 | 1 | 19 | |
| $t_{PZL}$ | | | | | 9.6 | 15 | 1 | 17 | 1 | 19 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$– $Q_H$ | | | 8.1 | 15.7 | 1 | 16.2 | 1 | 18.2 | |
| $t_{PLZ}$ | | | | | 9.3 | 15.7 | 1 | 16.2 | 1 | 18.2 | |

## 6.11 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 135 | 170 | | 115 | | 115 | | MHz |
| | | | $C_L$ = 50 pF | 120 | 140 | | 95 | | 95 | | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 15 pF | | 4.3 | 7.4 | 1 | 8.5 | 1 | 9.5 | ns |
| $t_{PHL}$ | | | | | 4.3 | 7.4 | 1 | 8.5 | 1 | 9.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | | | 4.5 | 8.2 | 1 | 9.4 | 1 | 10.4 | |
| $t_{PHL}$ | | | | | 4.5 | 8.2 | 1 | 9.4 | 1 | 10.4 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | | | 4.5 | 8 | 1 | 9.1 | 1 | 10.1 | |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | | | 4.3 | 8.6 | 1 | 10 | 1 | 11 | |
| $t_{PZL}$ | | | | | 5.4 | 8.6 | 1 | 10 | 1 | 11 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | | | 2.4 | 6 | 1 | 7.1 | 1 | 7.1 | |
| $t_{PLZ}$ | | | | | 2.7 | 5.1 | 1 | 7.2 | 1 | 7.2 | |
| $t_{PLH}$ | RCLK | $Q_A$–$Q_H$ | $C_L$ = 50 pF | | 5.6 | 9.4 | 1 | 10.5 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | | | 5.6 | 9.4 | 1 | 10.5 | 1 | 12.5 | |
| $t_{PLH}$ | SRCLK | $Q_{H'}$ | | | 6.4 | 10.2 | 1 | 11.4 | 1 | 13.4 | |
| $t_{PHL}$ | | | | | 6.4 | 10.2 | 1 | 11.4 | 1 | 13.4 | |
| $t_{PHL}$ | $\overline{SRCLR}$ | $Q_{H'}$ | | | 6.4 | 10 | 1 | 11.1 | 1 | 13.1 | |
| $t_{PZH}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | | | 5.7 | 10.6 | 1 | 12 | 1 | 14 | |
| $t_{PZL}$ | | | | | 6.8 | 10.6 | 1 | 12 | 1 | 14 | |
| $t_{PHZ}$ | $\overline{OE}$ | $Q_A$–$Q_H$ | | | 3.5 | 10.3 | 1 | 11 | 1 | 13 | |
| $t_{PLZ}$ | | | | | 3.4 | 10.3 | 1 | 11 | 1 | 13 | |

## 6.12 Noise Characteristics

$V_{CC}$ = 3.3 V, $C_L$ = 50 pF, $T_A$ = 25°C(1)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.3 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.2 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | | 2.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 0.99 | V |

(1) Characteristics are for surface-mount packages only.

## 6.13 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 10 MHz | 3.3 V | 111 | pF |
| | | | | 5 V | 114 | |

## 6.14 Typical Characteristics

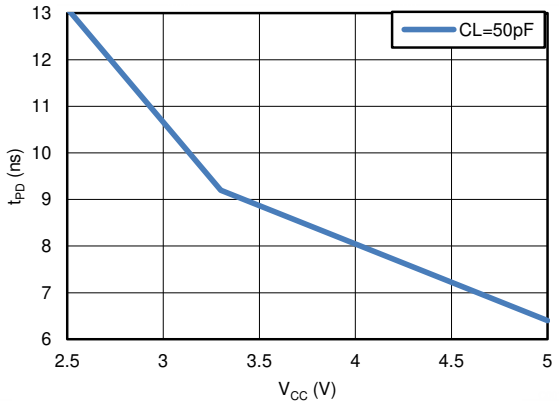
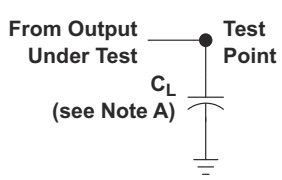
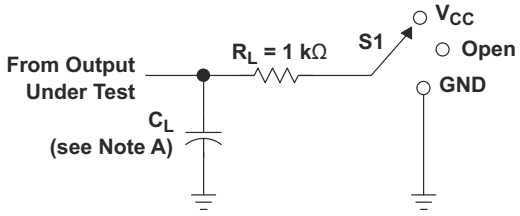



**Figure 6-2. TPD vs $V_{CC}$**

# 7 Parameter Measurement Information

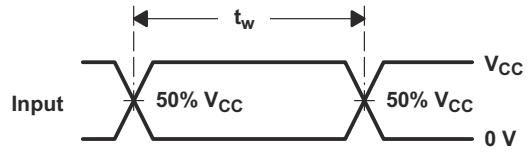



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

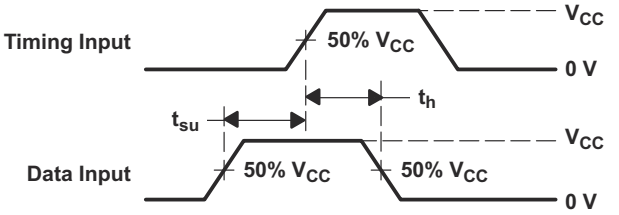



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

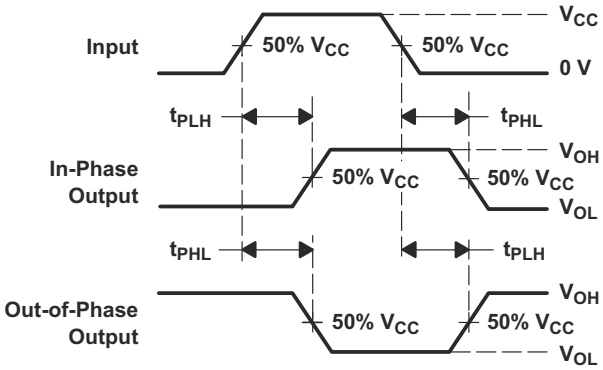
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



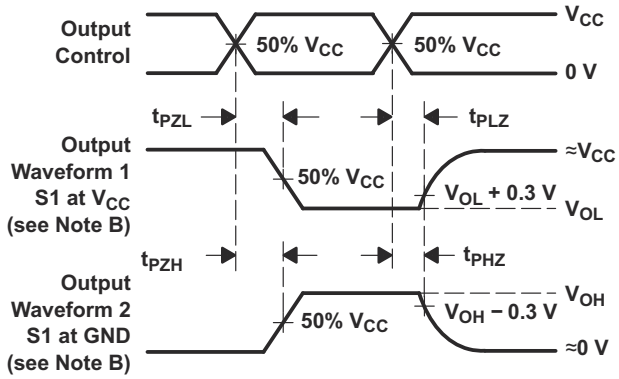

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PHL}$ and $t_{PLH}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 7-1. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SN74LV595A device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for the shift and storage registers. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, serial (SER) input, and serial outputs for cascading. When the output-enable ($\overline{OE}$) input is high, the outputs are in the high-impedance state. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, then the shift register always is one clock pulse ahead of the storage register.

## 8.2 Functional Block Diagram

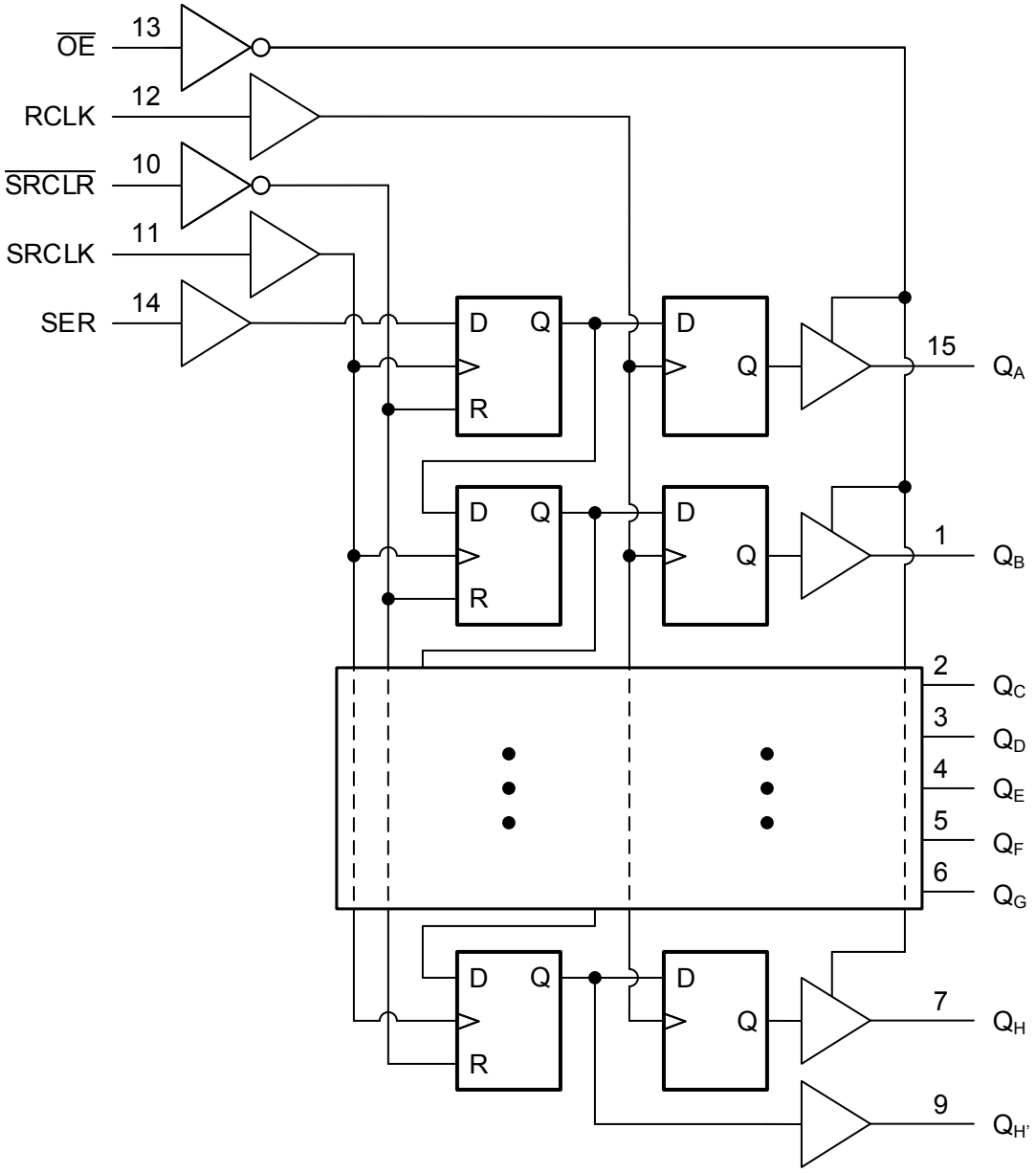



**Figure 8-1. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

### 8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

### 8.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

### 8.3.4 Partial Power Down ($I_{off}$)

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the $I_{off}$ specification in the *Electrical Characteristics* table.

### 8.3.5 Clamp Diode Structure

Figure 8-2 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

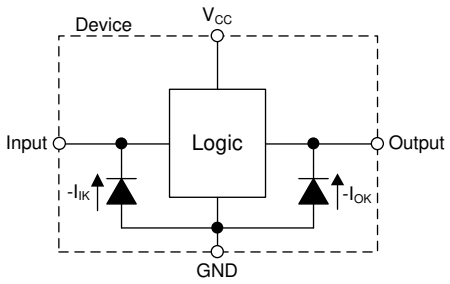



**Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 8-1. Function Table**

| INPUTS(1) | | | | | FUNCTION |
|---|---|---|---|---|---|
| SER | SRCLK | $\overline{\text{SRCLR}}$ | RCLK | $\overline{\text{OE}}$ | |
| X | X | X | X | H | Outputs $Q_A$–$Q_H$ are disabled. $Q_{H'}$ Remains enabled. |
| X | X | X | X | L | Outputs $Q_A$–$Q_H$ are enabled. |
| X | X | L | X | X | Shift register is cleared. |
| L | ↑ | H | X | X | First stage of the shift register goes low. Other stages store the data of previous stage, respectively. |
| H | ↑ | H | X | X | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X | X | X | ↑ | X | Shift-register data is stored in the storage register. |

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LV595A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are 5-V tolerant allowing for down translation to $V_{CC}$.

## 9.2 Typical Application

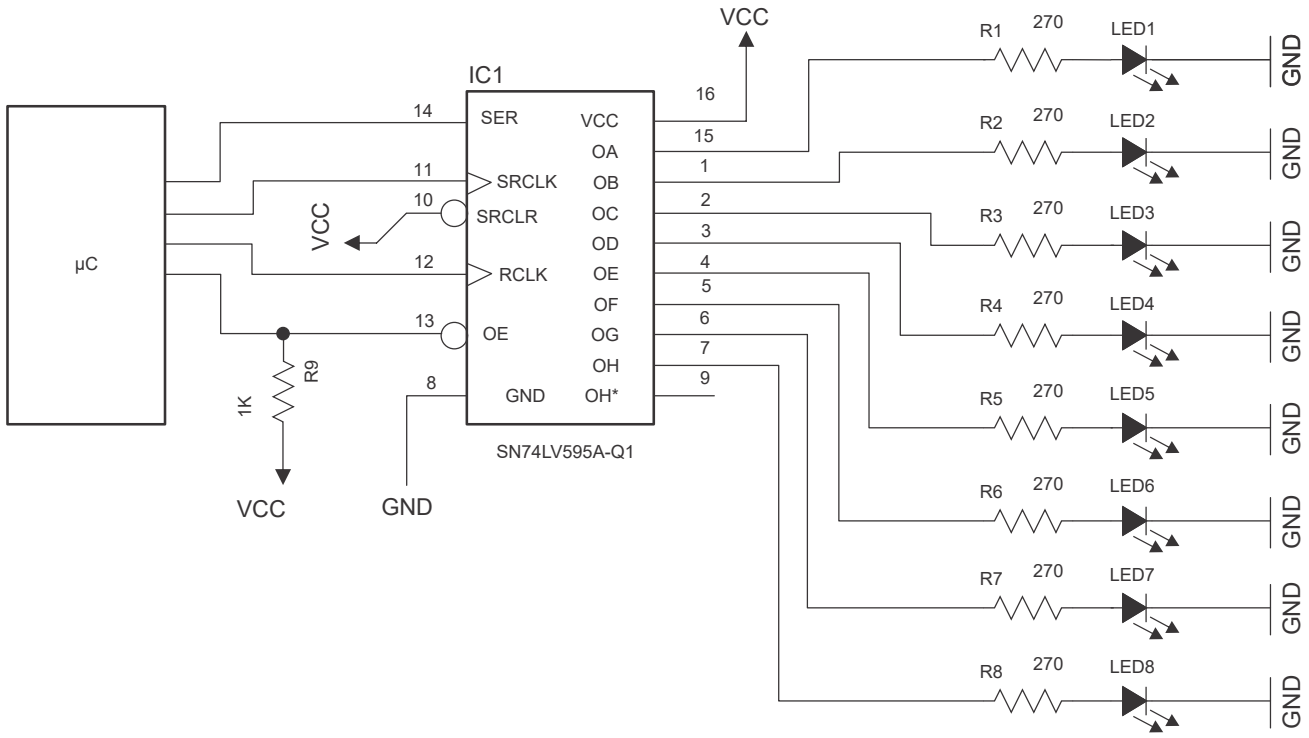



**Figure 9-1. SN74LV595A Expanding IOs to Drive LEDs**

### 9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV595A plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV595A plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV595A can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV595A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV595A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV595A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

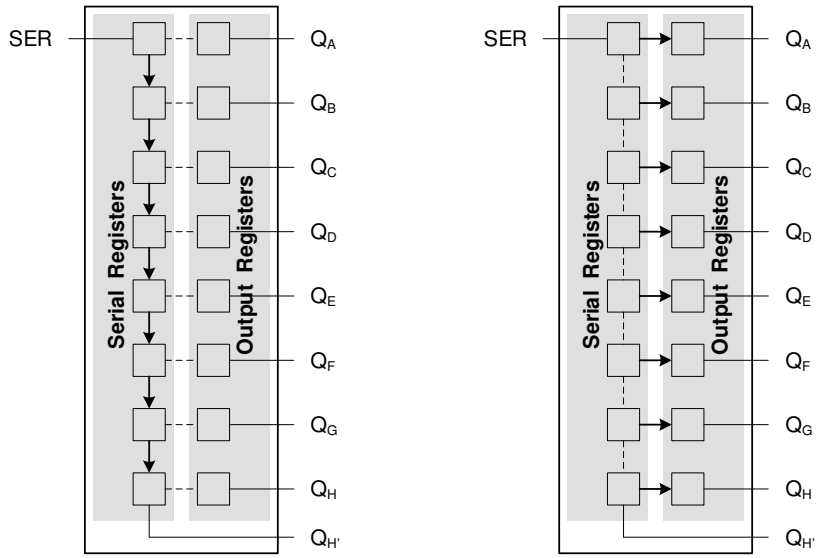
### 9.2.4 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 9.2.5 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV595A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

### 9.2.6 Application Curves




SRCLK rising edge shifts data in the serial registers only

RCLK rising edge shifts data to the output registers

**Figure 9-2. Simplified Functional Diagram Showing Clock Operation**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF capacitor is recommended. If there are multiple $V_{CC}$ terminals then 0.01 µF or 0.022 µF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 µF and 1.0 µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

# 11 Layout

## 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.

## 11.2 Layout Example

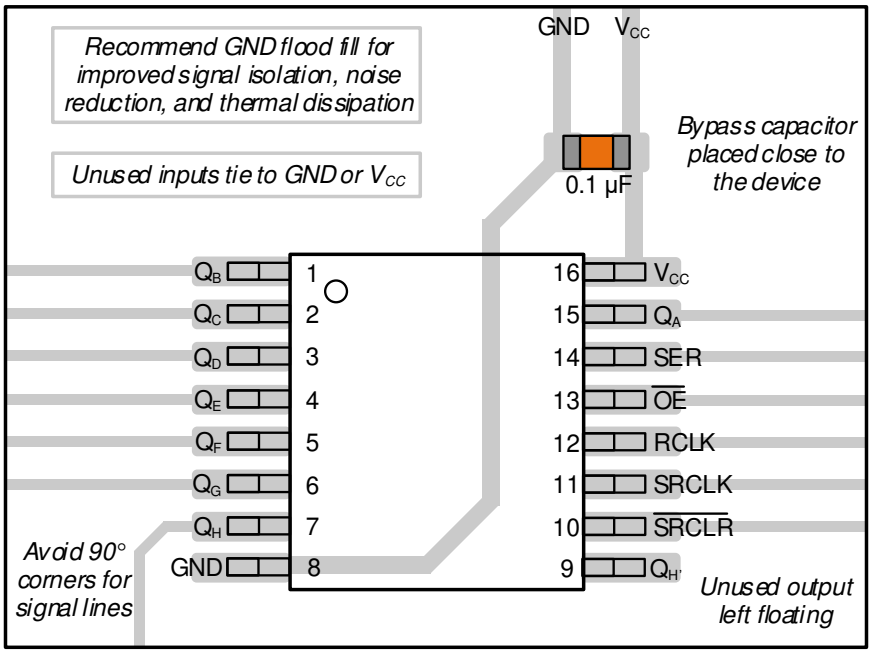



**Figure 11-1. Layout Example for the SN74LV595A in TSSOP**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* appliation report

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PSN74LV595ABQBR | ACTIVE | WQFN | BQB | 16 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| SN74LV595ABQBR | ACTIVE | WQFN | BQB | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV594A | Samples |
| SN74LV595AD | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595ADRG3 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595ANSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV595A | Samples |
| SN74LV595APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595APWRG3 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595APWT | ACTIVE | TSSOP | PW | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV595A | Samples |
| SN74LV595ARGYR | ACTIVE | VQFN | RGY | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV595A | Samples |
| SN74LV595ARGYRG4 | ACTIVE | VQFN | RGY | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV595A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN74LV595A :**

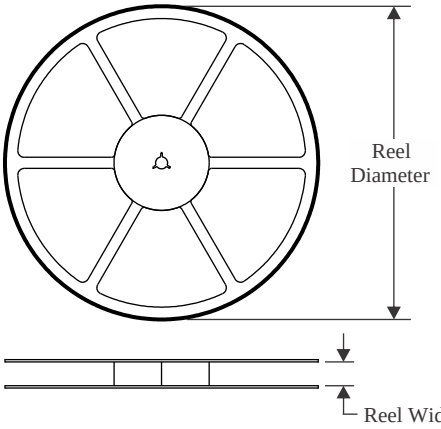
- Automotive : SN74LV595A-Q1
- Enhanced Product : SN74LV595A-EP

NOTE: Qualified Version Definitions:

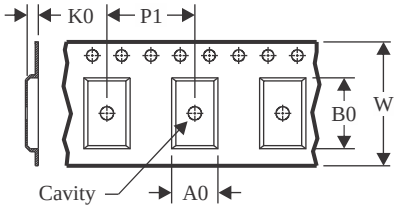
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

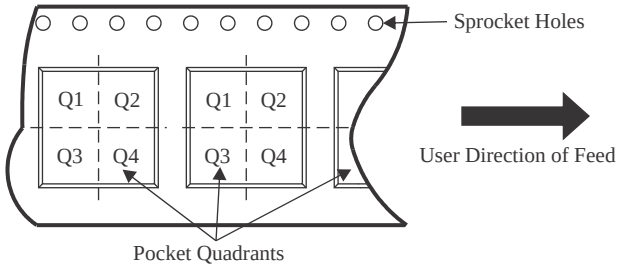



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

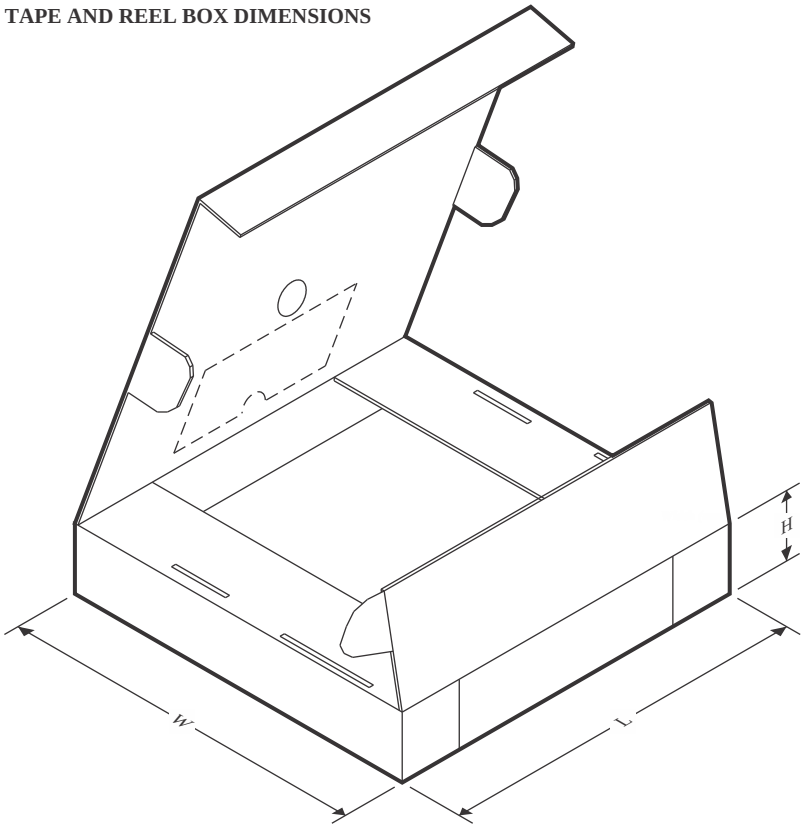
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV595ABQBR | WQFN | BQB | 16 | 3000 | 180.0 | 12.4 | 2.8 | 3.8 | 1.2 | 4.0 | 12.0 | Q1 |
| SN74LV595ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV595ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV595ADRG3 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV595ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV595ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV595APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595APWRG3 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595APWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV595ARGYR | VQFN | RGY | 16 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q1 |

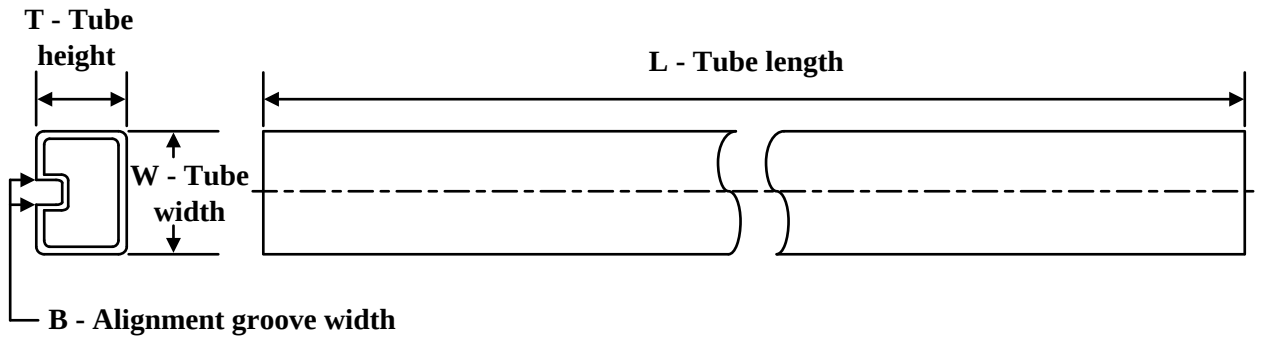
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

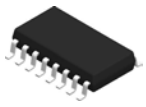
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV595ABQBR | WQFN | BQB | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LV595ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV595ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV595ADRG3 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74LV595ADRG4 | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV595ANSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV595APWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV595APWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV595APWRG3 | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV595APWRG4 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV595APWT | TSSOP | PW | 16 | 250 | 356.0 | 356.0 | 35.0 |
| SN74LV595ARGYR | VQFN | RGY | 16 | 3000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LV595AD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |

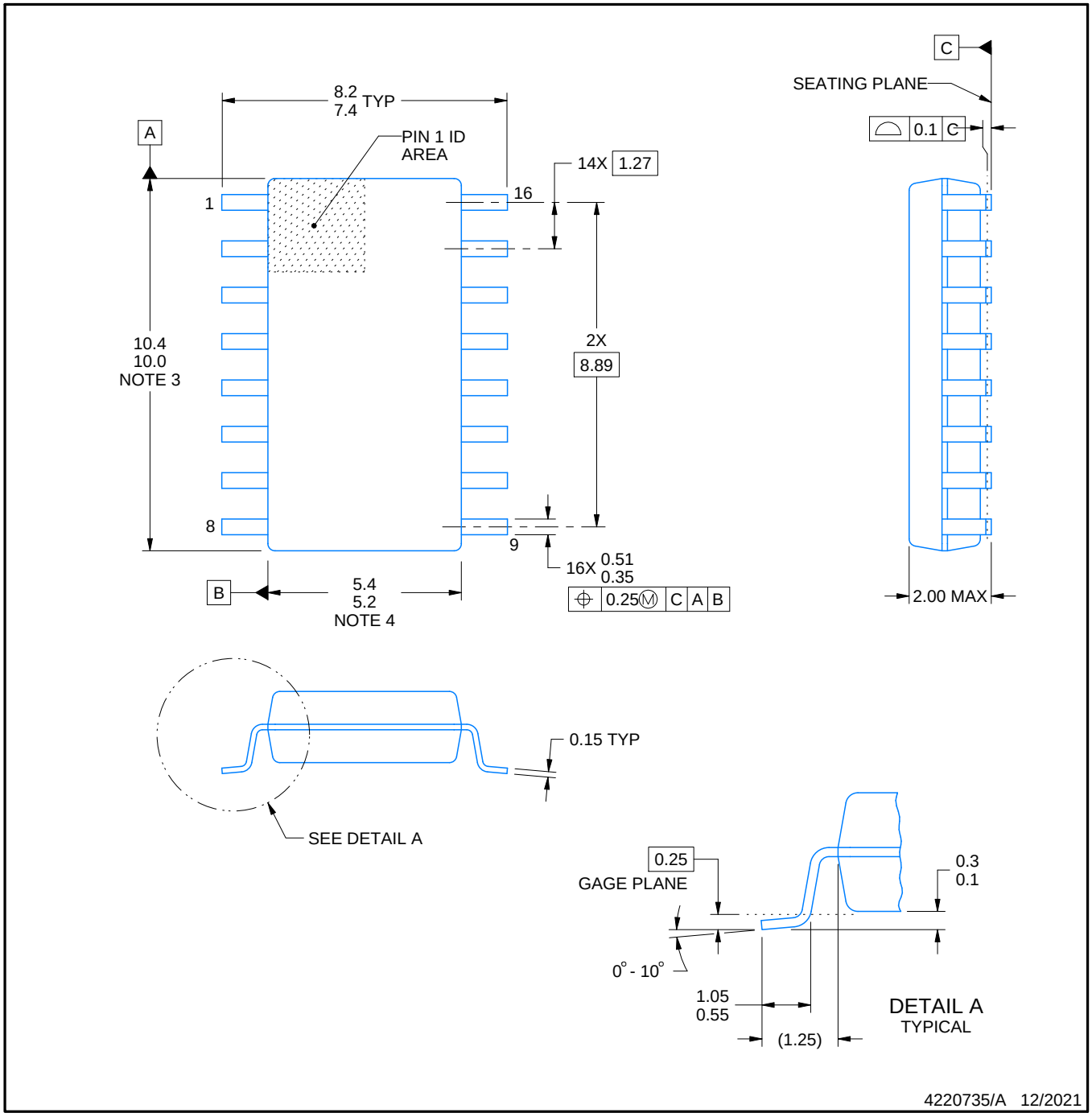


# PACKAGE OUTLINE

## NS0016A

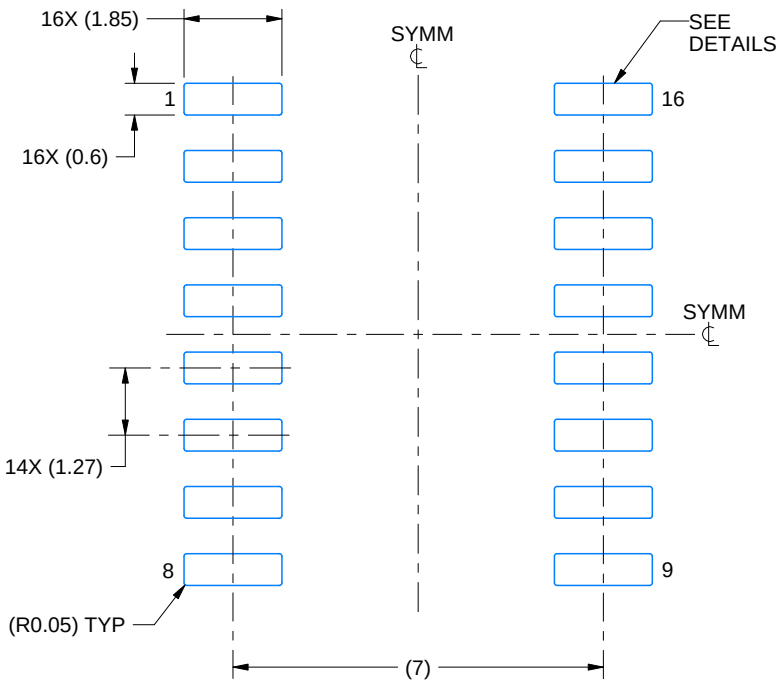
## SOP - 2.00 mm max height

SOP

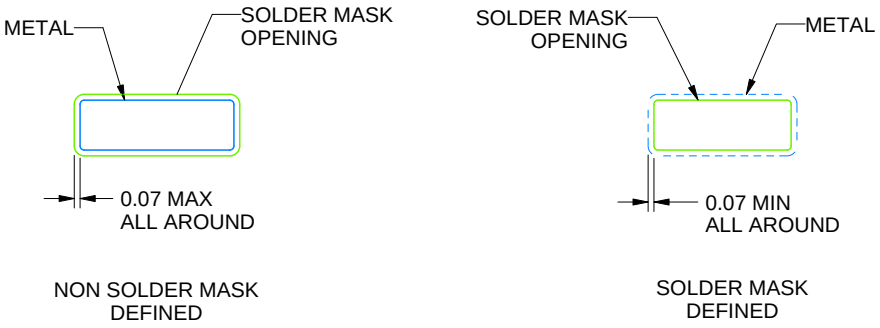



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

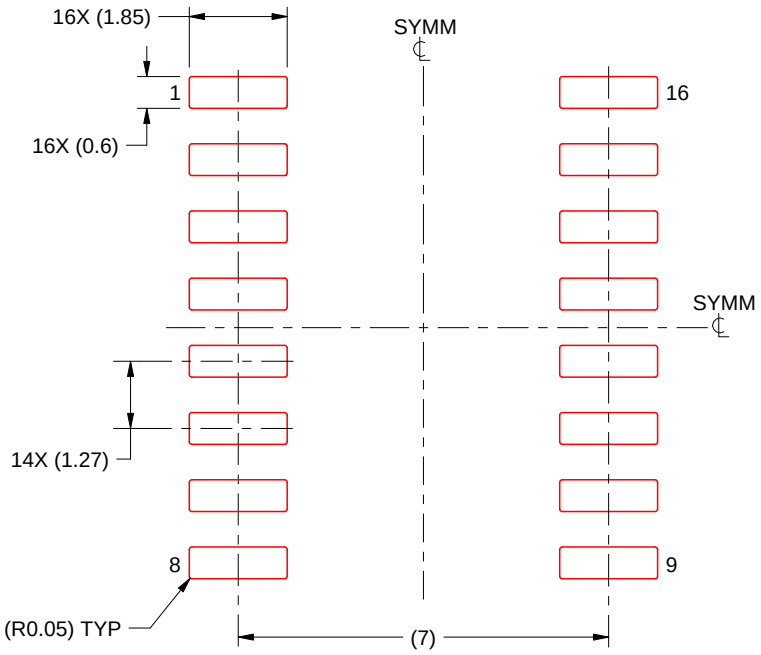
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



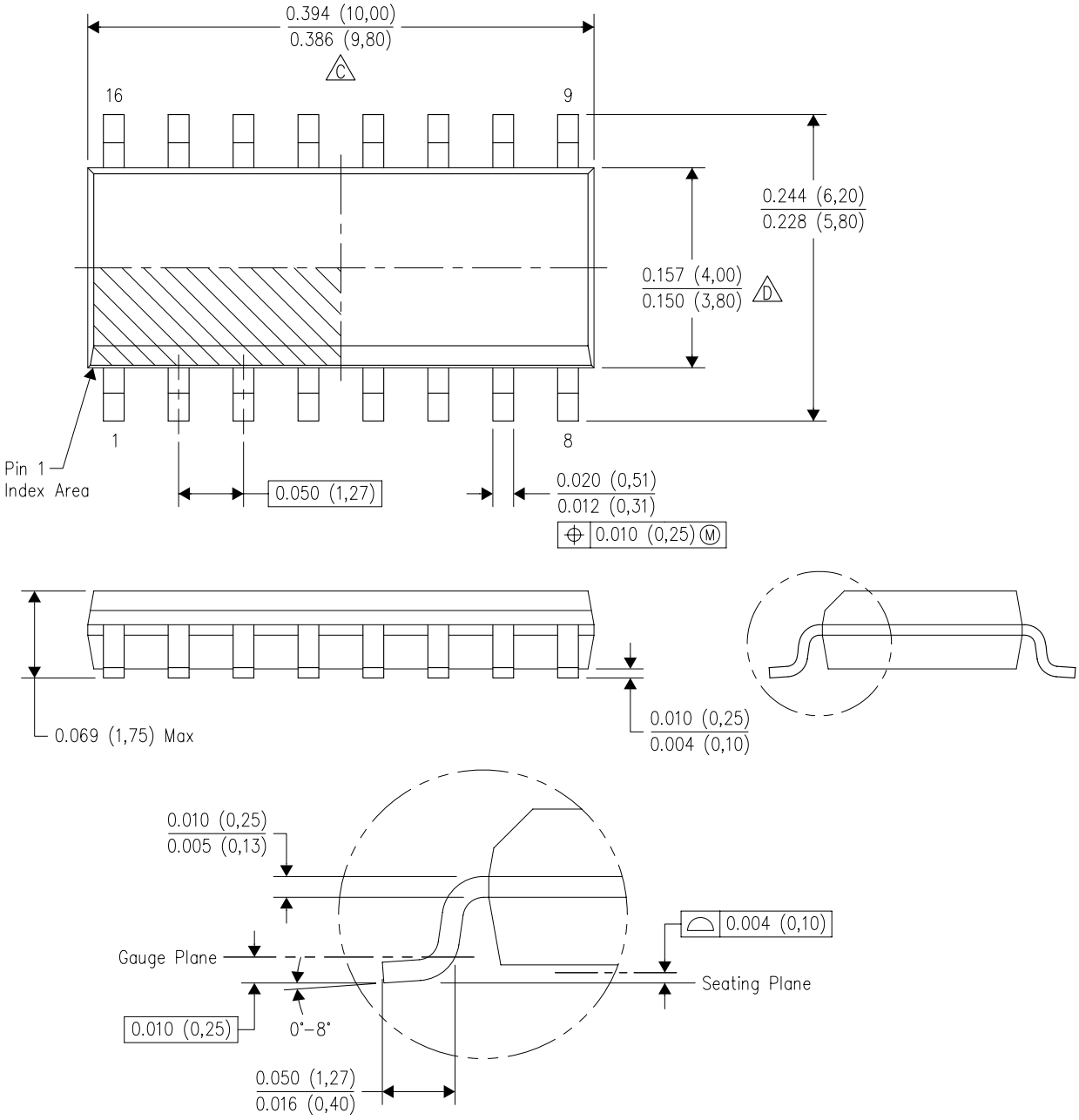

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

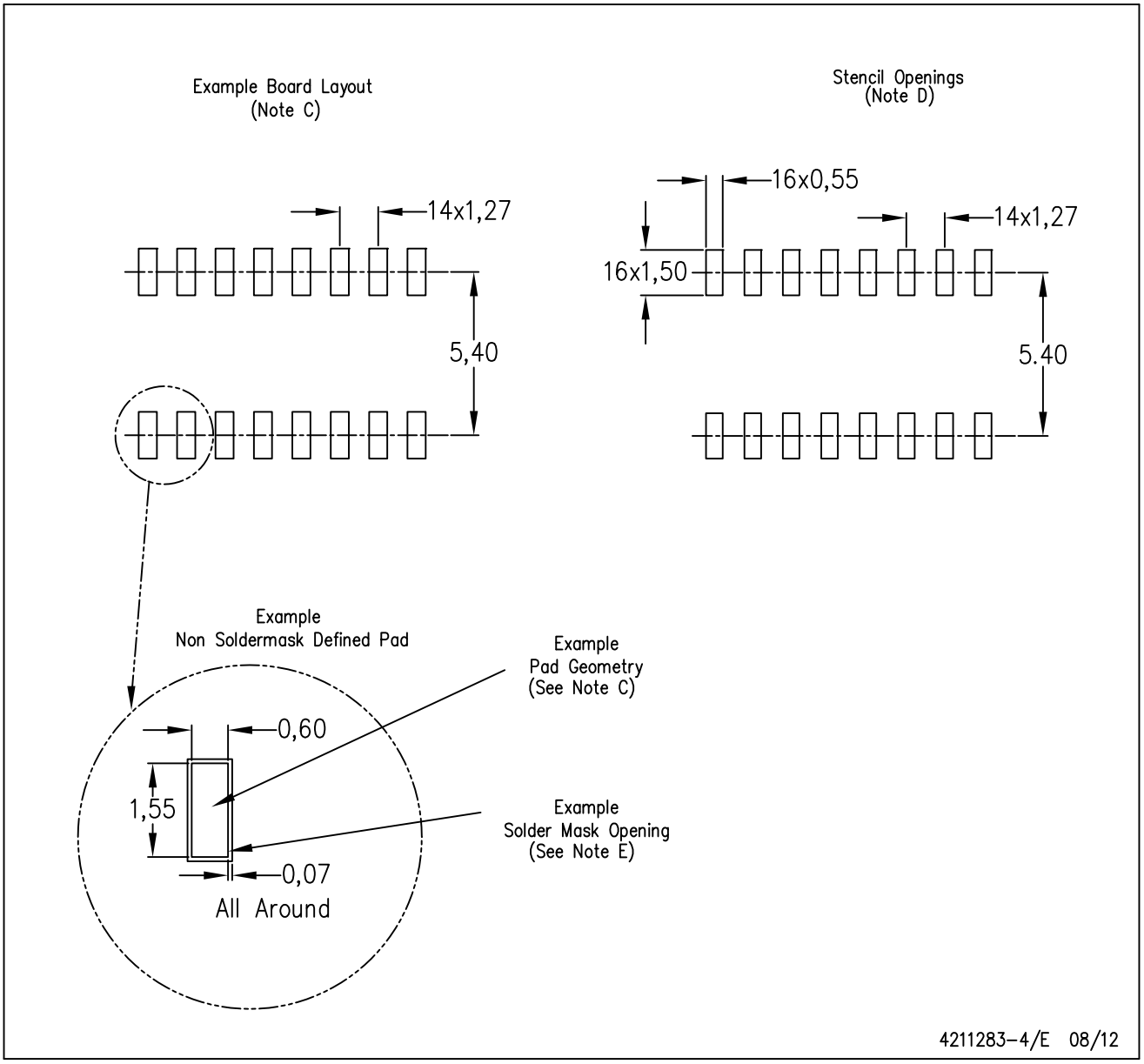
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



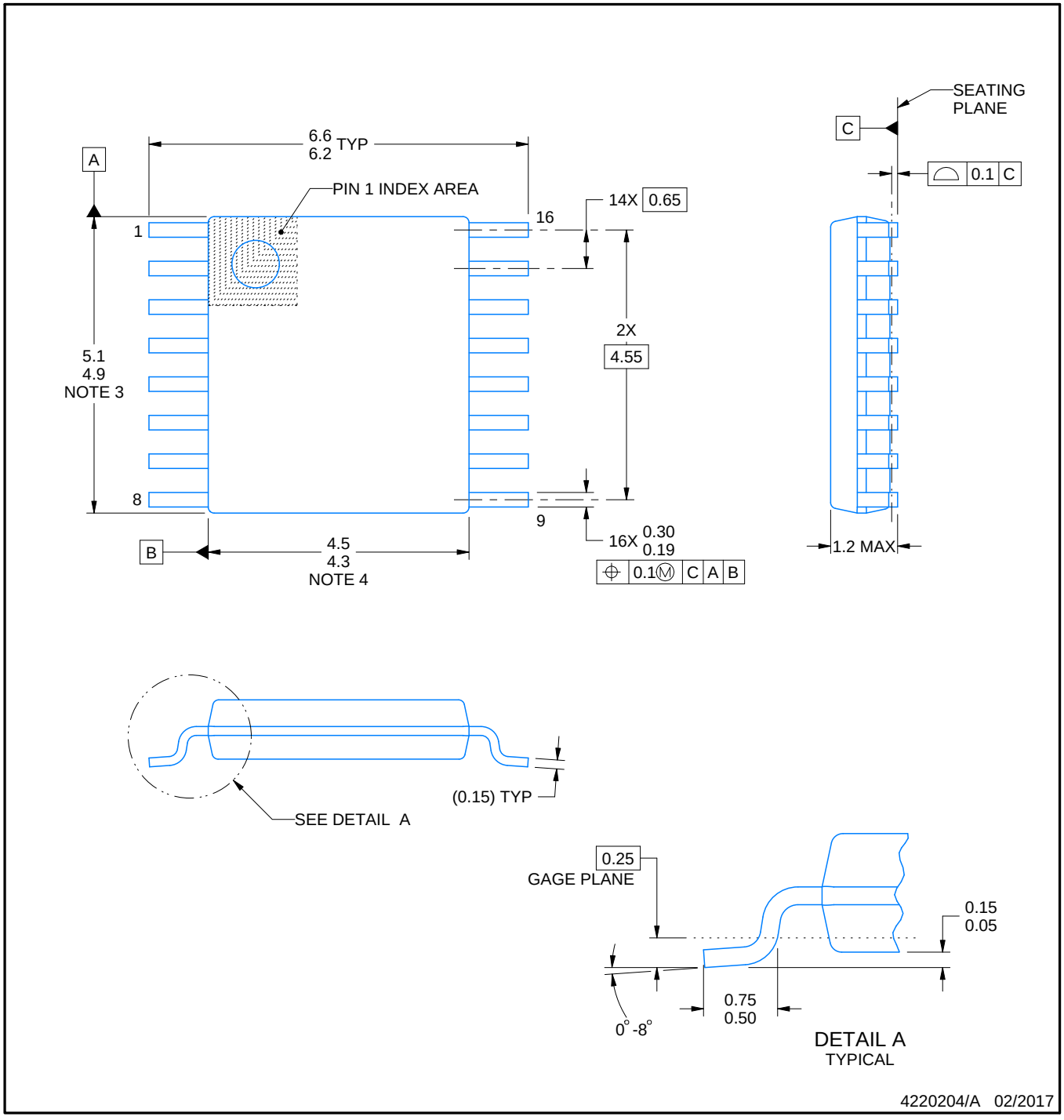

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## PW0016A

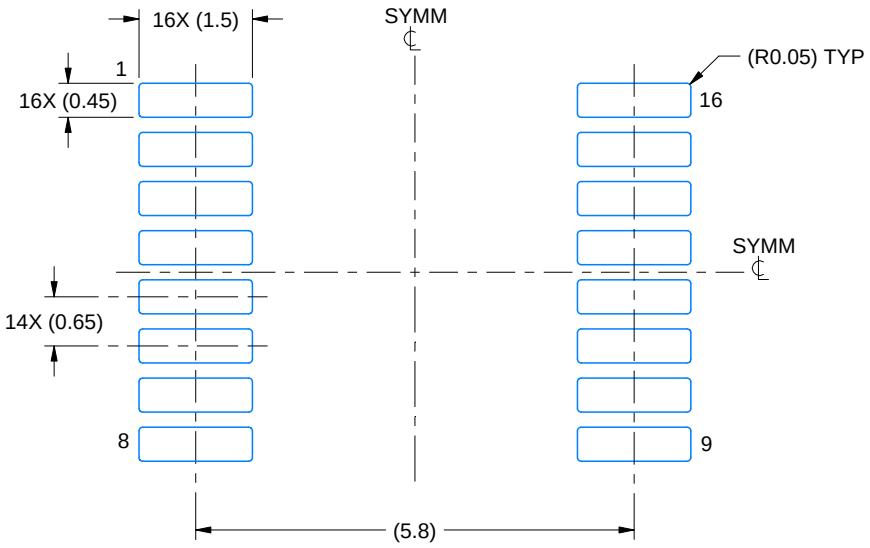
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

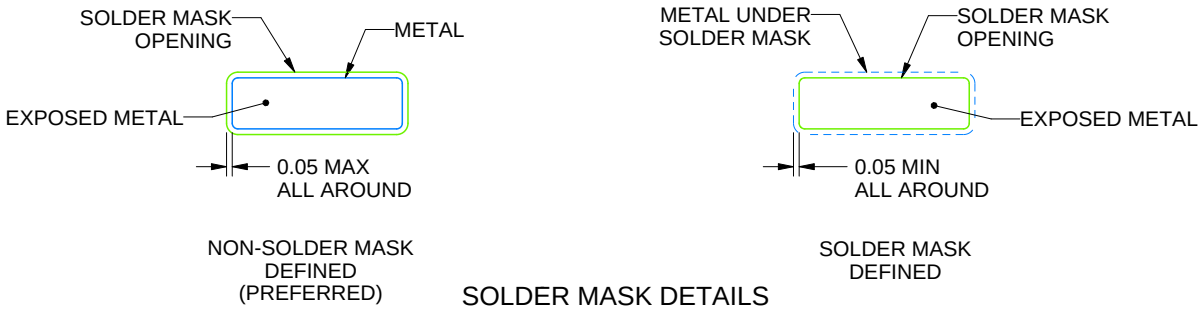



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

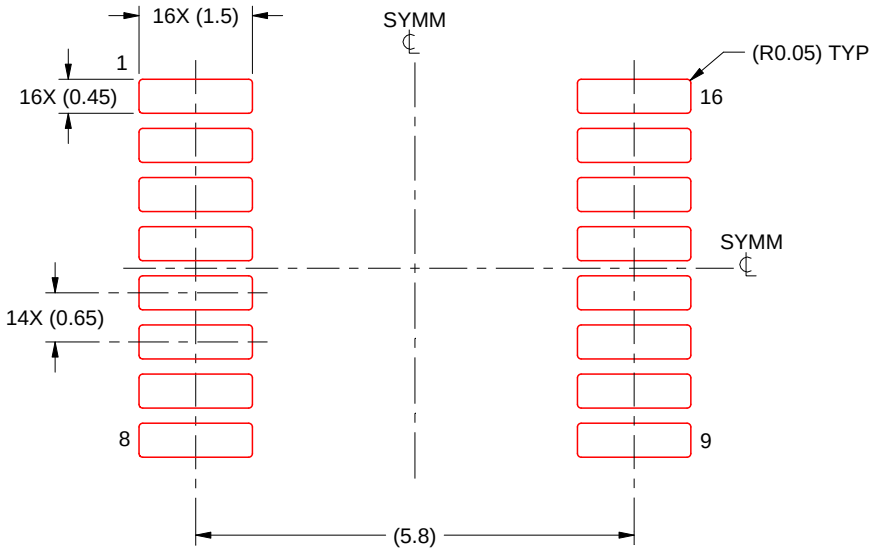



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

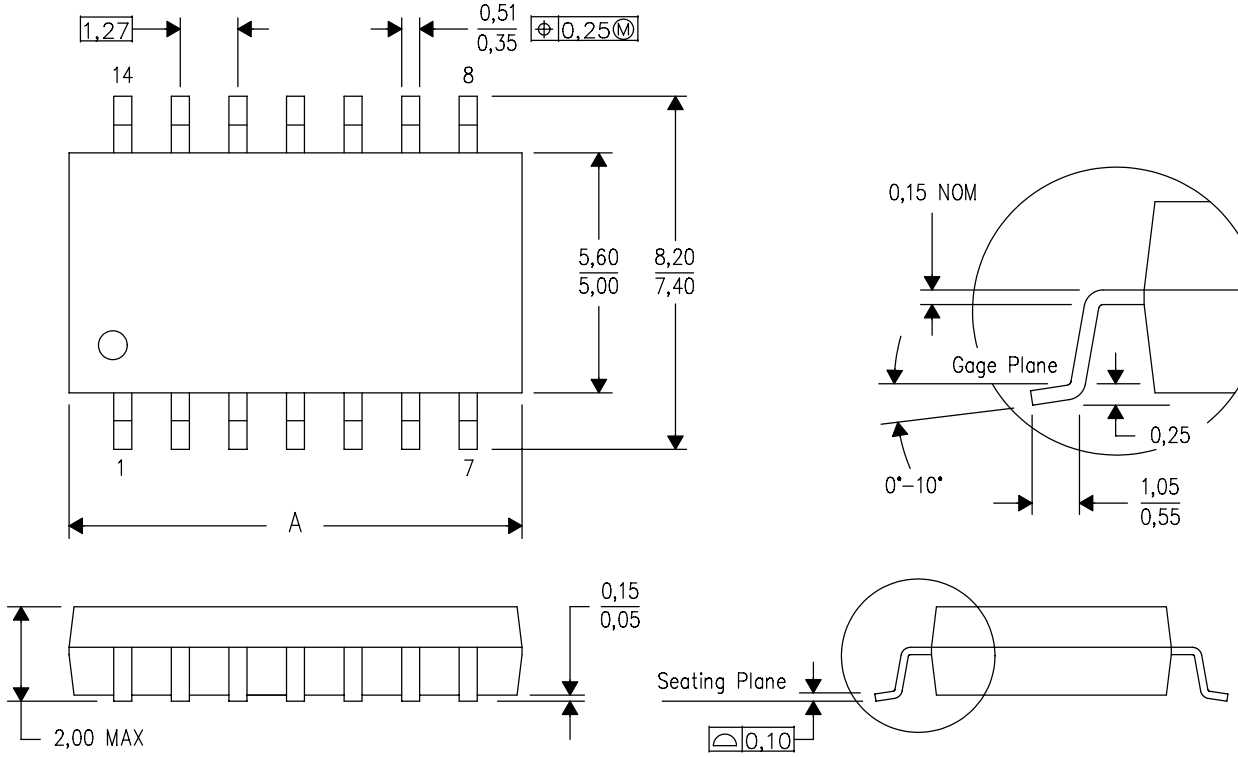
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# GENERIC PACKAGE VIEW

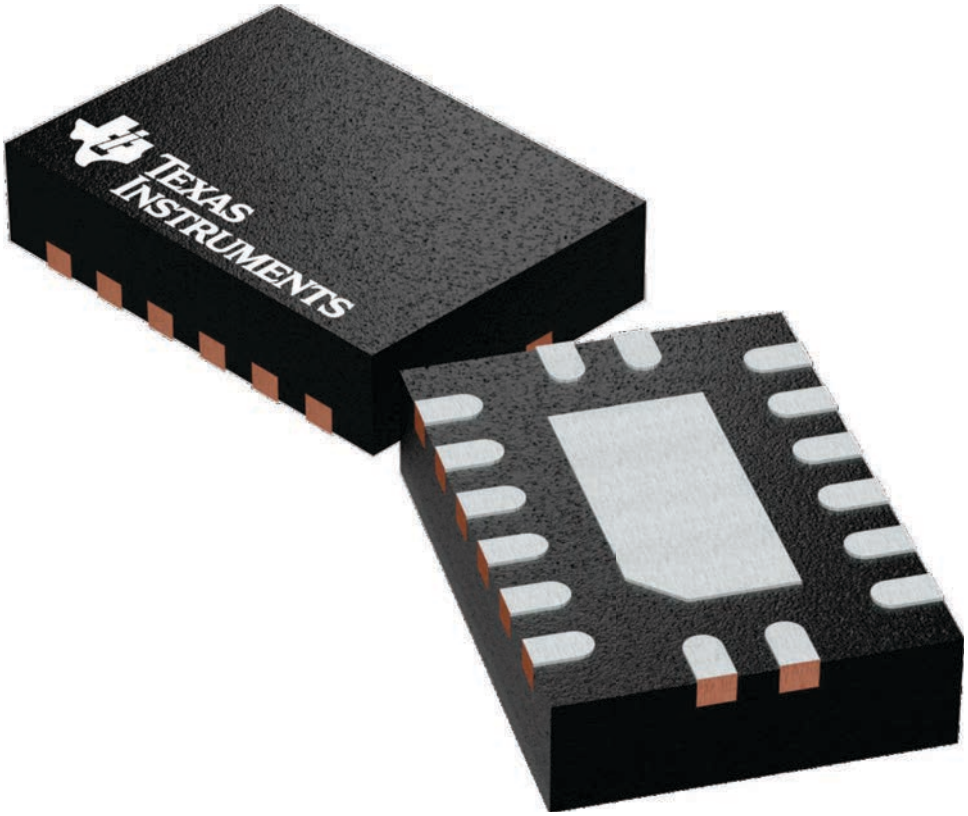
## BQB 16

## WQFN - 0.8 mm max height

**2.5 x 3.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



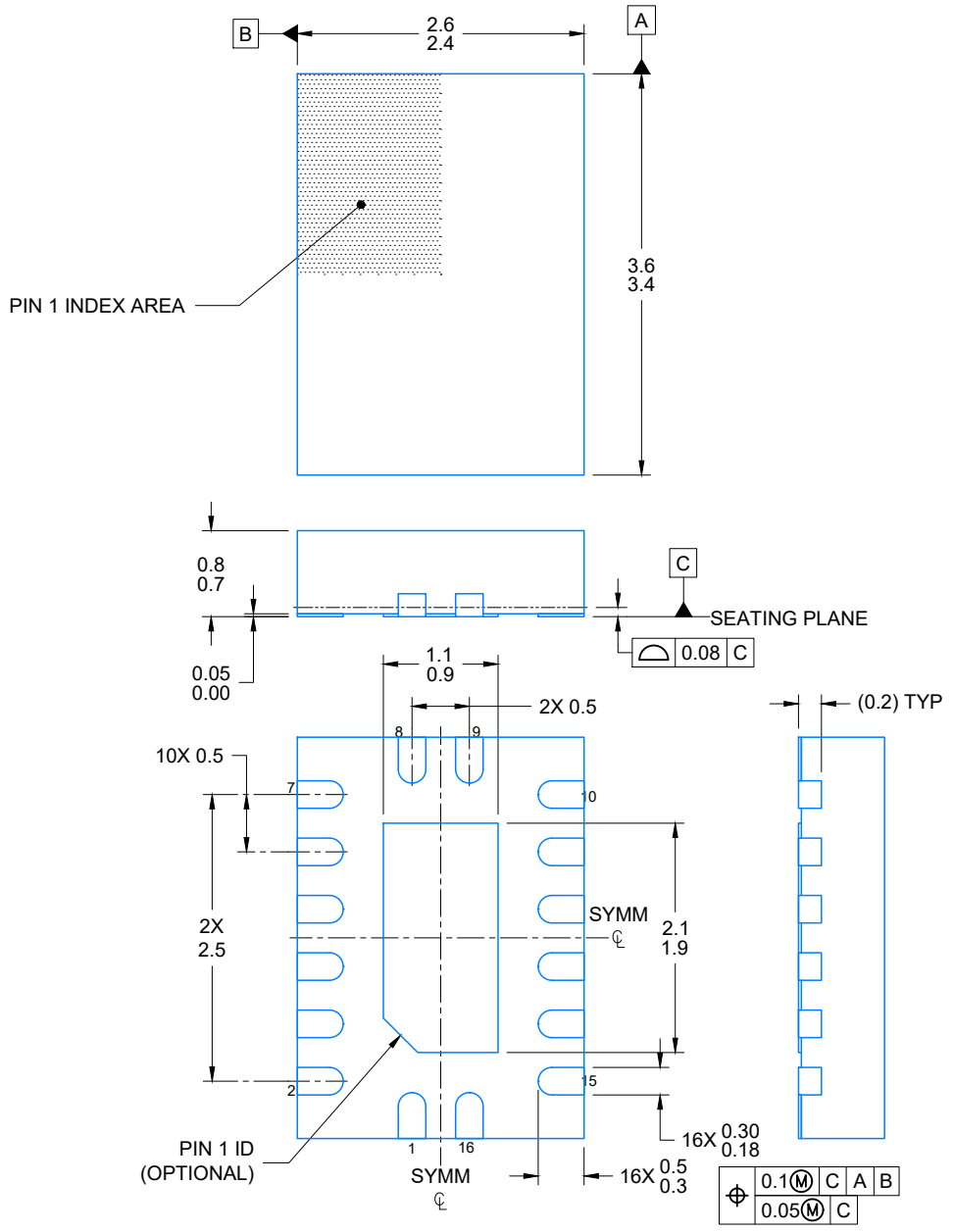

4226161/A

# PACKAGE OUTLINE

## BQB0016A

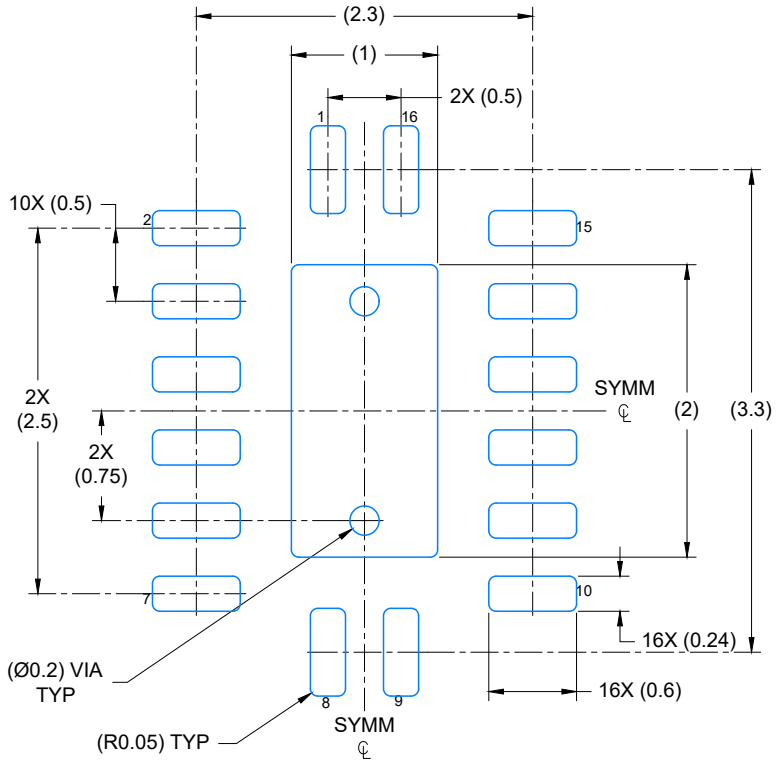
## WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

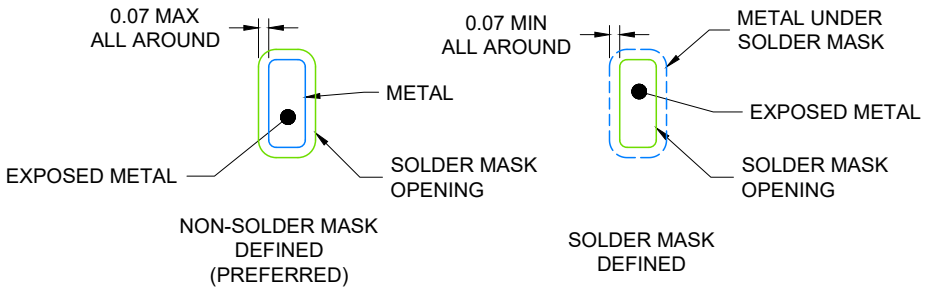



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



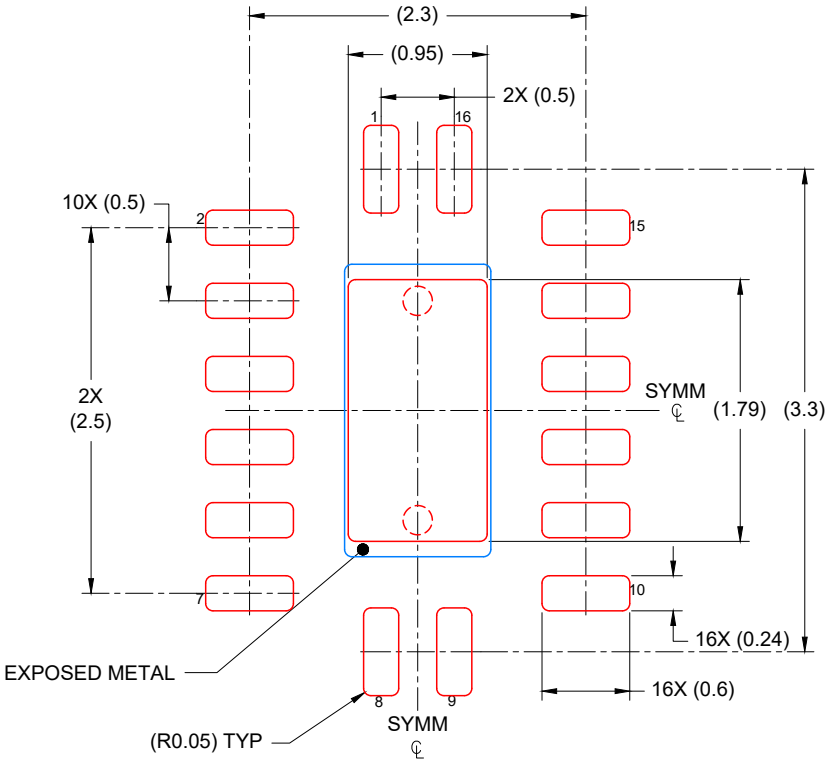

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

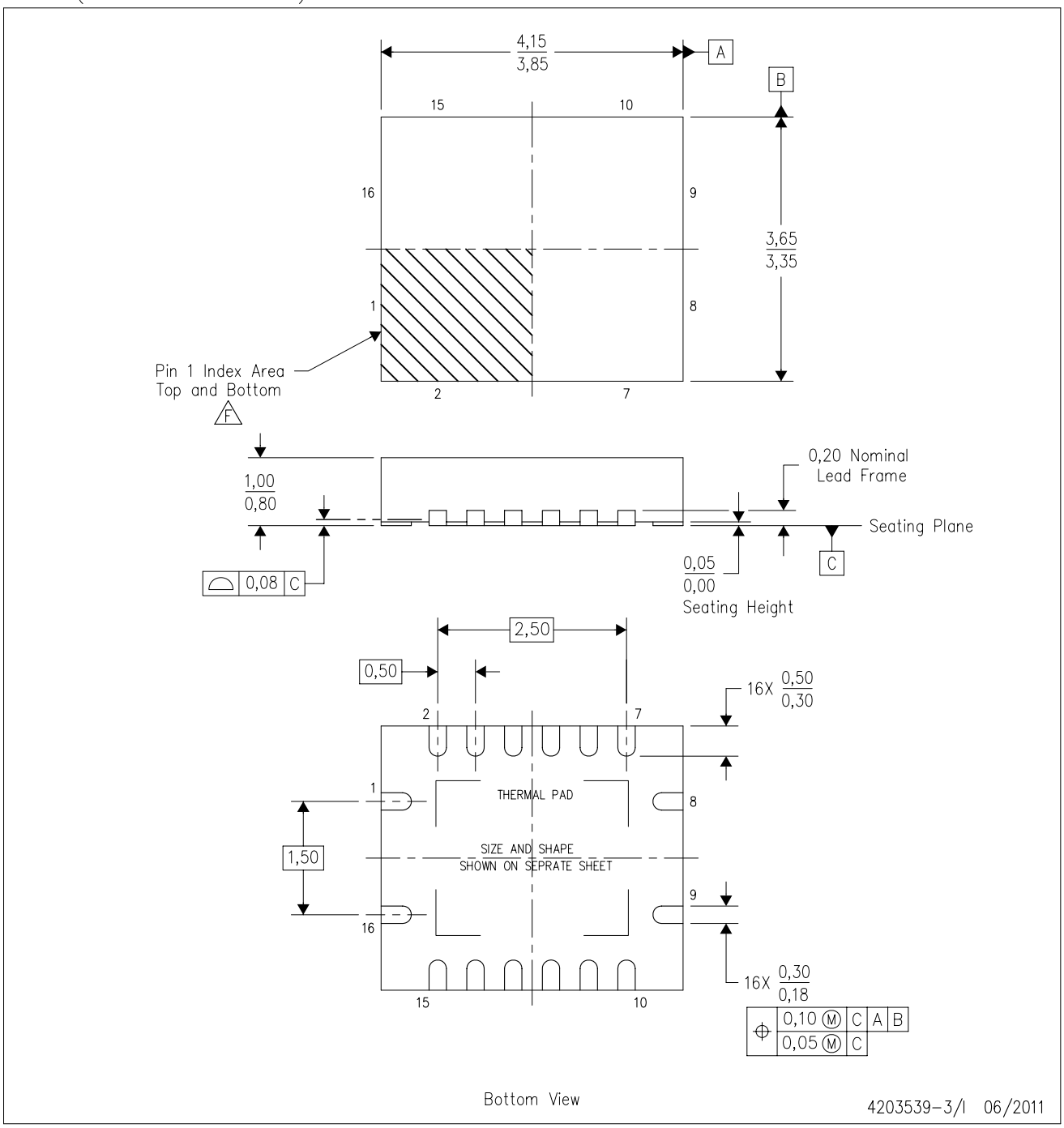
EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

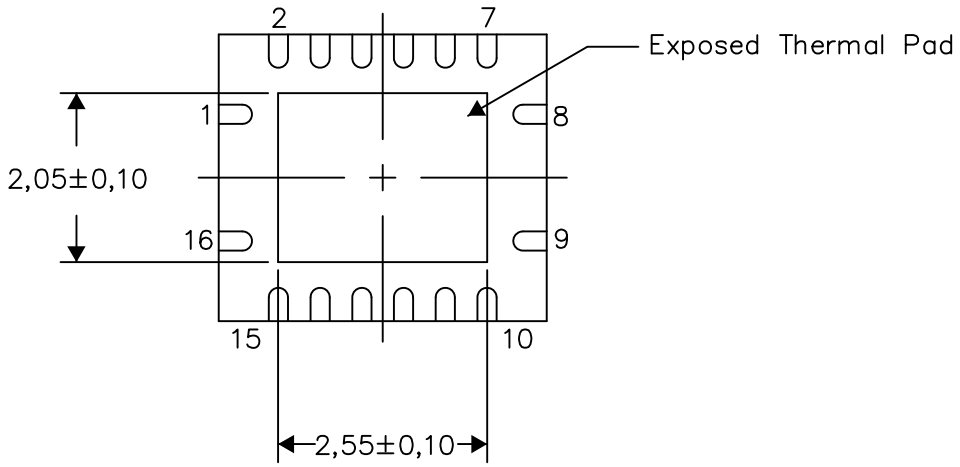
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



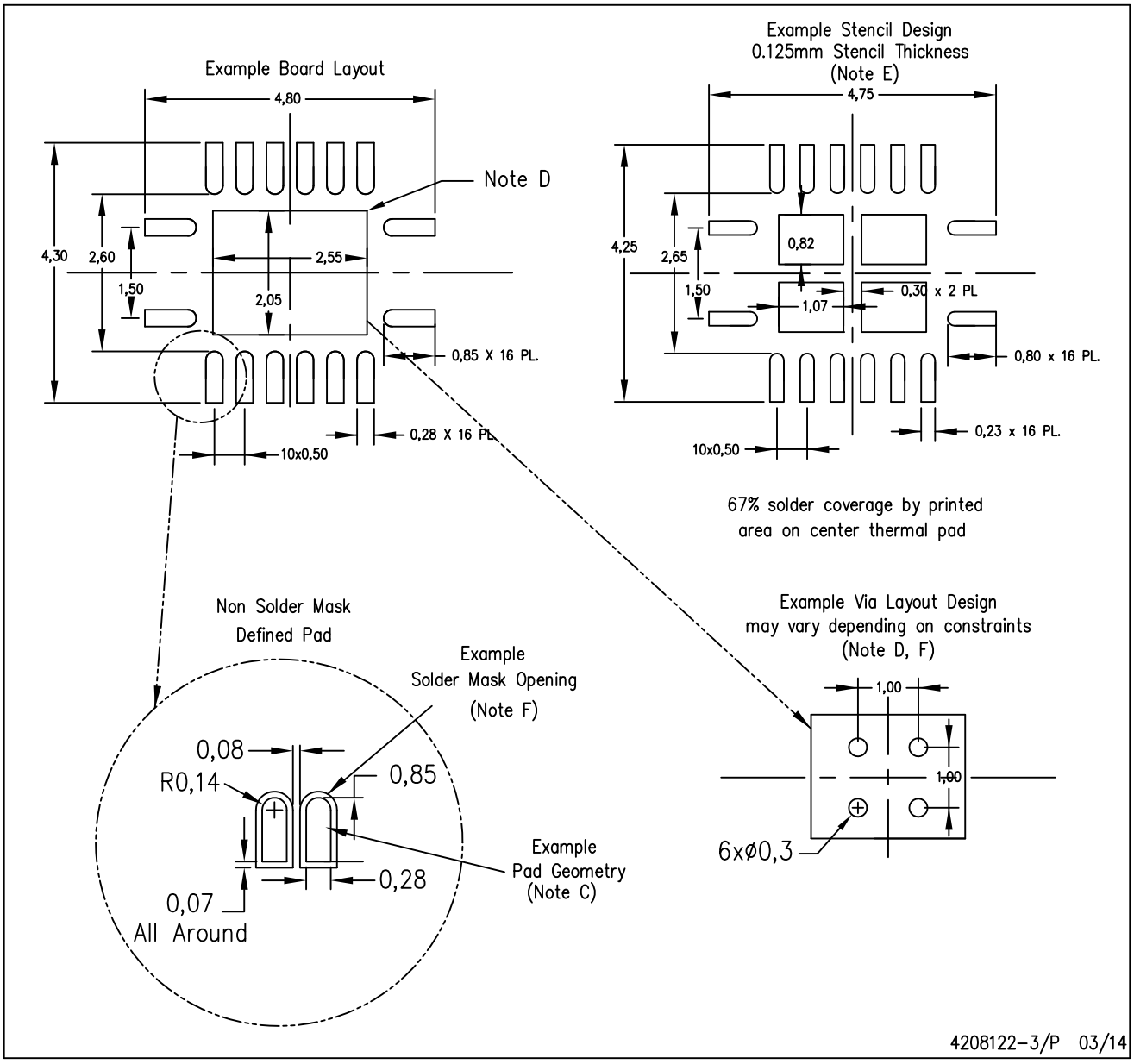

Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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