



Integrated Device Technology, Inc.

# MULTILEVEL PIPELINE REGISTERS

## IDT29FCT520AT/BT/CT/DT IDT29FCT521AT/BT/CT/DT

### FEATURES:

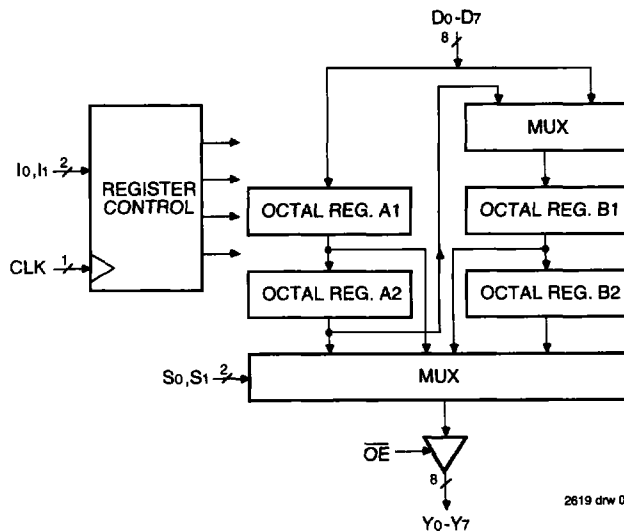
- A, B, C and D speed grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- High drive outputs (-15mA IOH, 48mA IOL)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

### DESCRIPTION:

The IDT29FCT520AT/BT/CT/DT and IDT29FCT521AT/BT/CT/DT each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520AT/BT/CT/DT when data is entered into the first level ( $I = 2$  or  $I = 1$ ), the existing data in the first level is moved to the second level. In the IDT29FCT521AT/BT/CT/DT, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction ( $I = 0$ ). This transfer also causes the first level to change. In either part  $I=3$  is for hold.

### FUNCTIONAL BLOCK DIAGRAM

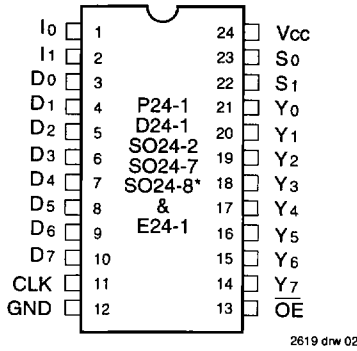


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MILITARY AND COMMERCIAL TEMPERATURE RANGES

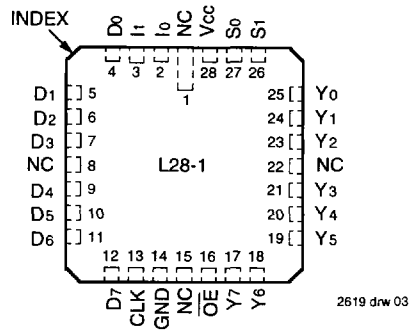
JUNE 1996

**PIN CONFIGURATIONS**



**DIP/SOIC/SSOP/QSOP/CERPACK  
 TOP VIEW**

\*FCT520 only



**LCC  
 TOP VIEW**

2619 drw 03

**DEFINITION OF FUNCTIONAL TERMS**

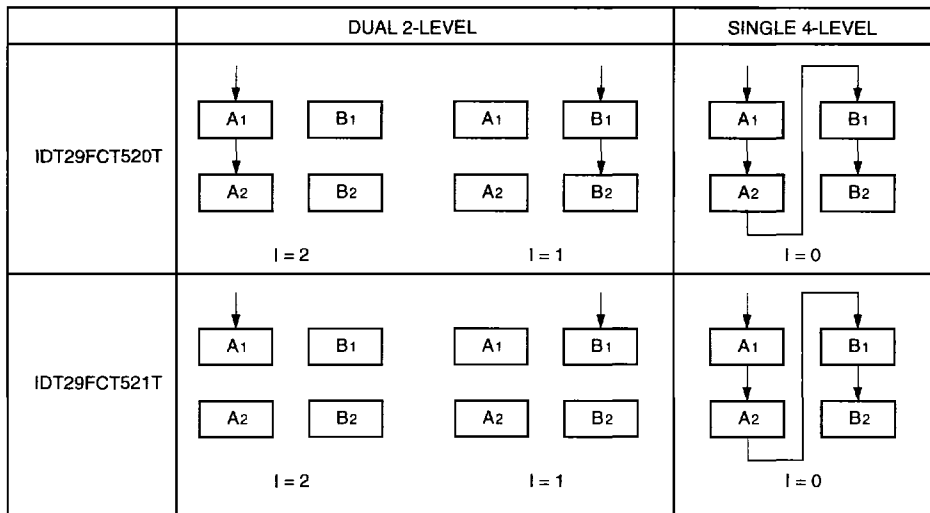
Pin Names	Description
D <sub>n</sub>	Register input Port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I <sub>0</sub> , I <sub>1</sub>	Instruction inputs. See Figure 1 and instruction Control Tables.
S <sub>0</sub> , S <sub>1</sub>	Multiplexer select. Inputs either register A <sub>1</sub> , A <sub>2</sub> , B <sub>1</sub> or B <sub>2</sub> data to be available at the output port.
OE	Output enable for 3-state output port.
Y <sub>n</sub>	Register output port.

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**REGISTER SELECTION**

S <sub>1</sub>	S <sub>0</sub>	Register
0	0	B <sub>2</sub>
0	1	B <sub>1</sub>
1	0	A <sub>2</sub>
1	1	A <sub>1</sub>

2619 tbl 02



**NOTE:**  
 1. l = 3 for hold.

**Figure 1. Data Loading in 2-Level Operation**

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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC +0.5	-0.5 to VCC +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

**NOTES:**

2619 Ink 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Input and Vcc terminals only.
- Outputs and I/O terminals only.

**CAPACITANCE (TA = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

**NOTE:**

2619 Ink 04

- This parameter is measured at characterization but not tested.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
IiH	Input HIGH Current <sup>(4)</sup>	VCC = Max.	VI = 2.7V	—	—	±1	µA
IiL	Input LOW Current <sup>(4)</sup>	VCC = Max.	VI = 0.5V	—	—	±1	µA
IoZH	High Impedance <sup>(4)</sup>	VCC = Max.	VO = 2.7V	—	—	±1	µA
IoZL	Output Current		VO = 0.5V	—	—	±1	µA
Ii	Input HIGH Current <sup>(4)</sup>	VCC = Max., VI = VCC (Max.)		—	—	±1	µA
Vik	Clamp Diode Voltage	VCC = Min., IN = -18mA		—	-0.7	-1.2	V
Ios	Short Circuit Current	VCC = Max. <sup>(3)</sup> , VO = GND		-60	-120	-225	mA
VOH	Output HIGH Voltage	VCC = Min. VIN = VIH or VIL	IoH = -6mA MIL. IoH = -8mA COM'L.	2.4	3.3	—	V
			IoH = -12mA MIL. IoH = -15mA COM'L.	2.0	3.0	—	
VOL	Output LOW Voltage	VCC = Min. VIN = VIH or VIL	IoL = 32mA MIL. IoL = 48mA COM'L.	—	0.3	0.5	V
VH	Input Hysteresis	—		—	200	—	mV
ICC	Quiescent Power Supply Current	VCC = Max. VIN = GND or VCC		—	0.01	1	mA

**NOTES:**

2619 Ibl 05

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is ±5µA at TA = -55°C.

**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current, TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.0	5.5	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.0	16.3 <sup>(5)</sup>	

2619 tbl 06

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ , +25°C ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} \cdot D_H \cdot N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.



**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	FCT520AT/521AT				FCT520BT/521BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPHL tPLH	Propagation Delay CLK to Y <sub>n</sub>	CL = 50pF RL = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	ns
tPHL tPLH	Propagation Delay S <sub>0</sub> or S <sub>1</sub> to Y <sub>n</sub>		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	ns
tSU	Set-up Time, HIGH or LOW D <sub>n</sub> to CLK		5.0	—	6.0	—	2.5	—	2.8	—	ns
tH	Hold Time, HIGH or LOW D <sub>n</sub> to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
tSU	Set-up Time, HIGH or LOW I <sub>0</sub> or I <sub>1</sub> to CLK		5.0	—	6.0	—	4.0	—	4.5	—	ns
tH	Hold Time, HIGH or LOW I <sub>0</sub> or I <sub>1</sub> to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
tPHZ tPLZ	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	ns
tPZH tPZL	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	ns
tw	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	ns

2619 tbl 07

Symbol	Parameter	Condition <sup>(1)</sup>	FCT520CT/521CT				FCT520DT/521DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPHL tPLH	Propagation Delay CLK to Y <sub>n</sub>	CL = 50pF RL = 500Ω	2.0	6.0	2.0	7.0	2.0	5.2	—	—	ns
tPHL tPLH	Propagation Delay S <sub>0</sub> or S <sub>1</sub> to Y <sub>n</sub>		2.0	6.0	2.0	7.0	2.0	4.8	—	—	ns
tSU	Set-up Time, HIGH or LOW D <sub>n</sub> to CLK		2.5	—	2.8	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW D <sub>n</sub> to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
tSU	Set-up Time, HIGH or LOW I <sub>0</sub> or I <sub>1</sub> to CLK		4.0	—	4.5	—	2.0	—	—	—	ns
tH	Hold Time, HIGH or LOW I <sub>0</sub> or I <sub>1</sub> to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	6.0	1.5	6.0	1.5	4.8	—	—	ns
tPZH tPZL	Output Enable Time		1.5	6.0	1.5	7.0	1.5	4.0	—	—	ns
tw	Clock Pulse Width HIGH or LOW <sup>(3)</sup>		5.5	—	6.0	—	3.0	—	—	—	ns

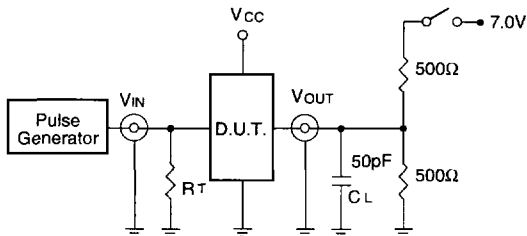
2619 tbl 08

**NOTES:**

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2619 drw 05

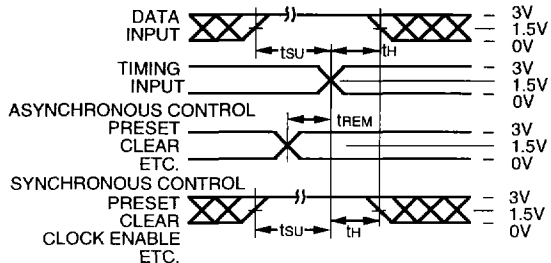
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

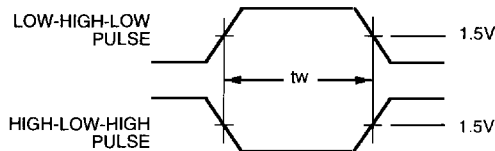
**DEFINITIONS:** 2619 Ink 09  
 C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
 R<sub>T</sub> = Termination resistance: should be equal to Z<sub>out</sub> of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES

PULSE WIDTH



2619 drw 06

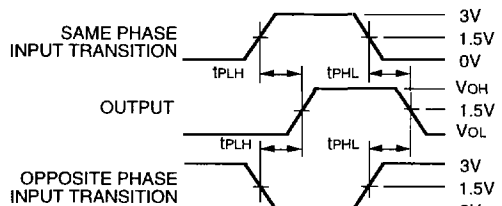


2619 drw 07

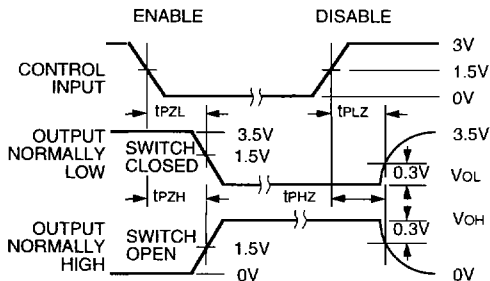


PROPAGATION DELAY

ENABLE AND DISABLE TIMES



2619 drw 08



2619 drw 09

- NOTES:**
- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
  - Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>r</sub> ≤ 2.5ns

**ORDERING INFORMATION**

XX Temperature Range	29FCT X Family	XX Device Type	X Package	X Process	
					Blank B Commercial MIL-STD-883, Class B
					P Plastic DIP
					D CERDIP
					L Leadless Chip Carrier
					SO Small Outline IC
					PY Shrink Small Outline Package
					E CERPACK
					Q Quarter-size Small Outline Package
					520AT Multilevel Pipeline Register
					521AT Multilevel Pipeline Register
					520BT
					521BT
					520CT
					521CT
					520DT
					521DT
					Blank 2 High Drive Balanced Drive
					54 -55°C to +125°C
					74 0°C to +70°C

2619 drw 10