

✓ 54/7496 010745

### 5-BIT SHIFT REGISTER

**DESCRIPTION** — The '96 consists of five RS master/slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the LOW state by applying a low level voltage to the clear input. This condition may be applied independent of the state of the clock input.

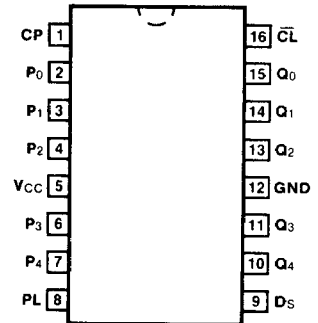
The flip-flops may be independently set to the HIGH state by applying a high level voltage to both the preset input of the specific flip-flop and the common parallel load input. The parallel enable input is provided to allow setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a LOW level to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input must be at a HIGH level and the parallel load input must be at a LOW level for serial shifting.

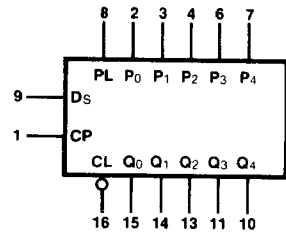
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	7496PC		9B
Ceramic DIP (D)	A	7496DC	5496DM	7B
Flatpak (F)	A	7496FC	5496FM	4L

#### CONNECTION DIAGRAM PINOUT A



#### LOGIC SYMBOL



V<sub>CC</sub> = Pin 5  
GND = Pin 12

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

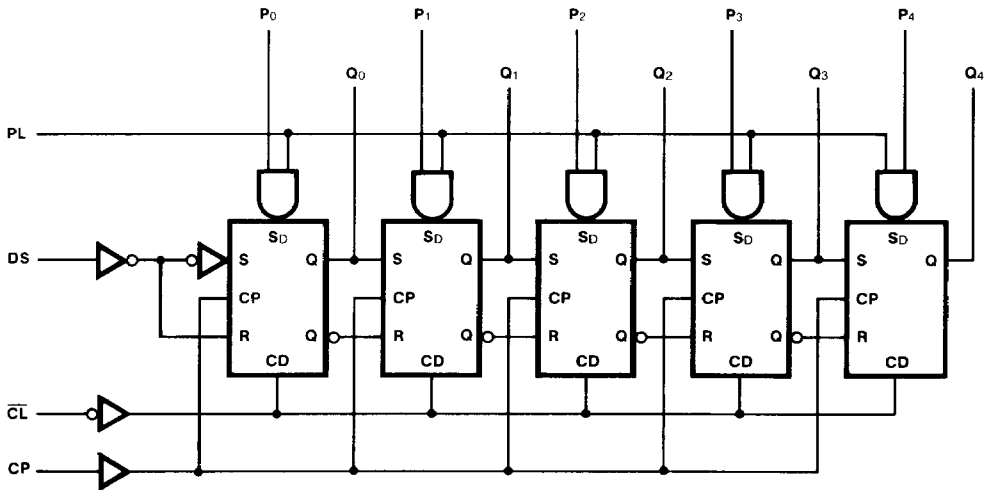
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
CL	Asynchronous Clear Input (Active LOW)	1.0/1.0
DS	Serial Data Input	1.0/1.0
P <sub>0</sub> — P <sub>4</sub>	Parallel Data Inputs	1.0/1.0
PL	Asynchronous Parallel Load Input (Active HIGH)	5.0/5.0
Q <sub>0</sub> — Q <sub>4</sub>	Parallel Outputs	10/10

MODE SELECT TABLE

INPUTS						OPERATION*
PL	P <sub>n</sub>	$\overline{CL}$	D <sub>s</sub>	CP	Q <sub>n</sub>	
L	X	L	X	X	L	Clear; all outputs forced LOW
H	H**	H	X	X	H	Selectively Preset; each output set to its P input
H	L**	H	X	X	L	Shift right; D <sub>s</sub> → Q <sub>0</sub> ; Q <sub>0</sub> → Q <sub>1</sub> , etc.
L	X	H	H, L	$\int$	Q <sub>n-1</sub>	

\*Simultaneous Preset and Clear operations produce undefined states.  
 \*\*To insure proper presetting, P inputs must remain stable while PL is LOW.  
 H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

LOGIC DIAGRAM



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I <sub>CC</sub>	Power Supply Current	XM	68	mA	V <sub>CC</sub> = Max
		XC	79		

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω			
		Min	Max		
f <sub>max</sub>	Maximum Shift Frequency	10		MHz	Figs. 3-1, 3-8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub>		40 40	ns	Figs. 3-1, 3-8
t <sub>PLH</sub>	Propagation Delay, PL or P <sub>n</sub> to Q <sub>n</sub>		35	ns	Figs. 3-1, 3-16
t <sub>PHL</sub>	Propagation Delay, CL to Q <sub>n</sub>		55	ns	Figs. 3-1, 3-16

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C

SYMBOL	PARAMETER	54/54		UNITS	CONDITIONS
		Min	Max		
t <sub>w</sub> (L)	CP Pulse Width LOW	35		ns	Fig. 3-8
t <sub>w</sub> (L)	CL Pulse Width LOW	30		ns	Fig. 3-16
t <sub>w</sub> (H)	PL Pulse Width HIGH	30		ns	Fig. 3-16
t <sub>s</sub> (H)	Setup Time HIGH, D <sub>s</sub> to CP	30		ns	Fig. 3-6
t <sub>h</sub> (H)	Hold Time HIGH, D <sub>s</sub> to CP	0		ns	Fig. 3-6
t <sub>s</sub> (L)	Setup Time LOW, D <sub>s</sub> to CP	30		ns	Fig. 3-6
t <sub>h</sub> (L)	Hold Time LOW, D <sub>s</sub> to CP	0		ns	Fig. 3-6