National Semiconductor

54F/74F164A
Serial-In, Parallel-Out Shift Register

General Description

The 'F164A is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. The 'F164A is a faster version of the 'F164.

Features

■ Typical shift frequency of 90 MHz
■ Asynchronous Master Reset
■ Gated serial data input
■ Fully synchronous data transfers
■ Guaranteed 4000V min ESD protection
■ 'F164A is a faster version of the 'F164

Ordering Code: See Section 11

| Commercial	Military	Package Number	Package Description
74F164APC		N14A	14-Lead (0.300″ Wide) Molded Dual-In-Line
	54F164ADM (Note 2)	J14A	14-Lead Ceramic Dual-In-Line
74F164ASC (Note 1)		M14A	14-Lead (0.150″ Wide) Molded Small Outline, JEDEC
74F164ASJ (Note 1)		M14D	14-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	74F164AFM (Note 2)	W14B	14-Lead Cerpack
	74F164ALM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.
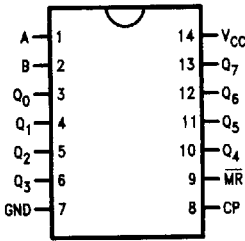
Logic Symbols

TL/F/10613-1

IEEE/IEC
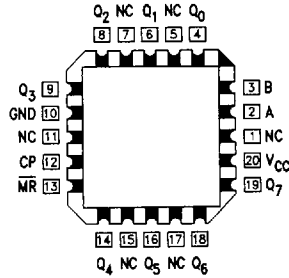

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6501122 0082276 266
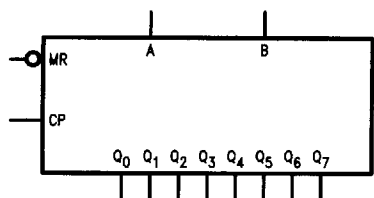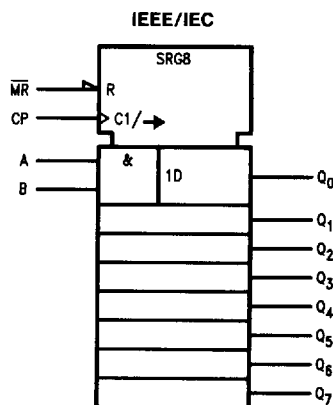
Connection Diagrams

**Pin Assignment for
DIP, SOIC and Flatpak**

```
A  ── 1      14 ── Vcc
B  ── 2      13 ── Q7
Q0 ── 3      12 ── Q6
Q1 ── 4      11 ── Q5
Q2 ── 5      10 ── Q4
Q3 ── 6       9 ── MR
GND── 7       8 ── CP
```

TL/F/10613-2

**Pin Assignment
for LCC**

```
        Q2  NC  Q1  NC  Q0
        8   7   6   5   4

Q3   9                    3  B
GND  10                   2  A
NC   11                   1  NC
CP   12                   20 Vcc
MR   13                   19 Q7

        14  15  16  17  18
        Q4  NC  Q5  NC  Q6
```

TL/F/10613-3

Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A, B	Data Inputs	1.0/1.0	20 μA/−0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
Q_0–Q_7	Outputs	50/33.3	−1 mA/20 mA

Functional Description

The 'F164A is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

Mode Select Table

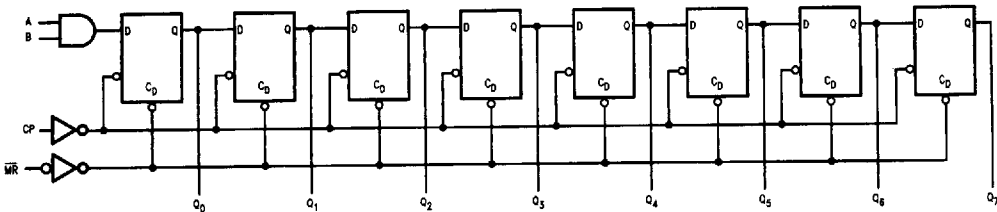| Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	Q_1–Q_7
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q_0–q_6
	H	l	h	L	q_0–q_6
	H	h	l	L	q_0–q_6
	H	h	h	H	q_0–q_6

H(h) = HIGH Voltage Levels
L(l) = LOW Voltage Levels
X = Immaterial
q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram

Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7

TL/F/10613-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$
V_{CC} Pin Potential to Ground Pin	$-0.5V$ to $+7.0V$
Input Voltage (Note 2)	$-0.5V$ to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	
Standard Output	$-0.5V$ to V_{CC}
TRI-STATE® Output	$-0.5V$ to $+5.5V$
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$
Supply Voltage	
Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA
		74F 10% V_{CC}	2.5					$I_{OH} = -1$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	$V_{IN} = 2.7V$
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	$V_{IN} = 7.0V$
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	$V_{OUT} = V_{CC}$
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9$ μA; All other pins grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 150$ mV; All other pins grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CC}	Power Supply Current			35	55	mA	Max	CP = HIGH; $\overline{MR}$ = GND, A, B = GND

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F T_A = +25°C V_CC = +5.0V C_L = 50 pF			54F T_A, V_CC = Mil C_L = 50 pF		74F T_A, V_CC = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	80	120		60		80		MHz	2–1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	3.0 3.5	4.8 5.0	7.5 8.0	2.5 3.0	9.0 8.5	3.0 3.5	7.5 8.0	ns	2–3
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	7.0	10.0	4.0	12.5	5.0	10.5	ns	2–3

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F T_A = +25°C V_CC = +5.0V		54F T_A, V_CC = Mil		74F T_A, V_CC = Com		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A or B to CP	4.5 4.0		5.5 4.0		4.5 4.0		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A or B to CP	1.0 1.0		1.0 1.0		1.0 1.0		ns	
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 7.0		4.0 7.0		4.0 7.0		ns	2–4
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	4.0		5.0		4.0		ns	2–4
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0		6.5		5.0		ns	2–6

7