

## I<sup>2</sup>C to PARALLEL CONVERTER

### ■ GENERAL DESCRIPTION

The **NJU3730** is a serial-to-parallel converter IC, which converts I<sup>2</sup>C serial data into 3 bits parallel data.

The **NJU3730** incorporates selectable three kinds of I<sup>2</sup>C-slave-address, which are used to distinguish one of three **NJU3730**s. Thus, maximum three of the NJU3730 can be connected onto the same I<sup>2</sup>C-bus and each NJU3730 operates as a controller for non-I<sup>2</sup>C device or extensive ports.

The **NJU3730** is suitable for I<sup>2</sup>C-BUS applications such as TV, AV amplifier, mini Stereo component, speaker system and others.

### ■ PACKAGE OUTLINE

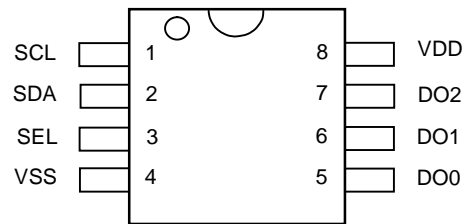


**NJU3730R**

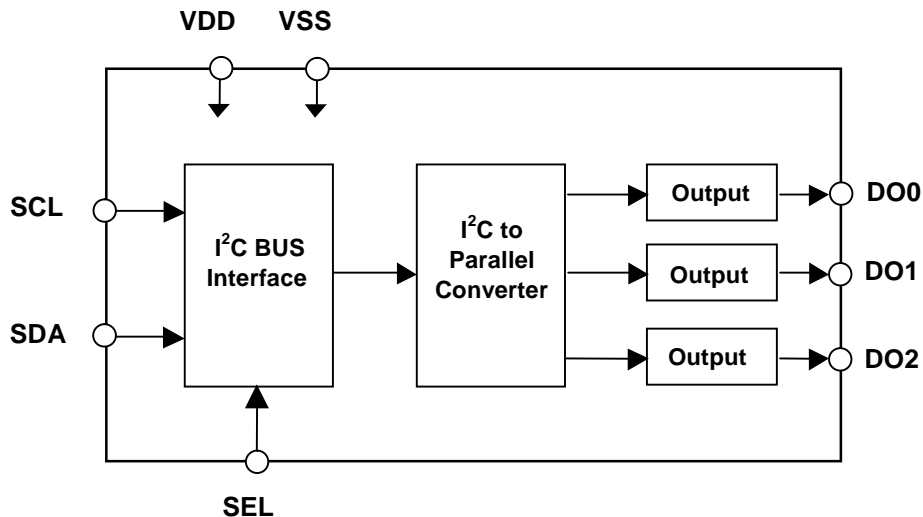
### ■ FEATURES

- Converts I<sup>2</sup>C data to parallel data
- 3 bits parallel output port
- Selectable 3 slave addresses
- Operating Voltage                    2.4 to 5.5V
- C-MOS Technology
- Package Outline                      VSP8

### ■ PIN CONFIGURATION



### ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

NO.	SYMBOL	I/O	FUNCTION
1	SCL	I	I <sup>2</sup> C-bus Serial Clock Input Terminal
2	SDA	I/O	I <sup>2</sup> C-bus Serial Data Input/Output Terminal
3	SEL	I	Slave-address Select Terminal
4	VSS	-	GND: VSS=0V
5	DO0	O	Output Terminal
6	DO1	O	Output Terminal
7	DO2	O	Output Terminal
8	VDD	-	Power Supply: VDD=3V / 5V

## ■ FUNCTIONAL DESCRIPTION

### (1) Data Transmission

NJU3730 is controlled by I<sup>2</sup>C-bus using the SCL and the SDA terminals. NJU3730 is a receive-only slave, and doesn't correspond to the general call address ("0000 0000").

The data transfer is available, when the following timing is executed. When the data transferred exactly, NJU3730 outputs "L" level signal from the SDA terminal as acknowledge signal just after each 8 bits.

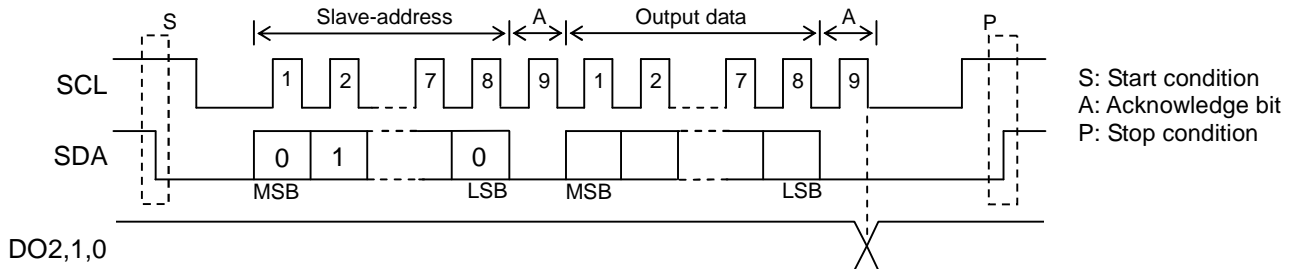


Fig.1 Data Transfer Timing

#### (1-1) Start Condition

A falling edge of the SDA terminal while the SCL terminal is "H" level is defined as the Start condition. After the Start condition, NJU3730 starts reading the data.

#### (1-2) Slave-address

The first byte defines the slave-address. When NJU3730 acknowledges a coincidence its own address with the address information, it outputs the Acknowledge at 9<sup>th</sup> bit timing.

#### (1-3) Output Data

The second byte defines the output data. NJU3730 outputs the Acknowledge at 9<sup>th</sup> bit timing.

#### (1-4) Stop Condition

A rising edge of the SDA terminal while the SCL terminal is "H" level is defined as the Stop condition. After the Stop condition, NJU3730 finishes reading the data.

### (2) Slave-address

The slave-address is selected by the condition of the SEL terminal.

SEL	Slave-address
Low Level	0100 0000
Open	0100 0010
High Level	0100 0100

### (3) Output Terminal (DO0-2) Settings

Output level of the DO0 to DO2 terminals is selected by the condition of the LSB 3 bits of the output data.

DO2	DO1	DO0	Output Data	Initial Value
L	L	L	XXXX X000	✓
L	L	H	XXXX X001	
L	H	L	XXXX X010	
L	H	H	XXXX X011	
H	L	L	XXXX X100	
H	L	H	XXXX X101	
H	H	L	XXXX X110	
H	H	H	XXXX X111	

## ■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V <sub>DD</sub>	-0.3 to +7.0	V
Input Voltage	V <sub>I</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Power Dissipation	P <sub>D</sub>	320 (VSP)	mW
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-40 to +125	°C

Note 1) All voltage values are specified as VSS=0V.

Note 2) If the LSI is used on condition beyond the absolute maximum rating, the LSI may be destroyed. Using LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electrical characteristics conditions will cause malfunction and poor reliability.

Note 3) Decoupling capacitors should be connected between VDD-VSS due to the stabilized operation.

## ■ ELECTRICAL CHARACTERISTICS

### ● DC Characteristics

(Ta=25°C, V<sub>DD</sub>=2.4 to 3.6V, V<sub>SS</sub>=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V <sub>DD</sub>		2.4	-	3.6	V
Operating Current	I <sub>DD</sub>	V <sub>DD</sub> =3.0V No signal, without pull up resistor	-	150	200	μA
Low level Input Voltage	V <sub>IL</sub>		0	-	0.2V <sub>DD</sub>	V
High level Input Voltage	V <sub>IH</sub>		0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V
Low level Output Voltage	V <sub>OL</sub>	V <sub>DD</sub> =3.0V, I <sub>OL</sub> =1mA	0	-	0.6	V
High level Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> =3.0V, I <sub>OH</sub> =-1mA	V <sub>DD</sub> -0.4	-	V <sub>DD</sub>	V
Input Leakage Current	I <sub>LI</sub>	V <sub>I</sub> =V <sub>DD</sub> or V <sub>SS</sub>	-1		1	μA

### ● DC Characteristics

(Ta=25°C, V<sub>DD</sub>=4.5 to 5.5V, V<sub>SS</sub>=0.0V, unless otherwise noted)

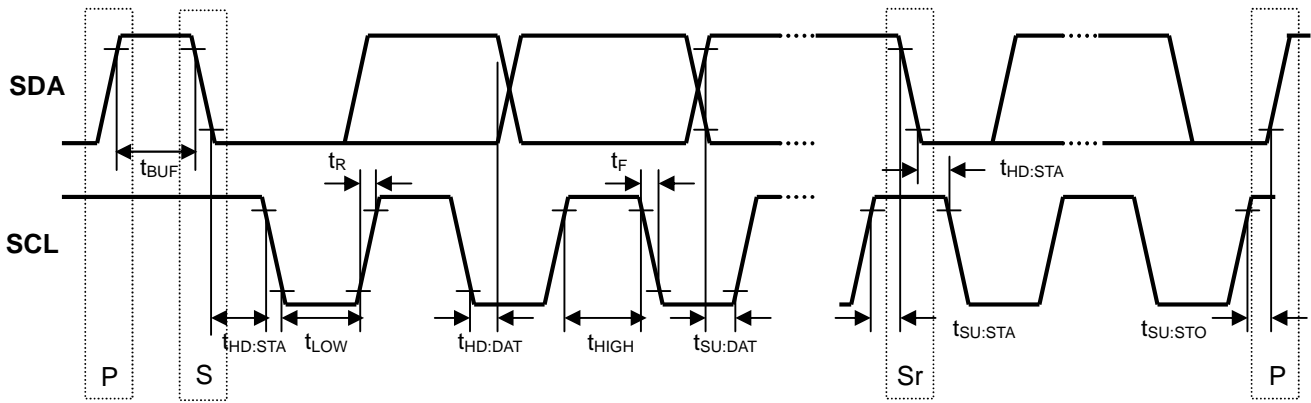
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V <sub>DD</sub>		4.5	-	5.5	V
Operating Current	I <sub>DD</sub>	V <sub>DD</sub> =5.0V No signal, without pull up resistor	-	250	300	μA
Low level Input Voltage	V <sub>IL</sub>		0	-	0.2V <sub>DD</sub>	V
High level Input Voltage	V <sub>IH</sub>		0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V
Low level Output Voltage	V <sub>OL</sub>	V <sub>DD</sub> =5.0V, I <sub>OL</sub> =1mA	0	-	0.4	V
High level Output Voltage	V <sub>OH</sub>	V <sub>DD</sub> =5.0V, I <sub>OH</sub> =-1mA	V <sub>DD</sub> -0.4	-	V <sub>DD</sub>	V
Input Leakage Current	I <sub>LI</sub>	V <sub>I</sub> =V <sub>DD</sub> or V <sub>SS</sub>	-1		1	μA

● AC Characteristics

(Ta=25°C, V<sub>DD</sub>=2.4 to 5.5V, V<sub>SS</sub>=0.0V, unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum Clock Frequency	f <sub>SCL</sub>	-	-	100	kHz
Data Change Minimum Waiting Time	t <sub>BUF</sub>	4.7	-	-	μs
Data Transfer Start Minimum Waiting Time	t <sub>HD:STA</sub>	4.0	-	-	μs
Low Level Clock Pulse Width	t <sub>LOW</sub>	4.7	-	-	μs
High Level Clock Pulse Width	t <sub>HIGH</sub>	4.0	-	-	μs
Minimum Start Preparation Waiting Time	t <sub>SU:STA</sub>	4.7	-	-	μs
Minimum Data Hold Time	t <sub>HD:DAT</sub>	5.0	-	-	μs
Minimum Data Preparation Time	t <sub>SU:DAT</sub>	250	-	-	ns
Rise Time	t <sub>R</sub>	-	-	1.0	μs
Fall Time	t <sub>F</sub>	-	-	300	ns
Minimum Stop Preparation Waiting Time	t <sub>SU:STO</sub>	4.0	-	-	μs

Note 4) I<sup>2</sup>C-bus Load Condition: Pull up resistance 4kΩ (Connected to +5V),  
Load capacitance 200pF (Connected to GND).

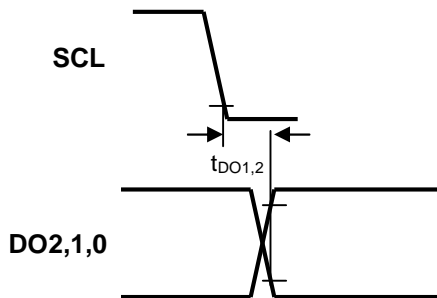


● OUTPUT DELAY TIME

(Ta=25°C, V<sub>SS</sub>=0.0V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Output Delay Time 1 (V <sub>DD</sub> =3.0V)	t <sub>DO1</sub>	-	-	200	ns
Output Delay Time 2 (V <sub>DD</sub> =5.0V)	t <sub>DO2</sub>	-	-	100	ns

Note 5) DOx terminal, C<sub>L</sub>=50pF

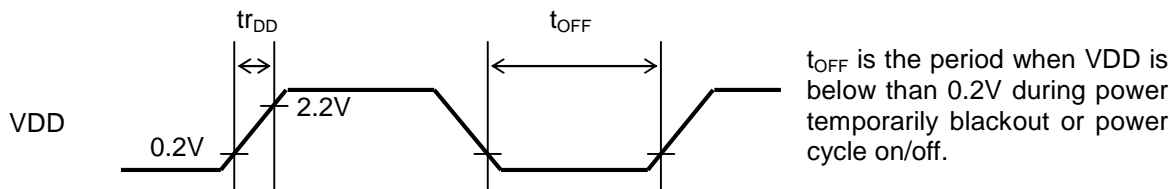


• Power Supply Startup

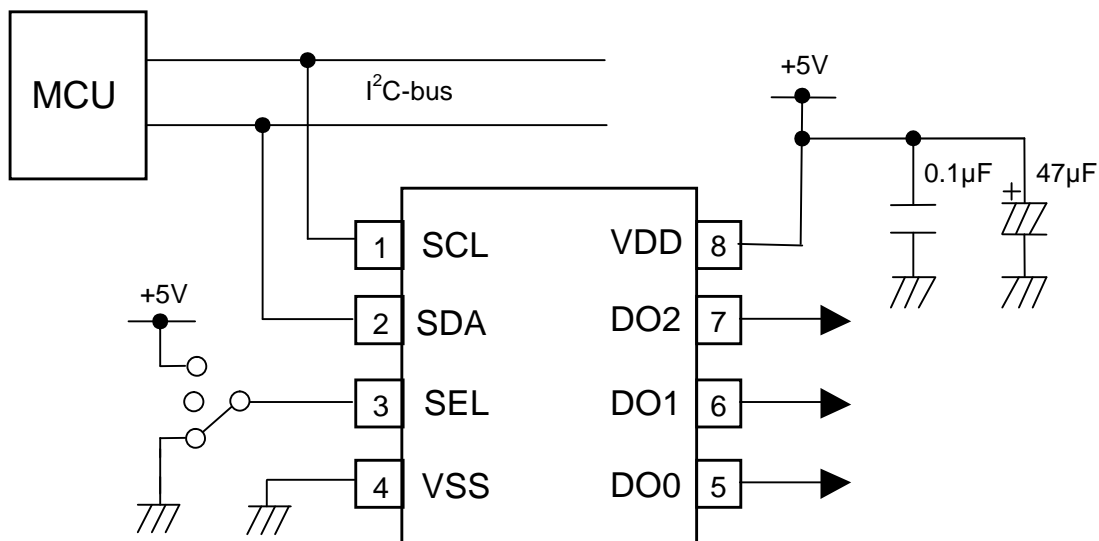
( $T_a=25^\circ\text{C}$ ,  $V_{DD}=2.4$  to  $5.5\text{V}$ ,  $V_{SS}=0.0\text{V}$ , unless otherwise noted)

Parameter	SYMBOL	MIN.	TYP.	MAX.	UNIT
Startup time of power supply	$t_{r_{DD}}$	0.1	-	5	ms
Time for Power supply off	$t_{OFF}$	1	-	-	ms

If the above conditions cannot be met, the internal reset circuit will malfunction.



■ APPLICATION CIRCUIT



[CAUTION]  
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