AK4160

16-channel Capacitive Touch Sensor IC

GENERAL DESCRIPTION

The AK4160 is a low operating voltage and low power consumption 16-channel capacitive touch sensor. Maximum 8 channels out of the 16-channel can be configured to LED drive or GPIO. The AK4160 has a channel independent automatic correct function of environmental drifts for each sense input. It reduces false detection by continuous calibration of the internal reference value in the situation when the input capacitance of the touch switch is changed by the external factors such as hydrothermal conditions. The automatic initial setting function sets the charge current and charge time according to the size and the shape of a touch switch. The AK4160 can be configured via serial interfaces, it is suitable for mobile phones, PCs and home electric applications.

FEATURE

- **Up to 16 capacitive sensor inputs**
- **Up to 8 general purpose inputs/outputs with PWM control for LED**
- **Automatic initial setting function for the charge current and time**
- **Independent automatic environmental drifts correct function for each sense terminal**
- **Independent threshold configuration for each sense terminal**
- **Selectable multi touch feature**
- **Integrated Median Averaging Filter**
- **Selectable 3 interrupt outputs that be able to use as GPIOs**
- **Reset Input pin**
- **I^2C Serial Interface**
- **10 bit SAR A/D Converter with S/H circuit**
- **Integrated Regulator**
- **Low Power Consumption: Typ. 3.4uA**
  (Sampling rate=512ms, 16ch Sensor input Active)
- **Power Down Current: Typ. 1.0uA**
- **Low Power Operation: VDD = 1.71V ~ 3.6V**
- **Operating Temperature: Ta = -40 ~ 85 °C**
- **Package: 28pin QFN (4.0mm x 4.0mm, pitch 0.4mm)**

I^2C-bus is a trademark of NXP B.V.

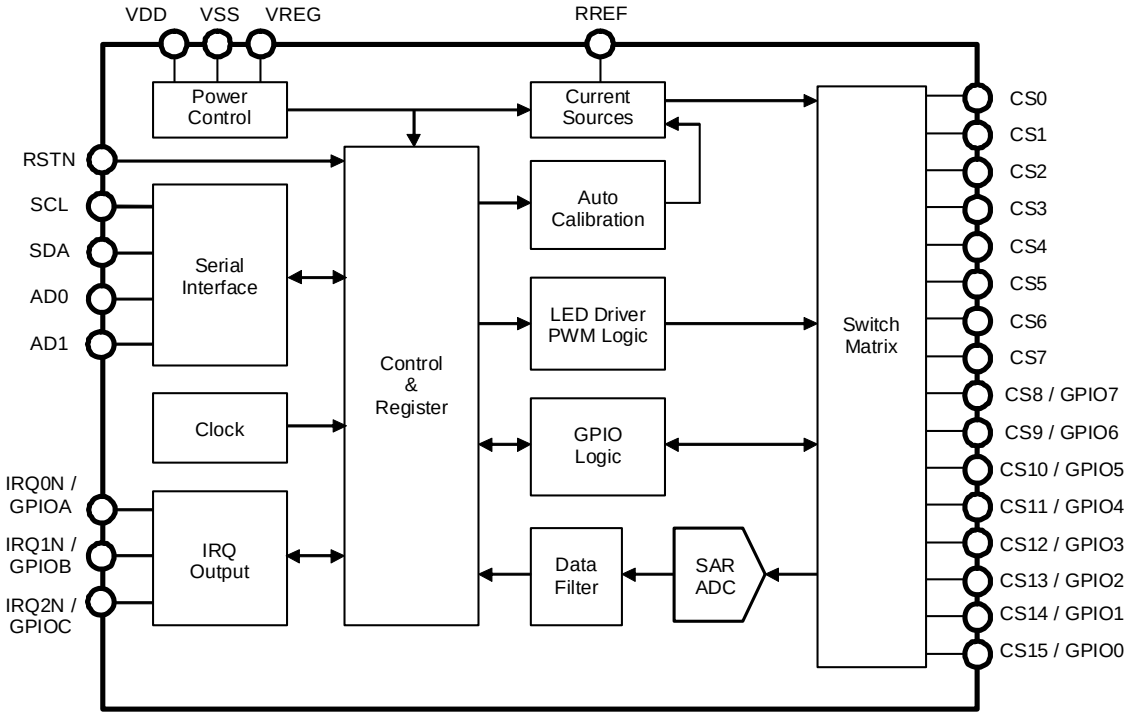
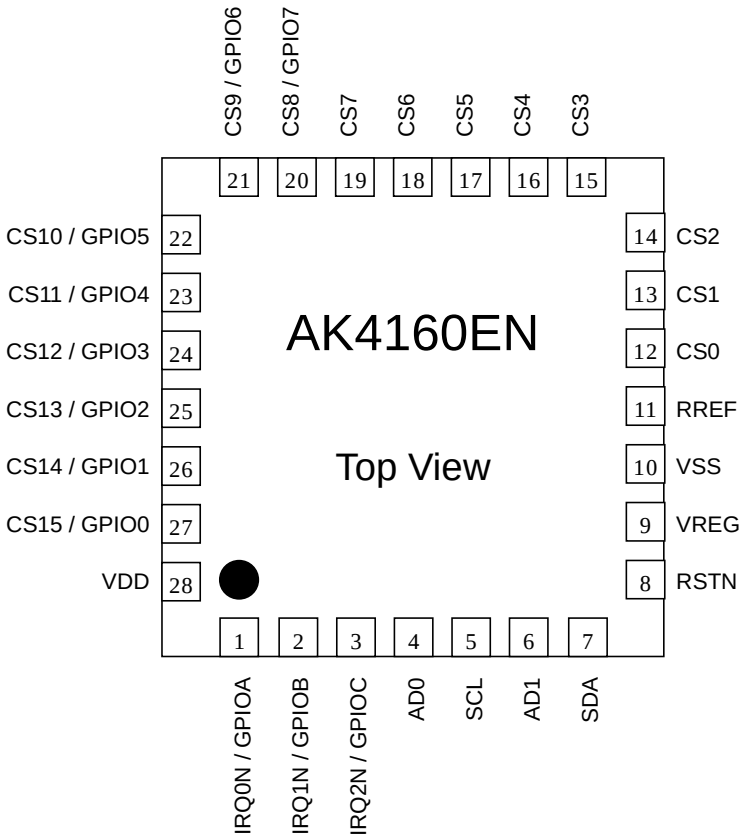


Figure 1. Block Diagram

■ Ordering Guide

AK4160EN	–40 ~ +85°C	28pin QFN (4mm x 4mm, 0.4mm pitch)
AKD4160	AK4160EN Evaluation Board	

■ Pin Layout


CS9 / GPIO6
CS8 / GPIO7
CS7
CS6
CS5
CS4
CS3
21
20
19
18
17
16
15
CS10 / GPIO5 22
CS11 / GPIO4 23
CS12 / GPIO3 24
CS13 / GPIO2 25
CS14 / GPIO1 26
CS15 / GPIO0 27
VDD 28
14 CS2
13 CS1
12 CS0
11 RREF
10 VSS
9 VREG
8 RSTN
AK4160EN
Top View
1
2
3
4
5
6
7
IRQ0N / GPIOA
IRQ1N / GPIOB
IRQ2N / GPIOC
AD0
SCL
AD1
SDA

PIN/FUNCTION

Pin No.	Pin Name	Type (Note 1)	I/O (Note 2)	Function	Reset State RSTN pin = "L"
1	IRQ0N / GPIOA	D	I/O	Interrupt Bit0 / GPIO PinA	Hi-z (Input)
2	IRQ1N / GPIOB	D	I/O	Interrupt Bit1 / GPIO PinB	Hi-z (Input)
3	IRQ2N / GPIOC	D	I/O	Interrupt Bit2 / GPIO PinC	Hi-z (Input)
4	AD0	D	I	I^2C Slave Address Bit 0	-
5	SCL	D	I	I^2C Serial Clock Input	-
6	AD1	D	I	I^2C Slave Address Bit 1	-
7	SDA	D	I/O	I^2C Serial Data Input/ Output	Hi-z (Input)
8	RSTN	D	I	Reset Pin Internal pull-up by 100kΩ (typ)	-
9	VREG	D	O	Internal Regulator Output Current must not be taken from this pin. A 47nF ± 20% capacitor should be connected between this pin and VSS.	Output
10	VSS	GND	-	Ground	-
11	RREF	A	I	Reference Resistor Input A 100kΩ ± 1% resistor should be connected between this pin and VSS.	Hi-z (Open)
12	CS0	A	I/O	Cap Sense Pin0	L
13	CS1	A	I/O	Cap Sense Pin1	L
14	CS2	A	I/O	Cap Sense Pin2	L
15	CS3	A	I/O	Cap Sense Pin3	L
16	CS4	A	I/O	Cap Sense Pin4	L
17	CS5	A	I/O	Cap Sense Pin5	L
18	CS6	A	I/O	Cap Sense Pin6	L
19	CS7	A	I/O	Cap Sense Pin7	Hi-z (Open) (Note 5)
20	CS8 / GPIO7	A/D	I/O	Cap Sense Pin8 / GPIO Pin7	Hi-z (Input)
21	CS9 / GPIO6	A/D	I/O	Cap Sense Pin9 / GPIO Pin6	Hi-z (Input)
22	CS10 / GPIO5	A/D	I/O	Cap Sense Pin10 / GPIO Pin5	Hi-z (Input)
23	CS11 / GPIO4	A/D	I/O	Cap Sense Pin11 / GPIO Pin4	Hi-z (Input)
24	CS12 / GPIO3	A/D	I/O	Cap Sense Pin12 / GPIO Pin3	Hi-z (Input)
25	CS13 / GPIO2	A/D	I/O	Cap Sense Pin13 / GPIO Pin2	Hi-z (Input)
26	CS14 / GPIO1	A/D	I/O	Cap Sense Pin14 / GPIO Pin1	Hi-z (Input)
27	CS15 / GPIO0	A/D	I/O	Cap Sense Pin15 / GPIO Pin0	Hi-z (Input)
28	VDD	PWR	-	Power Supply : 1.71V ~ 3.6V	-

Note 1. A (Analog terminal), D (Digital terminal), GND (Ground), PWR (Power)
Note 2. I (Input terminal), O (Output terminal)
Note 3. All digital input pins (AD0, AD1, SCL, SDA) must not be allowed to float.
Note 4. When GPIO pins (GPIOA ~ GPIOC, GPIO0 ~ GPIO7) are configured to digital inputs without internal pull resistor, the pins must not be left floating.
Note 5. Outputs "L" after releasing a reset.

■ Handling of Unused Pins

The unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Digital	IRQ0N / GPIOA ~ IRQ2N / GPIOC	This pin must be configured with internal pull-up/down resistor or be connected to VSS or VDD.
Analog	CS0 ~ CS7	This pin must be open.
Analog/Digital	CS8 / GPIO7 ~ CS15 / GPIO0	This pin must be configured with internal pull-down resistor or be connected to VSS.

ABSOLUTE MAXIMUM RATINGS

(VSS = 0V (Note 6))

Parameter	Symbol	Min	max	Unit
Power Supply	VDD	-0.3	4.3	V
Input Current Any Pins except for supply	IIN	-	±10	mA
GPIO Source Current per Pin	Isource	-	12	mA
GPIO Sink Current per Pin	Isink	-	1.2	mA
Input Voltage (Note 7)	VIN	-0.3	VDD+0.3 or 4.3	V
Ambient Temperature (power applied)	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 6. All voltages with respect to ground.
Note 7. For all input pins. The maximum value is smaller value between (VDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS = 0V (Note 6))

Parameter	Symbol	min	typ	max	Unit
Power Supply	VDD	1.71	1.8	3.6	V

Note 6. All voltages with respect to ground.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta = -40°C ~ 85°C, VDD = 1.8V; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
A/D Converter					
Resolution	RESO	-	10	-	Bits
Touch Sensor					
Charge Current Variation Against Nominal Value (Note 8)	ICHG	-5	-	5	%
Power Supply Current					
Measurement Current (All function in active)	IMEAS	-	0.8	1	mA
Idle Current	IIDLE	-	3	11	uA
Average Supply Current	IDD				
TSR= 4ms, NCH=16, TCHG=2us, NF1S=4		-	54	-	uA
TSR= 8ms, NCH=16, TCHG=2us, NF1S=4		-	29	-	uA
TSR= 16ms, NCH=16, TCHG=2us, NF1S=4		-	16	-	uA
TSR= 32ms, NCH=16, TCHG=2us, NF1S=4		-	9	-	uA
TSR= 64ms, NCH=16, TCHG=2us, NF1S=4		-	6	-	uA
TSR=128ms, NCH=16, TCHG=2us, NF1S=4		-	5	-	uA
TSR=256ms, NCH=16, TCHG=2us, NF1S=4		-	4	-	uA
TSR=512ms, NCH=16, TCHG=2us, NF1S=4		-	3.4	-	uA
Shutdown Current NCH=0 (Shutdown Mode)	ISHUT	-	1	9	uA

Note 8. Sense terminal voltage condition: The AD conversion value should be less or equal to VDD-0.2[V].
The charge current is dependent on the operating voltage, and is configured with registers in "0.556 x VDD [uA]" to "35.028 x VDD [uA]" range.

DC CHARACTERISTICS (Logic I/O)

(Ta = -40°C ~ 85°C, VDD = 1.71V ~ 3.6V; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Input Leakage Current (Note 9) (Note 10)	IILH	-1.0	-	1.0	uA
Input High Voltage	VIH	0.7xVDD	-	-	V
Input Low Voltage	VIL	-	-	0.3xVDD	V
Output High Voltage (Note 11) (Note 14) Io=-10mA	VOHF1	VDD-0.5	-	-	V
Output High Voltage (Note 11) (Note 15) Io=-3.3mA	VOH1	VDD-0.5	-	-	V
Output Low Voltage (Note 11) (Note 14) Io=1mA	VOLF1	-	-	0.5	V
Output Low Voltage (Note 11) (Note 15) Io=0.33mA	VOL1	-	-	0.5	V
Output High Voltage (Note 12) (Note 14) Io=-6mA	VOHF2	VDD-0.5	-	-	V
Output High Voltage (Note 12) (Note 15) Io=-2mA	VOH2	VDD-0.5	-	-	V
Output Low Voltage (Note 12) (Note 14) Io=6mA	VOLF2	-	-	0.5	V
Output Low Voltage (Note 12) (Note 15) Io=2mA	VOL2	-	-	0.5	V
Output Low Voltage (Note 13) Io=3mA	VOL3	-	-	0.5	V
Pull-up Current (Note 11) (Note 12) (Pull-up Setting)	IPU	5	-	200	uA
Pull-down Current (Note 11) (Note 12) (Pull-down Setting)	IPD	-200	-	-5	uA

Note 9. GPIO0~GPIO7, AD0, AD1, GPIOA~GPIOC, SCL, SDA
Note 10. Except for the RSTN pin. The RSTN pin has an internal pull-up device, normally 100kΩ.
Note 11. GPIO0~GPIO7
Note 12. IRQ0N~IRQ2N
Note 13. SDA
Note 14. Full Drive Operation
Note 15. 1/3 Drive Operation

SWITCHING CHARACTERISTICS

(Ta = -40°C ~ 85°C, VDD = 1.71V ~ 3.6V; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
Touch Sensor					
Charge Time (Note 16)	TCHG	-15	-	15	%
Sampling Rate (Note 17)	TSR	-35	-	35	%
PWM					
Frequency Accuracy	ACCF	-35	-	35	%
Reset Timing					
Reset Pulse Width (Note 18)	tRSTN	10	-	-	us
Reset Pin Pulse Width of Spike Noise Suppressed by Input Filter (Note 19)	tRSTNS	0.5	-	-	us
Start Up Timing					
Power up time (Note 20)	tPU	-	-	1	ms
Power up rise time	tPR	-	-	20	ms
Power up Interval time (Note 21)	tPI	20	-	-	ms
I^2C					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 22)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	50	-	-	ns
Capacitive load on bus	Cb	-	-	400	pF

Note 16. Variation against nominal value of TCHG (0.25us to 32us)
Note 17. Variation against nominal value of TSR (4ms to 512ms)
Note 18. The AK4160 can be reset by the RSTN pin = "L". This is to initialize the AK4160 for sure.
Note 19. Pulse width of spike noise suppressed by input filter of the RSTN pin.
Note 20. Time as the starting point when reached VDD=1.71V and VREG=1.0V, with CREG=47nF.
Note 21. The condition of "VDD=VSS" should be kept during the Power up Interval Time.
Note 22. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

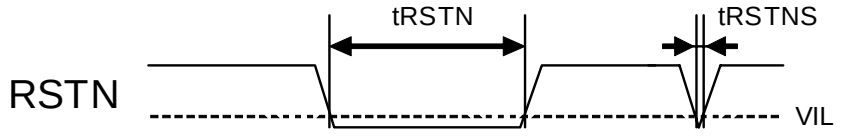


Figure 2. Reset Timing Diagram

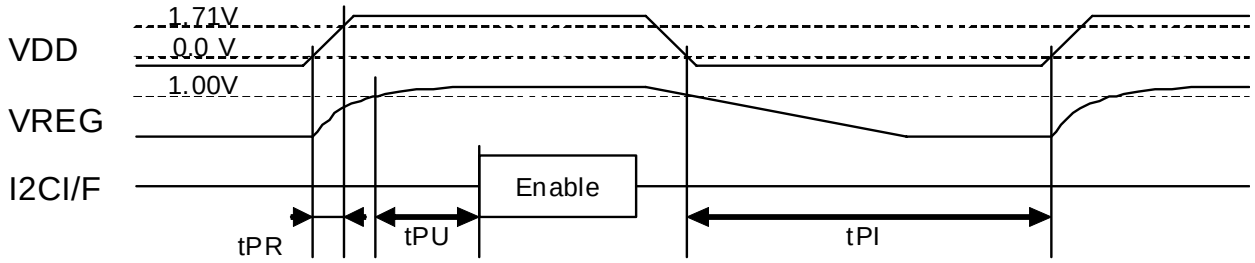


Figure 3. Power up Timing Diagram

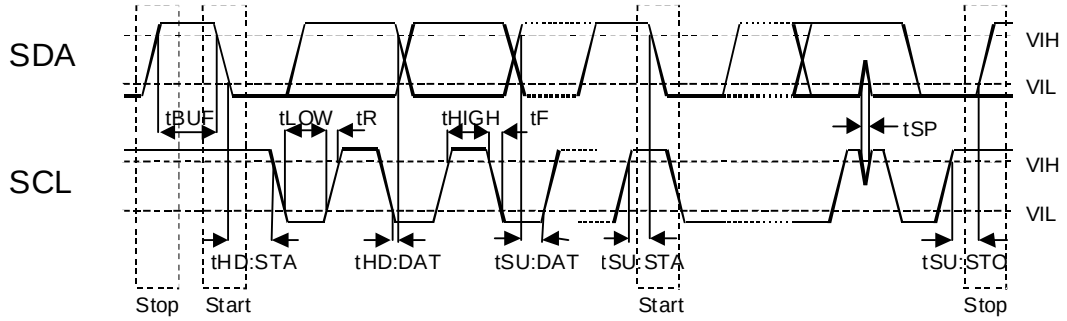


Figure 4. I^2C Interface Timing Diagram

OPERATION OVERVIEW

■ Operation of Touch Sensor

The touch switch (capacitor) that is connected to the sense input is charged up with direct current during a given period of time. The switch is connected to ground before the measurement. As a result, the touch switch capacitance is completely discharged before start being charged. When the touch switch is fully charged, the voltage is inversely proportional to the capacitance. When the touch switch is touched, this charge voltage decreases because the capacitance value when the switch is touched is larger than when not touched. The charged voltage is converted to a digital data by ADC. The data is get through the noise reduction filter, and compared to a touch threshold value. When the measurement value exceeds the threshold that is corrected environmental drifts, the AK4160 updates the status register to the touch detected state.

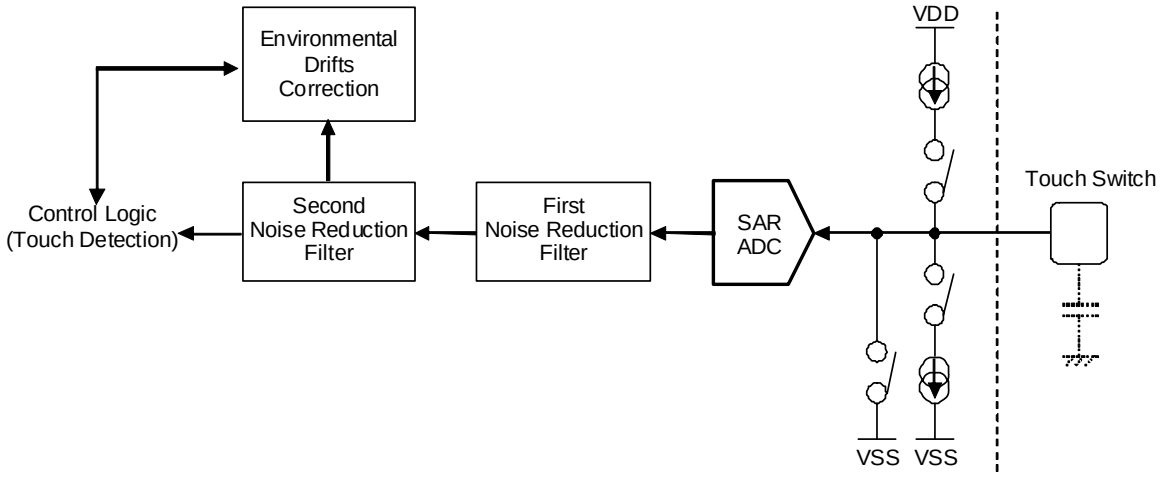


Figure 5. Touch Sensor Block Diagram

■ Capacitance – Voltage Converter

The touch switch (capacitance C), that is connected to the sense terminal, is charged with a direct current I during the period T. The voltage of the sense terminal is V=(I × T)/C, and if the values of I and T are constant, the charged voltage is inversely proportional to the value of capacitance C. The charge voltage is decreased by V=(I × T)/(C+dC) when the capacitance C is increased by dC by touching the touch switch comparing with the not touched status. After the voltage is charged, the AK4160 discharges the sense terminal by a direct current I, during T period. At the same time, the ADC converts the terminal value. The sense terminal must be connected to ground before the next measurement. The next measurement should be started when the sense terminal is discharged completely.

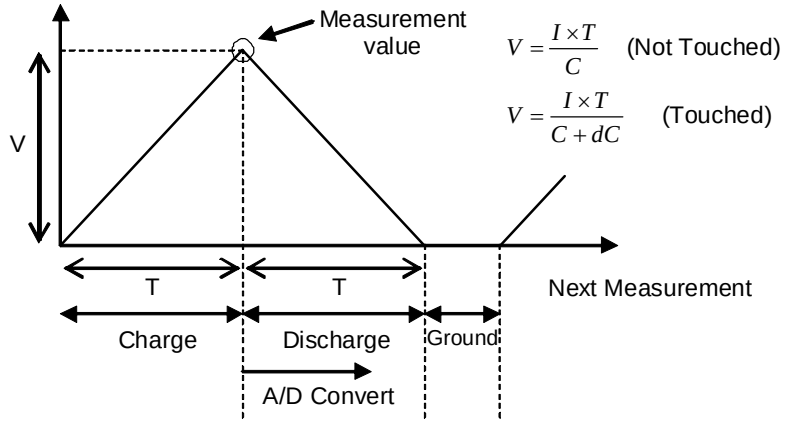


Figure 6. The Voltage Transaction of a Sense Terminal

■ Noise Reduction Filter

The voltage of a sense terminal is measured for N consecutive times. Then the first filter calculates the average value, discarding the minimum and the maximum values. The N of the measurement time is user-selectable from 4, 6, 10, and 18 times. (Address 0x70 NF1S1-0 bits) The sampling rate is dependent on the charge time.

The second filter has the same structure as the first filter. The outputs of the first filter are input to the second filter. The N of the measurement time is user-selectable from 4, 6, 10, and 18 times independent of the first filter. (Address 0x70 NF2S1-0 bits) The sampling rate of the second filter is user-selectable from 4ms to 512ms in factorial of 2 steps. (Address 0x74 TSR2-0 bits)

The output rate of the second filter is "Sampling Rate × Sample Count". The output data is compared to "The Noncontact Reference Value" that output by the calibration circuit for environment changes.

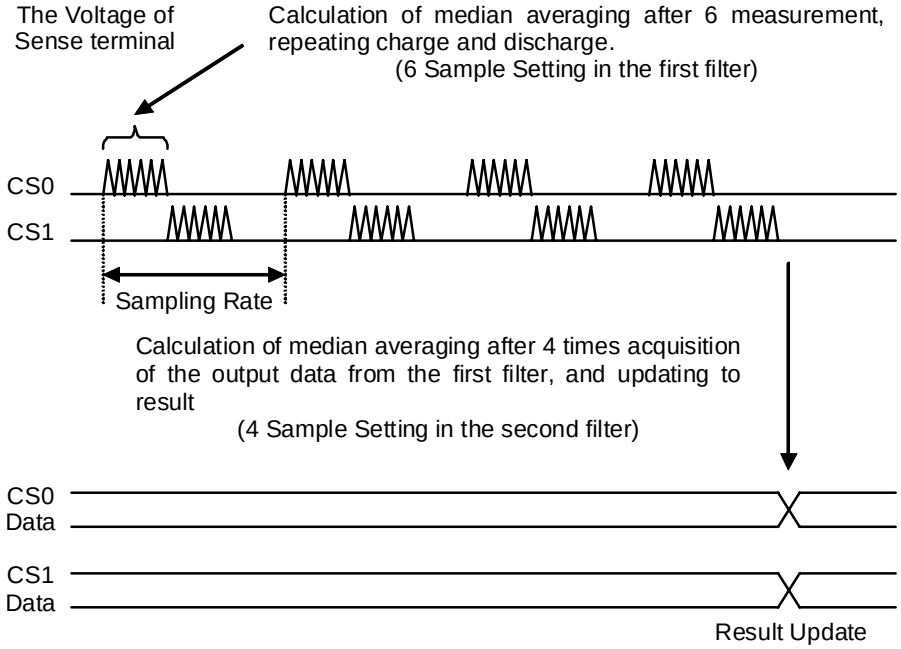


Figure 7. The Measurement of a Sense Terminal and The Data Update

■ Correction of Environment Drifts

The Capacitance of a sense terminal is influenced from the hydrothermal condition and the grime of the surface. The AK4160 monitors the measurement value continuously. If the value is changed by the environment, "The Noncontact Reference Value" is corrected. The reference value is charged very slowly following the measurement value of not touched status by the correction circuit. The threshold of touch detection and release detection is synchronized with the reference value. In case of the touch detection, the reference value is not followed to the measurement value.

The increasing rate and the decreasing rate of the reference value can be configured independently. When a finger approaches slowly to the touch switch, the measurement value is decreased gradually. The decreasing rate of the reference value must be configured slower than the increasing rate to avoid false detection.

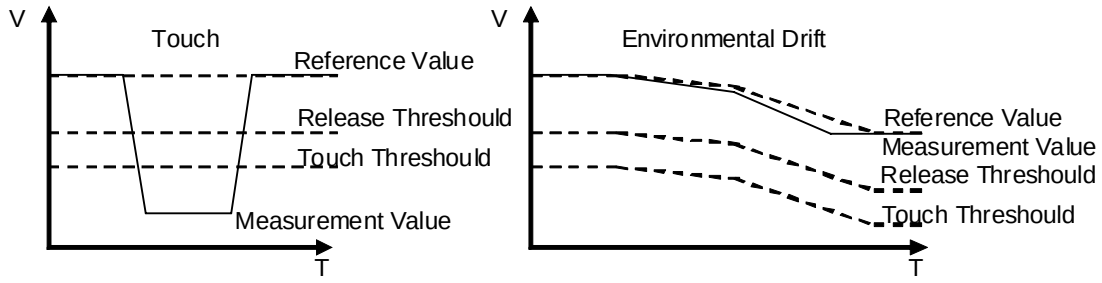


Figure 8. The Voltage of Sense Terminal and Automatic Correction of Environmental Drift

The initial reference value after the reset release can be selected from a user configuration and the automatic configuration that configured to 32/32, 31/32, and 30/32 of the first measurement value. (Address 0x70 RIM1-0 bits)

■ Debounce

The touch status is updated when the output of the second filter is judged as touched or released for N times continuously for a stabilized touch detection. The count "N" is user-selectable from 0 to 15 times. (Address 0x71 DEBT3-0, DEBR3-0 bits) The Update rate of the touch status is calculated as follows. "Sampling Rate of Second Filter x Sample Count of Second Filter x Debounce Count"

■ Automatic Initial Setting

The capacitance of a sensor is different according to the size and the shape of a touch switch. The charge current and the charge period should be configured adequately for optimal sensitivity to every touch switches. (Address 0x45-0x54 CCn5-0 bits, Address 0x55-0x5C CTn2-0 bits) The AK4160 has the automatic initial calibration that configured to the optimal setting. (Address 0x5F ACC)

■ External Reset

The RSTN pin is input terminal for a low-active asynchronous reset with an internal pull-up resistor. A measurement operation is aborted and the internal circuit is initialized immediately by the reset. The serial interface transaction is also aborted. If the reset is executed in a transaction, an unintended access may occur. Therefore, the reset must be executed without transaction of serial interface.

■ Programmable Interrupt

A state change of a sense terminal or GPIO is notified to the host by the IRQ output. The output driver is selectable from open-drain type and totem-pole type, and the activate polarity can be configured. The active condition of the IRQ pins is user-selectable as follows.

1. State Change
2. Touch (State Change from release state to touch state at sense terminals)
3. Release (State Change from touch state to release state at sense terminals)
4. Measurement Execution (any states)
5. Input edge detection of GPIO

Three IRQ pins can be independently configured to different conditions. Several user applications can be supported by the flexible configuration. The unused pin of IRQ pins can simply be configured as a GPIO pin.

■ Multi Touch

The AK4160 supports multi touch operation. The multi touch function can be controlled, improving operability of an application by enabling and disabling.

・Multi Touch Enabled
The status register reflects a touch detection of each sense terminal directly. Update of the status register is independent for each sense terminal. The state of a sense terminal is not influenced by the state of other sense terminals.

・Multi Touch Disabled
Update of the status register is executed singularly. This is for an application that expects a single touch. The user can select a mode shown below.

1. Release ALL
   In this mode, if some sense terminals are touched while all sense terminals are internally released, only the most pushed sense terminal is detected as touched and other touched sense terminal statuses are not updated to touched. (Their statuses remain as released, but internally they are judged as touched.) All sense terminals must be released internally, for a new touch detection in this state.

2. Release CH
   In this mode, if some sense terminals are touched while all sense terminals are internally released, only the most pushed sense terminal is detected as touched and other touched sense terminal statuses are not updated to touched. (Their statuses remain as released, but internally they are judged as touched.) The most pushed sense terminal must be released internally, for a new touch detection in this state. When the most pushed sense terminal is released, the status of second most pushed sense terminal is updated to touched.

This exclusive update (multi touch disabled) can independently be assigned to each sense terminal. However, Release ALL or Release CH mode configuration is common to all sense terminals which are assigned as multi touch disabled.

“The most pushed sense terminal” means a sense terminal which has the biggest difference between measured and reference values. If there was a tie for the biggest difference value, the state of the sense terminal which has the smallest channel number will be changed. By the user setting, “a touched sense terminal with the smallest channel number” can be chosen as the condition of Release CH mode instead of the “the most pushed terminal”.

■ GPIO

8 out of 16 channels can be allocated to GPIO. In or output modes of GPIO is selected by the user.

• Input Mode

1. Connect a pull-up or pull-down resistor.
2. Debounce Function (Update only for continuous inputs of N times)
3. IRQ Interrupt Permitted or Not Permitted
4. IRQ Interrupt Edge Select ("↑" or "↓")

The AK4160 monitors terminal level in every 31.25us by the debounce function. When the input levels are the same for selected number of times continuously, the AK4160 reflects it as an input value.

Setting Value	Continuous Number of Times	Continuous Time (ms)
0	1	-
1	4	0.125
2	8	0.25
3	16	0.5
4	32	1
5	64	2
6	128	4
7	256	8
8	512	16
9	1024	32
10	2048	64
11	4096	128
12	8192	256
13	16384	512
14,15	32768	1024

Table 1. Debounce Function Setting

• Output Mode

1. Selected from CMOS, Open Drain ("H" or "L") outputs
2. Drive Ability Select
3. User setting output or CHn status output from the GPIOn pin.
4. PWM Function

Brightness adjustment of LEDs can be made by PWM function. 125, 250, 500Hz or 1kHz can be configured independently for each GPIO pin. The duty ratio can be set in 32 levels (5bit). When driving LED, High-side output should be selected to decrease influences to the measuring result.

■ Digital I/F

The AK4160 is controlled by a microprocessor via I^{2}C bus supporting standard mode (100kHz) and fast mode (400kHz). Note that the AK4160 operates in those two modes and does not support a High speed mode I^{2}C-bus system (3.4MHz). The AK4160 can operate as a slave device on the I^{2}C bus network. The digital I/O of AK4160 operates off of supply voltage down to 1.71V in order to connect a low voltage microprocessor.

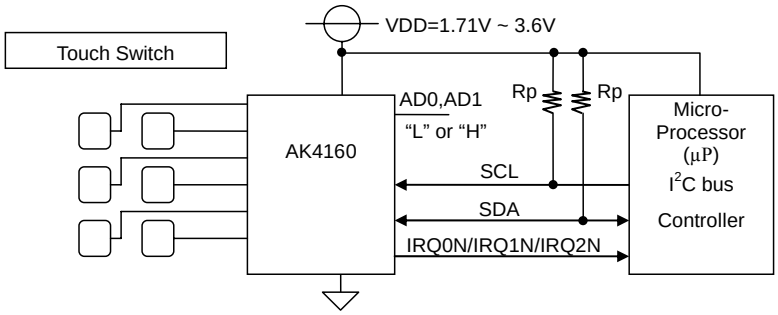


Figure 9. Digital I/F

1. WRITE Operations

Figure 10 shows the data transfer sequence for the I^{2}C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 14). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "10100". The next bits is AD1 and AD0 (device address bit). These bits identify the specific device on the bus. The hard-wired input pin (AD0, AD1 pin) set this device address bit (Figure 11). If the slave address matches that of the AK4160, the AK4160 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 15). R/W bit value of "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4160. The format is MSB first, and those most significant two bits are fixed to zeros (Figure 12). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 13). The AK4160 generates an acknowledge after each byte is received. A data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 14).

The AK4160 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4160 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "9FH" prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 16) except for the START and STOP conditions.

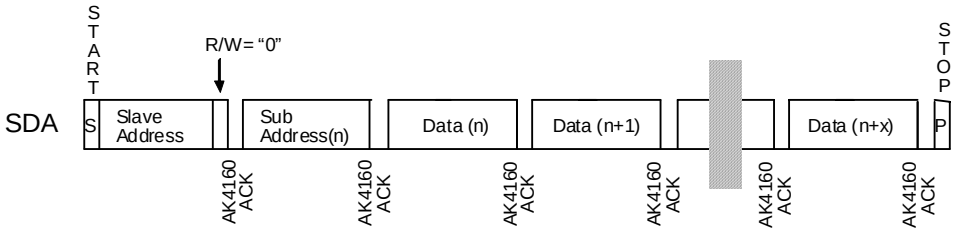


Figure 10. Data Transfer Sequence at the I²C-bus Mode

1	0	1	0	0	AD1	AD0	R/W

(AD0 and AD1 should match with AD0 and AD1 pin.)

Figure 11. The First Byte

A7	A6	A5	A4	A3	A2	A1	A0

Figure 12. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 13. Byte Structure after the second byte

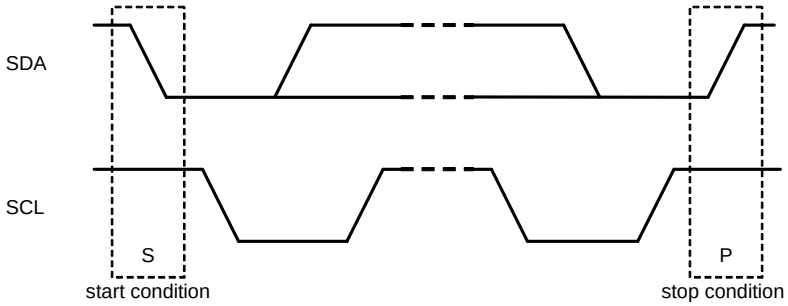


Figure 14. START and STOP Conditions

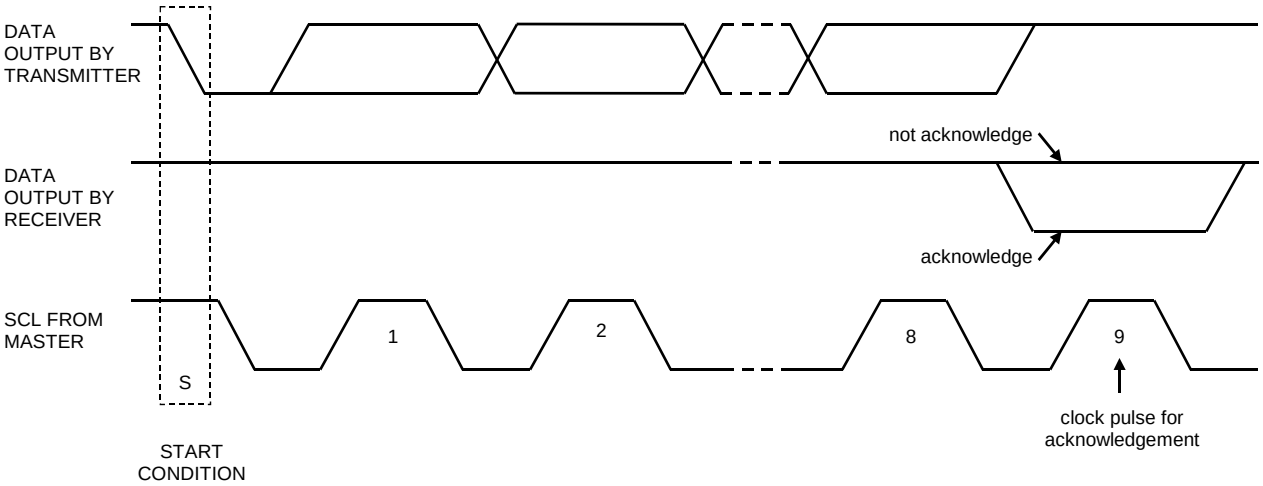


Figure 15. Acknowledge on the I²C-Bus

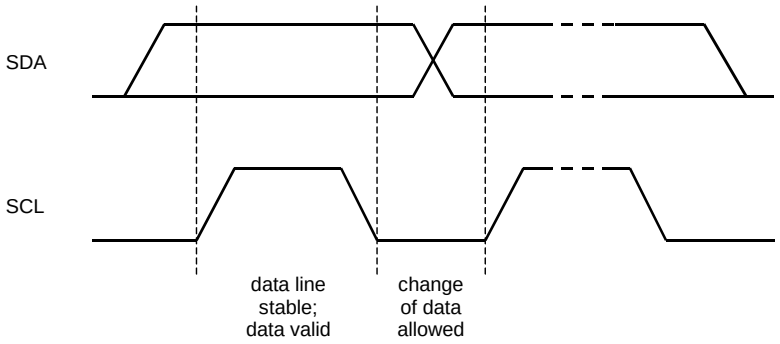


Figure 16. Bit Transfer on the I^2C-Bus

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4160.

After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds "9FH" prior to generating stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out. The register read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4160 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates stop condition instead, the AK4160 ceases transmission.

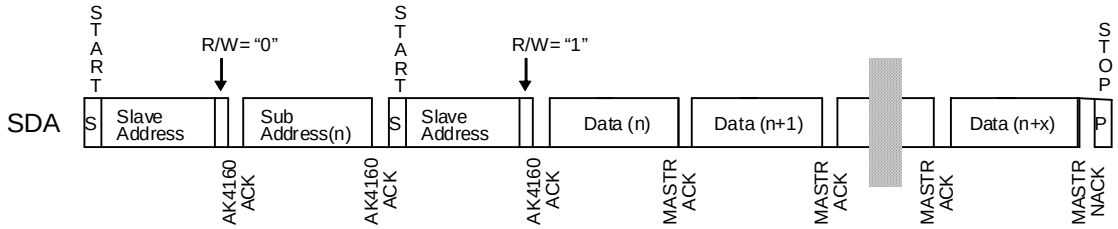


Figure 17. Register Address Read

■ Register Map

Register Address	Description	Type	Symbol	Fields								Initial Value
				D7	D6	D5	D4	D3	D2	D1	D0	
0x00	Touch Status	R	TS	TS[15]	TS[14]	TS[13]	TS[12]	TS[11]	TS[10]	TS[9]	TS[8]	0x00
0x01		R		TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]	0x00
0x02	IRQ Status	R	IRQS	DRDY	TOUCH	REL	ACF	RANGE	GPIN	Reserved	Reserved	0x00
0x03		W/R		IOVER	Reserved	Reserved	Reserved	Reserved	IRQ2	IRQ1	IRQ0	0x00
0x04	GPIO Input Data	R	GPIN	GPIN[7]	GPIN[6]	GPIN[5]	GPIN[4]	GPIN[3]	GPIN[2]	GPIN[1]	GPIN[0]	0x00
0x05	CS0 Data Register	R	CSD0	CSD0[15]	CSD0[14]	CSD0[13]	CSD0[12]	CSD0[11]	CSD0[10]	CSD0[9]	CSD0[8]	0x00
0x06		R		CSD0[7]	CSD0[6]	CSD0[5]	CSD0[4]	CSD0[3]	CSD0[2]	CSD0[1]	CSD0[0]	0x00
0x07	CS1 Data Register	R	CSD1	CSD1[15]	CSD1[14]	CSD1[13]	CSD1[12]	CSD1[11]	CSD1[10]	CSD1[9]	CSD1[8]	0x00
0x08		R		CSD1[7]	CSD1[6]	CSD1[5]	CSD1[4]	CSD1[3]	CSD1[2]	CSD1[1]	CSD1[0]	0x00
0x09	CS2 Data Register	R	CSD2	CSD2[15]	CSD2[14]	CSD2[13]	CSD2[12]	CSD2[11]	CSD2[10]	CSD2[9]	CSD2[8]	0x00
0x0A		R		CSD2[7]	CSD2[6]	CSD2[5]	CSD2[4]	CSD2[3]	CSD2[2]	CSD2[1]	CSD2[0]	0x00
0x0B	CS3 Data Register	R	CSD3	CSD3[15]	CSD3[14]	CSD3[13]	CSD3[12]	CSD3[11]	CSD3[10]	CSD3[9]	CSD3[8]	0x00
0x0C		R		CSD3[7]	CSD3[6]	CSD3[5]	CSD3[4]	CSD3[3]	CSD3[2]	CSD3[1]	CSD3[0]	0x00
0x0D	CS4 Data Register	R	CSD4	CSD4[15]	CSD4[14]	CSD4[13]	CSD4[12]	CSD4[11]	CSD4[10]	CSD4[9]	CSD4[8]	0x00
0x0E		R		CSD4[7]	CSD4[6]	CSD4[5]	CSD4[4]	CSD4[3]	CSD4[2]	CSD4[1]	CSD4[0]	0x00
0x0F	CS5 Data Register	R	CSD5	CSD5[15]	CSD5[14]	CSD5[13]	CSD5[12]	CSD5[11]	CSD5[10]	CSD5[9]	CSD5[8]	0x00
0x10		R		CSD5[7]	CSD5[6]	CSD5[5]	CSD5[4]	CSD5[3]	CSD5[2]	CSD5[1]	CSD5[0]	0x00
0x11	CS6 Data Register	R	CSD6	CSD6[15]	CSD6[14]	CSD6[13]	CSD6[12]	CSD6[11]	CSD6[10]	CSD6[9]	CSD6[8]	0x00
0x12		R		CSD6[7]	CSD6[6]	CSD6[5]	CSD6[4]	CSD6[3]	CSD6[2]	CSD6[1]	CSD6[0]	0x00
0x13	CS7 Data Register	R	CSD7	CSD7[15]	CSD7[14]	CSD7[13]	CSD7[12]	CSD7[11]	CSD7[10]	CSD7[9]	CSD7[8]	0x00
0x14		R		CSD7[7]	CSD7[6]	CSD7[5]	CSD7[4]	CSD7[3]	CSD7[2]	CSD7[1]	CSD7[0]	0x00
0x15	CS8 Data Register	R	CSD8	CSD8[15]	CSD8[14]	CSD8[13]	CSD8[12]	CSD8[11]	CSD8[10]	CSD8[9]	CSD8[8]	0x00
0x16		R		CSD8[7]	CSD8[6]	CSD8[5]	CSD8[4]	CSD8[3]	CSD8[2]	CSD8[1]	CSD8[0]	0x00
0x17	CS9 Data Register	R	CSD9	CSD9[15]	CSD9[14]	CSD9[13]	CSD9[12]	CSD9[11]	CSD9[10]	CSD9[9]	CSD9[8]	0x00
0x18		R		CSD9[7]	CSD9[6]	CSD9[5]	CSD9[4]	CSD9[3]	CSD9[2]	CSD9[1]	CSD9[0]	0x00
0x19	CS10 Data Register	R	CSD10	CSD10[15]	CSD10[14]	CSD10[13]	CSD10[12]	CSD10[11]	CSD10[10]	CSD10[9]	CSD10[8]	0x00
0x1A		R		CSD10[7]	CSD10[6]	CSD10[5]	CSD10[4]	CSD10[3]	CSD10[2]	CSD10[1]	CSD10[0]	0x00
0x1B	CS11 Data Register	R	CSD11	CSD11[15]	CSD11[14]	CSD11[13]	CSD11[12]	CSD11[11]	CSD11[10]	CSD11[9]	CSD11[8]	0x00
0x1C		R		CSD11[7]	CSD11[6]	CSD11[5]	CSD11[4]	CSD11[3]	CSD11[2]	CSD11[1]	CSD11[0]	0x00
0x1D	CS12 Data Register	R	CSD12	CSD12[15]	CSD12[14]	CSD12[13]	CSD12[12]	CSD12[11]	CSD12[10]	CSD12[9]	CSD12[8]	0x00
0x1E		R		CSD12[7]	CSD12[6]	CSD12[5]	CSD12[4]	CSD12[3]	CSD12[2]	CSD12[1]	CSD12[0]	0x00
0x1F	CS13 Data Register	R	CSD13	CSD13[15]	CSD13[14]	CSD13[13]	CSD13[12]	CSD13[11]	CSD13[10]	CSD13[9]	CSD13[8]	0x00
0x20		R		CSD13[7]	CSD13[6]	CSD13[5]	CSD13[4]	CSD13[3]	CSD13[2]	CSD13[1]	CSD13[0]	0x00
0x21	CS14 Data Register	R	CSD14	CSD14[15]	CSD14[14]	CSD14[13]	CSD14[12]	CSD14[11]	CSD14[10]	CSD14[9]	CSD14[8]	0x00
0x22		R		CSD14[7]	CSD14[6]	CSD14[5]	CSD14[4]	CSD14[3]	CSD14[2]	CSD14[1]	CSD14[0]	0x00
0x23	CS15 Data Register	R	CSD15	CSD15[15]	CSD15[14]	CSD15[13]	CSD15[12]	CSD15[11]	CSD15[10]	CSD15[9]	CSD15[8]	0x00
0x24		R		CSD15[7]	CSD15[6]	CSD15[5]	CSD15[4]	CSD15[3]	CSD15[2]	CSD15[1]	CSD15[0]	0x00
0x25	CS0 Touch Threshold	W/R	TT0	T8X0	TT0[6]	TT0[5]	TT0[4]	TT0[3]	TT0[2]	TT0[1]	TT0[0]	0x00
0x26	CS0 Release Threshold	W/R	RT0	R8X0	RT0[6]	RT0[5]	RT0[4]	RT0[3]	RT0[2]	RT0[1]	RT0[0]	0x00
0x27	CS1 Touch Threshold	W/R	TT1	T8X1	TT1[6]	TT1[5]	TT1[4]	TT1[3]	TT1[2]	TT1[1]	TT1[0]	0x00
0x28	CS1 Release Threshold	W/R	RT1	R8X1	RT1[6]	RT1[5]	RT1[4]	RT1[3]	RT1[2]	RT1[1]	RT1[0]	0x00
0x29	CS2 Touch Threshold	W/R	TT2	T8X2	TT2[6]	TT2[5]	TT2[4]	TT2[3]	TT2[2]	TT2[1]	TT2[0]	0x00
0x2A	CS2 Release Threshold	W/R	RT2	R8X2	RT2[6]	RT2[5]	RT2[4]	RT2[3]	RT2[2]	RT2[1]	RT2[0]	0x00
0x2B	CS3 Touch Threshold	W/R	TT3	T8X3	TT3[6]	TT3[5]	TT3[4]	TT3[3]	TT3[2]	TT3[1]	TT3[0]	0x00
0x2C	CS3 Release Threshold	W/R	RT3	R8X3	RT3[6]	RT3[5]	RT3[4]	RT3[3]	RT3[2]	RT3[1]	RT3[0]	0x00
0x2D	CS4 Touch Threshold	W/R	TT4	T8X4	TT4[6]	TT4[5]	TT4[4]	TT4[3]	TT4[2]	TT4[1]	TT4[0]	0x00
0x2E	CS4 Release Threshold	W/R	RT4	R8X4	RT4[6]	RT4[5]	RT4[4]	RT4[3]	RT4[2]	RT4[1]	RT4[0]	0x00
0x2F	CS5 Touch Threshold	W/R	TT5	T8X5	TT5[6]	TT5[5]	TT5[4]	TT5[3]	TT5[2]	TT5[1]	TT5[0]	0x00
0x30	CS5 Release Threshold	W/R	RT5	R8X5	RT5[6]	RT5[5]	RT5[4]	RT5[3]	RT5[2]	RT5[1]	RT5[0]	0x00
0x31	CS6 Touch Threshold	W/R	TT6	T8X6	TT6[6]	TT6[5]	TT6[4]	TT6[3]	TT6[2]	TT6[1]	TT6[0]	0x00
0x32	CS6 Release Threshold	W/R	RT6	R8X6	RT6[6]	RT6[5]	RT6[4]	RT6[3]	RT6[2]	RT6[1]	RT6[0]	0x00
0x33	CS7 Touch Threshold	W/R	TT7	T8X7	TT7[6]	TT7[5]	TT7[4]	TT7[3]	TT7[2]	TT7[1]	TT7[0]	0x00
0x34	CS7 Release Threshold	W/R	RT7	R8X7	RT7[6]	RT7[5]	RT7[4]	RT7[3]	RT7[2]	RT7[1]	RT7[0]	0x00
0x35	CS8 Touch Threshold	W/R	TT8	T8X8	TT8[6]	TT8[5]	TT8[4]	TT8[3]	TT8[2]	TT8[1]	TT8[0]	0x00
0x36	CS8 Release Threshold	W/R	RT8	R8X8	RT8[6]	RT8[5]	RT8[4]	RT8[3]	RT8[2]	RT8[1]	RT8[0]	0x00
0x37	CS9 Touch Threshold	W/R	TT9	T8X9	TT9[6]	TT9[5]	TT9[4]	TT9[3]	TT9[2]	TT9[1]	TT9[0]	0x00
0x38	CS9 Release Threshold	W/R	RT9	R8X9	RT9[6]	RT9[5]	RT9[4]	RT9[3]	RT9[2]	RT9[1]	RT9[0]	0x00
0x39	CS10 Touch Threshold	W/R	TT10	T8X10	TT10[6]	TT10[5]	TT10[4]	TT10[3]	TT10[2]	TT10[1]	TT10[0]	0x00
0x3A	CS10 Release Threshold	W/R	RT10	R8X10	RT10[6]	RT10[5]	RT10[4]	RT10[3]	RT10[2]	RT10[1]	RT10[0]	0x00
0x3B	CS11 Touch Threshold	W/R	TT11	T8X11	TT11[6]	TT11[5]	TT11[4]	TT11[3]	TT11[2]	TT11[1]	TT11[0]	0x00
0x3C	CS11 Release Threshold	W/R	RT11	R8X11	RT11[6]	RT11[5]	RT11[4]	RT11[3]	RT11[2]	RT11[1]	RT11[0]	0x00
0x3D	CS12 Touch Threshold	W/R	TT12	T8X12	TT12[6]	TT12[5]	TT12[4]	TT12[3]	TT12[2]	TT12[1]	TT12[0]	0x00
0x3E	CS12 Release Threshold	W/R	RT12	R8X12	RT12[6]	RT12[5]	RT12[4]	RT12[3]	RT12[2]	RT12[1]	RT12[0]	0x00
0x3F	CS13 Touch Threshold	W/R	TT13	T8X13	TT13[6]	TT13[5]	TT13[4]	TT13[3]	TT13[2]	TT13[1]	TT13[0]	0x00

Table 2. AK4160 Register Map (1)

Register Address	Description	Type	Symbol	Fields								Initial Value
				D7	D6	D5	D4	D3	D2	D1	D0	
0x40	CS13 Release Threshold	W/R	RT13	R8X13	RT13[6]	RT13[5]	RT13[4]	RT13[3]	RT13[2]	RT13[1]	RT13[0]	0x00
0x41	CS14 Touch Threshold	W/R	TT14	T8X14	TT14[6]	TT14[5]	TT14[4]	TT14[3]	TT14[2]	TT14[1]	TT14[0]	0x00
0x42	CS14 Release Threshold	W/R	RT14	R8X14	RT14[6]	RT14[5]	RT14[4]	RT14[3]	RT14[2]	RT14[1]	RT14[0]	0x00
0x43	CS15 Touch Threshold	W/R	TT15	T8X15	TT15[6]	TT15[5]	TT15[4]	TT15[3]	TT15[2]	TT15[1]	TT15[0]	0x00
0x44	CS15 Release Threshold	W/R	RT15	R8X15	RT15[6]	RT15[5]	RT15[4]	RT15[3]	RT15[2]	RT15[1]	RT15[0]	0x00
0x45	CS0 Charge Current	W/R	CC0	Reserved	Reserved	CC0[5]	CC0[4]	CC0[3]	CC0[2]	CC0[1]	CC0[0]	0x00
0x46	CS1 Charge Current	W/R	CC1	Reserved	Reserved	CC1[5]	CC1[4]	CC1[3]	CC1[2]	CC1[1]	CC1[0]	0x00
0x47	CS2 Charge Current	W/R	CC2	Reserved	Reserved	CC2[5]	CC2[4]	CC2[3]	CC2[2]	CC2[1]	CC2[0]	0x00
0x48	CS3 Charge Current	W/R	CC3	Reserved	Reserved	CC3[5]	CC3[4]	CC3[3]	CC3[2]	CC3[1]	CC3[0]	0x00
0x49	CS4 Charge Current	W/R	CC4	Reserved	Reserved	CC4[5]	CC4[4]	CC4[3]	CC4[2]	CC4[1]	CC4[0]	0x00
0x4A	CS5 Charge Current	W/R	CC5	Reserved	Reserved	CC5[5]	CC5[4]	CC5[3]	CC5[2]	CC5[1]	CC5[0]	0x00
0x4B	CS6 Charge Current	W/R	CC6	Reserved	Reserved	CC6[5]	CC6[4]	CC6[3]	CC6[2]	CC6[1]	CC6[0]	0x00
0x4C	CS7 Charge Current	W/R	CC7	Reserved	Reserved	CC7[5]	CC7[4]	CC7[3]	CC7[2]	CC7[1]	CC7[0]	0x00
0x4D	CS8 Charge Current	W/R	CC8	Reserved	Reserved	CC8[5]	CC8[4]	CC8[3]	CC8[2]	CC8[1]	CC8[0]	0x00
0x4E	CS9 Charge Current	W/R	CC9	Reserved	Reserved	CC9[5]	CC9[4]	CC9[3]	CC9[2]	CC9[1]	CC9[0]	0x00
0x4F	CS10 Charge Current	W/R	CC10	Reserved	Reserved	CC10[5]	CC10[4]	CC10[3]	CC10[2]	CC10[1]	CC10[0]	0x00
0x50	CS11 Charge Current	W/R	CC11	Reserved	Reserved	CC11[5]	CC11[4]	CC11[3]	CC11[2]	CC11[1]	CC11[0]	0x00
0x51	CS12 Charge Current	W/R	CC12	Reserved	Reserved	CC12[5]	CC12[4]	CC12[3]	CC12[2]	CC12[1]	CC12[0]	0x00
0x52	CS13 Charge Current	W/R	CC13	Reserved	Reserved	CC13[5]	CC13[4]	CC13[3]	CC13[2]	CC13[1]	CC13[0]	0x00
0x53	CS14 Charge Current	W/R	CC14	Reserved	Reserved	CC14[5]	CC14[4]	CC14[3]	CC14[2]	CC14[1]	CC14[0]	0x00
0x54	CS15 Charge Current	W/R	CC15	Reserved	Reserved	CC15[5]	CC15[4]	CC15[3]	CC15[2]	CC15[1]	CC15[0]	0x00
0x55	CS1/0 Charge Time	W/R	CT0	Reserved	CT1[2]	CT1[1]	CT1[0]	Reserved	CT0[2]	CT0[1]	CT0[0]	0x00
0x56	CS3/2 Charge Time	W/R	CT2	Reserved	CT3[2]	CT3[1]	CT3[0]	Reserved	CT2[2]	CT2[1]	CT2[0]	0x00
0x57	CS5/4 Charge Time	W/R	CT4	Reserved	CT5[2]	CT5[1]	CT5[0]	Reserved	CT4[2]	CT4[1]	CT4[0]	0x00
0x58	CS7/6 Charge Time	W/R	CT6	Reserved	CT7[2]	CT7[1]	CT7[0]	Reserved	CT6[2]	CT6[1]	CT6[0]	0x00
0x59	CS9/8 Charge Time	W/R	CT8	Reserved	CT9[2]	CT9[1]	CT9[0]	Reserved	CT8[2]	CT8[1]	CT8[0]	0x00
0x5A	CS11/10 Charge Time	W/R	CT10	Reserved	CT11[2]	CT11[1]	CT11[0]	Reserved	CT10[2]	CT10[1]	CT10[0]	0x00
0x5B	CS13/12 Charge Time	W/R	CT12	Reserved	CT13[2]	CT13[1]	CT13[0]	Reserved	CT12[2]	CT12[1]	CT12[0]	0x00
0x5C	CS15/14 Charge Time	W/R	CT14	Reserved	CT15[2]	CT15[1]	CT15[0]	Reserved	CT14[2]	CT14[1]	CT14[0]	0x00
0x5D	GPIO Data	W/R	GPDT	GPDT[7]	GPDT[6]	GPDT[5]	GPDT[4]	GPDT[3]	GPDT[2]	GPDT[1]	GPDT[0]	0x00
0x5E	GPIO Enable	W/R	GPEN	GPEN[7]	GPEN[6]	GPEN[5]	GPEN[4]	GPEN[3]	GPEN[2]	GPEN[1]	GPEN[0]	0x00
0x5F	AC Control	W/R	ACC	ACE	RCE	RCIM	CCO	VS[3]	VS[2]	VS[1]	VS[0]	0x06
0x60	AC Status	R	ACS	ACS[15]	ACS[14]	ACS[13]	ACS[12]	ACS[11]	ACS[10]	ACS[9]	ACS[8]	0x00
0x61		R		ACS[7]	ACS[6]	ACS[5]	ACS[4]	ACS[3]	ACS[2]	ACS[1]	ACS[0]	0x00
0x62	Multi Touch Inhibit	W/R	MTI	MTI[15]	MTI[14]	MTI[13]	MTI[12]	MTI[11]	MTI[10]	MTI[9]	MTI[8]	0x00
0x63		W/R		MTI[7]	MTI[6]	MTI[5]	MTI[4]	MTI[3]	MTI[2]	MTI[1]	MTI[0]	0x00
0x64	IRQ Control 0	W/R	IRQC0	GPEN	CLRM	HIGH	DRV[1]	DRV[0]	DSTR	PE	PU	0x08
0x65		W/R		DRDY	TOUCH	REL	ACF	RANGE	GPIN	Reserved	LVL	0x00
0x66	IRQ Mask 0	W/R	IRQM0	IRQM[15]	IRQM[14]	IRQM[13]	IRQM[12]	IRQM[11]	IRQM[10]	IRQM[9]	IRQM[8]	0x00
0x67		W/R		IRQM[7]	IRQM[6]	IRQM[5]	IRQM[4]	IRQM[3]	IRQM[2]	IRQM[1]	IRQM[0]	0x00
0x68	IRQ Control 1	W/R	IRQC1	GPEN	CLRM	HIGH	DRV[1]	DRV[0]	DSTR	PE	PU	0x08
0x69		W/R		DRDY	TOUCH	REL	ACF	RANGE	GPIN	Reserved	LVL	0x00
0x6A	IRQ Mask 1	W/R	IRQM1	IRQM[15]	IRQM[14]	IRQM[13]	IRQM[12]	IRQM[11]	IRQM[10]	IRQM[9]	IRQM[8]	0x00
0x6B		W/R		IRQM[7]	IRQM[6]	IRQM[5]	IRQM[4]	IRQM[3]	IRQM[2]	IRQM[1]	IRQM[0]	0x00
0x6C	IRQ Control 2	W/R	IRQC2	GPEN	CLRM	HIGH	DRV[1]	DRV[0]	DSTR	PE	PU	0x08
0x6D		W/R		DRDY	TOUCH	REL	ACF	RANGE	GPIN	Reserved	LVL	0x00
0x6E	IRQ Mask 2	W/R	IRQM2	IRQM[15]	IRQM[14]	IRQM[13]	IRQM[12]	IRQM[11]	IRQM[10]	IRQM[9]	IRQM[8]	0x00
0x6F		W/R		IRQM[7]	IRQM[6]	IRQM[5]	IRQM[4]	IRQM[3]	IRQM[2]	IRQM[1]	IRQM[0]	0x00
0x70	Noise Filter Control	W/R	NFC	NF2S[1]	NF2S[0]	NF1S[1]	NF1S[0]	RIM[1]	RIM[0]	LCH	RCH	0x00
0x71	Debounce Control	W/R	DEB	DEBT[3]	DEBT[2]	DEBT[1]	DEBT[0]	DEBR[3]	DEBR[2]	DEBR[1]	DEBR[0]	0x00
0x72	EF Control	W/R	EFC	EUP[5]	EUP[4]	EUP[3]	EUP[2]	EUP[1]	EUP[0]	EUR[1]	EUR[0]	0x00
0x73		W/R		EDP[5]	EDP[4]	EDP[3]	EDP[2]	EDP[1]	EDP[0]	EDR[1]	EDR[0]	0x00
0x74	Sampling Rate and Channel Control	W/R	SCC	TSR[2]	TSR[1]	TSR[0]	NCH[4]	NCH[3]	NCH[2]	NCH[1]	NCH[0]	0x00
0x75	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x76	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x77	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x78	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x79	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x7A	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x7B	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x7C	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x7D	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00
0x7E	Soft Reset	W/R	SRST	SRST[7]	SRST[6]	SRST[5]	SRST[4]	SRST[3]	SRST[2]	SRST[1]	SRST[0]	0x00
0x7F	Reserved	-	-	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0x00

Table 3. AK4160 Register Map (2)

Register Address	Description	Type	Symbol	Fields								Initial
				D7	D6	D5	D4	D3	D2	D1	D0	Value
0x80	CS0 Reference Data	W/R	REF0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF0[9]	REF0[8]	0x00
0x81		W/R		REF0[7]	REF0[6]	REF0[5]	REF0[4]	REF0[3]	REF0[2]	REF0[1]	REF0[0]	0x00
0x82	CS1 Reference Data	W/R	REF1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF1[9]	REF1[8]	0x00
0x83		W/R		REF1[7]	REF1[6]	REF1[5]	REF1[4]	REF1[3]	REF1[2]	REF1[1]	REF1[0]	0x00
0x84	CS2 Reference Data	W/R	REF2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF2[9]	REF2[8]	0x00
0x85		W/R		REF2[7]	REF2[6]	REF2[5]	REF2[4]	REF2[3]	REF2[2]	REF2[1]	REF2[0]	0x00
0x86	CS3 Reference Data	W/R	REF3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF3[9]	REF3[8]	0x00
0x87		W/R		REF3[7]	REF3[6]	REF3[5]	REF3[4]	REF3[3]	REF3[2]	REF3[1]	REF3[0]	0x00
0x88	CS4 Reference Data	W/R	REF4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF4[9]	REF4[8]	0x00
0x89		W/R		REF4[7]	REF4[6]	REF4[5]	REF4[4]	REF4[3]	REF4[2]	REF4[1]	REF4[0]	0x00
0x8A	CS5 Reference Data	W/R	REF5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF5[9]	REF5[8]	0x00
0x8B		W/R		REF5[7]	REF5[6]	REF5[5]	REF5[4]	REF5[3]	REF5[2]	REF5[1]	REF5[0]	0x00
0x8C	CS6 Reference Data	W/R	REF6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF6[9]	REF6[8]	0x00
0x8D		W/R		REF6[7]	REF6[6]	REF6[5]	REF6[4]	REF6[3]	REF6[2]	REF6[1]	REF6[0]	0x00
0x8E	CS7 Reference Data	W/R	REF7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF7[9]	REF7[8]	0x00
0x8F		W/R		REF7[7]	REF7[6]	REF7[5]	REF7[4]	REF7[3]	REF7[2]	REF7[1]	REF7[0]	0x00
0x90	CS8 Reference Data	W/R	REF8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF8[9]	REF8[8]	0x00
0x91		W/R		REF8[7]	REF8[6]	REF8[5]	REF8[4]	REF8[3]	REF8[2]	REF8[1]	REF8[0]	0x00
0x92	CS9 Reference Data	W/R	REF9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF9[9]	REF9[8]	0x00
0x93		W/R		REF9[7]	REF9[6]	REF9[5]	REF9[4]	REF9[3]	REF9[2]	REF9[1]	REF9[0]	0x00
0x94	CS10 Reference Data	W/R	REF10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF10[9]	REF10[8]	0x00
0x95		W/R		REF10[7]	REF10[6]	REF10[5]	REF10[4]	REF10[3]	REF10[2]	REF10[1]	REF10[0]	0x00
0x96	CS11 Reference Data	W/R	REF11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF11[9]	REF11[8]	0x00
0x97		W/R		REF11[7]	REF11[6]	REF11[5]	REF11[4]	REF11[3]	REF11[2]	REF11[1]	REF11[0]	0x00
0x98	CS12 Reference Data	W/R	REF12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF12[9]	REF12[8]	0x00
0x99		W/R		REF12[7]	REF12[6]	REF12[5]	REF12[4]	REF12[3]	REF12[2]	REF12[1]	REF12[0]	0x00
0x9A	CS13 Reference Data	W/R	REF13	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF13[9]	REF13[8]	0x00
0x9B		W/R		REF13[7]	REF13[6]	REF13[5]	REF13[4]	REF13[3]	REF13[2]	REF13[1]	REF13[0]	0x00
0x9C	CS14 Reference Data	W/R	REF14	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF14[9]	REF14[8]	0x00
0x9D		W/R		REF14[7]	REF14[6]	REF14[5]	REF14[4]	REF14[3]	REF14[2]	REF14[1]	REF14[0]	0x00
0x9E	CS15 Reference Data	W/R	REF15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REF15[9]	REF15[8]	0x00
0x9F		W/R		REF15[7]	REF15[6]	REF15[5]	REF15[4]	REF15[3]	REF15[2]	REF15[1]	REF15[0]	0x00

Table 4. AK4160 Register Map (3)

■ Register definition

Touch Status Register

Address 0x00 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Touch Status	TS[15]	TS[14]	TS[13]	TS[12]	TS[11]	TS[10]	TS[9]	TS[8]

Address 0x01 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Touch Status	TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]

Bits	Name	Description
15-0	TS	Touch Status for Each Sense Terminal 0: Release 1: Touch

IRQ Status Register

Address 0x02 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ Status	DRDY	TOUCH	REL	ACF	RANGE	GPIN	Reserved	Reserved

Bits	Name	Description
D7	DRDY	Data Ready Interrupt The DRDY bit is set to “1” in the status of data ready. When the data ready interrupt is invalid, this bit is fix to “0”.
D6	TOUCH	Touch Interrupt The TOUCH bit is set to “1” in the status of touch transition. When touch interrupt is invalid, this bit is fix to “0”. The sense terminal connected to the interrupt is selected by IRQM register. (Address 0x66~0x67, 0x6A~0x6B, 0x6E~0x6F)
D5	REL	Release Interrupt The REL bit is set to “1” in the status of release transaction. When release interrupt is invalid, this bit is fix to “0”. The sense terminal connected to the interrupt is selected by IRQM register. (Address 0x66~0x67, 0x6A~0x6B, 0x6E~0x6F)
D4	ACF	Automatic Setting Fail Interrupt The ACF bit is set to “1”, when the measured value of the sense terminal is over the upper limit at the termination of automatic setting. When the automatic setting or the automatic setting fail interrupt is invalid, this bit is fix to “0”.
D3	RANGE	Range Over Interrupt The RANGE bit is set to “1”, when the measured value of the sense terminal is over the upper limit. When the automatic resetting or the range over interrupt is invalid, the bit is fix to “0”.
D2	GPIN	GPIO Input Interrupt The GPIN bit is set to “1” when a GPIO Input Interrupt occurs. When the GPIO input interrupt is invalid, the bit is fix to “0”.
D1-D0	Reserved	Reserved

When the IRQ bit (Addr 0x03 IRQ2-0 bits) with permission of interrupt is cleared, these bits are also cleared.

Address 0x03 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ Status	IOVER	Reserved	Reserved	Reserved	Reserved	IRQ2	IRQ1	IRQ0

Bits	Name	Description
D7	IOVER	Short Detection of the RREF pin The IOVER bit is set to "1", when the RREF pin is shorted to VSS in run mode. The AK4160 is changed from run mode to shutdown mode for the over current protection. The IRQ bit setting to the edge action is fix to the active state. When the IOVER bit is "1", run mode is invalid. When the IOVER bit is written "1", the IOVER bit or IRQ2-0 bits are cleared.
D6-D3	Reserved	Reserved: Must write "0"
D2-D0	IRQ2-0	IRQ Status ・The Edge Action case The IRQ bits are set to "1", when an interrupt occurs. There are 2ways to clear these bits. It is selected by CLRM bit in the IRQCn register. CLRM bit = "0": When the lower byte of the IRQ Status register is read. CLRM bit = "1": When the related bit (IRQ2-0 bits) is written "1", the bit is cleared ・The Level Action case The IRQ bits are set to the input level of IRQN2-0 terminals. Reading or writing "1" to the IRQ bits is invalid. ・The GPIO Function The IRQ bits are set to the level of IRQN2-0 terminals. Reading or writing "1" to the IRQ bits is invalid.

GPIO Input Data Register

Address 0x04 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Input Data	GPIN[7]	GPIN[6]	GPIN[5]	GPIN[4]	GPIN[3]	GPIN[2]	GPIN[1]	GPIN[0]

Bits	Name	Description
D7-D0	GPIN	The level output of GPIO The reading value changes at each setting of GPIO. (Table 5)

GPEN (Note 23)	Direction (Note 24)	Debounce (Note 25)	SRC1-0 bits (Note 26)	The Value that returned from GPIO
0	-	-	-	0
1	Input	Invalid	-	Terminal Level
		Valid	-	Debounced Level
	Output	-	00	Terminal Level
		-	01, 10, 11	Output Enable

Note 23. This is the setting value at the address 0x5E.
Note 24. This is set by DIR bit at the address 0x35~0x44.
Note 25. This is set by DEB1[3:0] bits and DEB0[3:0] bits at address 0x35~0x44.
Note 26. This is set by SRC1-0 bits at address 0x32~0x44.

Table 5. GPIO Register Value

Capacitor Sense Data Register (CSDn: n=0~15)

Address 0x05/0x07/.../0x23 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
CSn Data Register	CSDn[15]	CSDn[14]	CSDn[13]	CSDn[12]	CSDn[11]	CSDn[10]	CSDn[9]	CSDn[8]

Address 0x06/0x08/…/0x24 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
CSn Data Register	CSDn[7]	CSDn[6]	CSDn[5]	CSDn[4]	CSDn[3]	CSDn[2]	CSDn[1]	CSDn[0]

Bits	Name	Description
15-0	CSDn	Measurement Data of each sense terminal The last measurement data is kept when the operating state is changed from run-mode to shutdown-mode. Afterwards, the measurement data is updated in run-mode whenever the data is settled.

CS	Address	CS	Address
CS0	0x05 - 0x06	CS8	0x15 - 0x16
CS1	0x07 - 0x08	CS9	0x17 - 0x18
CS2	0x09 - 0x0A	CS10	0x19 - 0x1A
CS3	0x0B - 0x0C	CS11	0x1B - 0x1C
CS4	0x0D - 0x0E	CS12	0x1D - 0x1E
CS5	0x0F - 0x10	CS13	0x1F - 0x20
CS6	0x11 - 0x12	CS14	0x21 - 0x22
CS7	0x13 - 0x14	CS15	0x23 - 0x24

Table 6. Address to each CS pins

Threshold Register (THn: n=0~15)

Address 0x25/0x27/…/0x43 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
CSn Touch Threshold	T8Xn	TTn[6]	TTn[5]	TTn[4]	TTn[3]	TTn[2]	TTn[1]	TTn[0]

Address 0x26/0x28/…/0x44 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
CSn Release Threshold	R8Xn	RTn[6]	RTn[5]	RTn[4]	RTn[3]	RTn[2]	RTn[1]	RTn[0]

Bits	Name	Description
D7	T8Xn	The touch threshold of the terminal CSn is increased by a factor of eight.
D6-D0	TTn	The touch threshold of the terminal CSn is set. T8Xn=0: The threshold is 0~127 (Step 1) T8Xn=1: The threshold is 0~1016 (Step 8)

Bits	Name	Description
D7	R8Xn	The release threshold of the terminal CSn is increased by a factor of eight.
D6-D0	RTn	The release threshold of the terminal CSn is set. R8Xn=0: The threshold is 0~127 (Step 1) R8Xn=1: The threshold is 0~1016 (Step 8)

The threshold register should not be updated in run-mode.

When the sense terminal is set to GPIO, the threshold register becomes a GPIO control register GPCn (n=0~7).

Address	CS	GPIO
0x25 – 0x26	CS0 Threshold Register	-
0x27 – 0x28	CS1 Threshold Register	-
0x29 – 0x2A	CS2 Threshold Register	-
0x2B – 0x2C	CS3 Threshold Register	-
0x2D – 0x2E	CS4 Threshold Register	-
0x2F – 0x30	CS5 Threshold Register	-
0x31 – 0x32	CS6 Threshold Register	-
0x33 – 0x34	CS7 Threshold Register	-
0x35 – 0x36	CS8 Threshold Register	GPIO7 Control Register
0x37 – 0x38	CS9 Threshold Register	GPIO6 Control Register
0x39 – 0x3A	CS10 Threshold Register	GPIO5 Control Register
0x3B – 0x3C	CS11 Threshold Register	GPIO4 Control Register
0x3D – 0x3E	CS12 Threshold Register	GPIO3 Control Register
0x3F – 0x40	CS13 Threshold Register	GPIO2 Control Register
0x41 – 0x42	CS14 Threshold Register	GPIO1 Control Register
0x43 – 0x44	CS15 Threshold Register	GPIO0 Control Register

Table 7. CS Threshold Register and GPIO Control Register

GPIO Control Register (GPCn: n=0~7)

CS8~CS15 can be used as GPIO by setting GPIO enable register (Addr 0x5E). In this case, the threshold register works as the GPIO control register. The bit allocation of the GPIO control register at the input setting (DIR bit = "0") is different from the allocation at the output setting (DIR bit = "1").

GPIO Input Control Register

Address 0x35/0x37/…/0x43 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Input Control	DIR	Reserved	Reserved	Reserved	IRQC[1]	IRQC[0]	PE	PU

Address 0x36/0x38/…/0x44 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Input Control	DEB1[3]	DEB1[2]	DEB1[1]	DEB1[0]	DEB0[3]	DEB0[2]	DEB0[1]	DEB0[0]

Bits	Name	Description
D7	DIR	This bit should be set to “0” at the input setting of GPIO.
D6-D4	Reserved	Reserved: This bit should be written by “0”, when writing.
D3-D2	IRQC	GPIO Interrupt Setting 00: No Interrupt 01: Interrupt on a rising edge 10: Interrupt on a falling edge 11: Interrupt on both edges
D1	PE	Pull-up, Pull-down Enable 0: Invalid 1: Valid. The direction is fixed by PU bit.
D0	PU	Pull-up / Pull-down Selector 0: Pull-down 1: Pull-up

Bits	Name	Description
D7-D4	DEB1	Debounce Setting at Rising Edge When “1” is detected “2 x 2^{DEB1}” times in a row with 31.25us of the sampling frequency, the result of input is set to “1”. (Table 8) However, when DEB1[3:0] bits = “0”, the result is updated by detecting “1” one time.
D3-D0	DEB0	Debounce Setting at Falling Edge When “1” is detected “2 x 2^{DEB0}” times in a row with 31.25us of the sampling frequency, the result of input is set to “0”. (Table 8) However, when DEB0[3:0] bits = “0”, the result is updated by detecting “1” one time.

DEB0, DEB1	Consecutive number	Consecutive time (ms)	DEB0, DEB1	Consecutive number	Consecutive time (ms)
0000	1	-	1000	512	16
0001	4	0.125	1001	1024	32
0010	8	0.25	1010	2048	64
0011	16	0.5	1011	4096	128
0100	32	1	1100	8192	256
0101	64	2	1101	16384	512
0110	128	4	1110	32768	1024
0111	256	8	1111	32768	1024

Table 8. Debounce Setting

Refer to Table 7 for the correspondence of the register address and the GPIO pin.

GPIO Output Control Register

Address 0x35/0x37/…/0x43 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Output Control	DIR	REL	SRC[1]	SRC[0]	DRV[1]	DRV[0]	INV	DSTR

Address 0x36/0x38/…/0x44 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Output Control	PWM	PRD[1]	PRD[0]	DUTY[4]	DUTY[3]	DUTY[2]	DUTY[1]	DUTY[0]

Bits	Name	Description
D7	DIR	This bit should be set to “1” at the output setting of GPIO.
D6	REL	The Output Setting (SRC1-0 bits = “01”, “10”, “11”) 0: Touch Status 1: Release Status
D5-D4	SRC	The Selection of Output Data 00: The value set by GPDT register (Addr 0x5D) is output. 01: The status value set by REL bit is output. 10: The status value set by REL bit is output in the toggle. (Initial value 0) 11: The status value set by REL bit is output in the toggle. (Initial value 1) When the touch status (release status) is selected as output data, the terminal GPIOn outputs the status of terminal CSn (n=0~7). Touch status is recognized as “0” at shutdown mode. The output value is initialized by writing “0” to corresponding GPDT register (Addr 0x5D) when SRC1-0 bits = “01”, “10”, “11”. 01: The output value is initialized by “0”. 10: The output value is initialized by “0”. 11: The output value is initialized by “1”.
D3-D2	DRV	Output Driver Setting 00: CMOS Output 01: Low Side Output: When Output is “H”, Hi-z (Open Drain) 10: High Side Output: When Output is “L”, Hi-z (Open Drain) 11: CMOS Output (Same as 00 Setting)
D1	INV	The output level is reversed.
D0	DSTR	The Driving ability of the GPIO output driver is set. 0: 1/3 drive 1: full drive

Bits	Name	Description
D7	PWM	PWM Output Enable
D6-D5	PRD	Cycle of the PWM output is set. 00: 125Hz 01: 250Hz 10: 500Hz 11: 1000Hz
D4-D0	DUTY	Duty of the PWM output is set. Duty=(DUTY + 1) / 32: 1/32 ~ 32/32

Refer to Table 7 for the correspondence of the register address and the GPIO pin.

Charge Current Register (CCn: n=0~15)

Address 0x45-0x54 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Charge Current	Reserved	Reserved	CCn[5]	CCn[4]	CCn[3]	CCn[2]	CCn[1]	CCn[0]

Bits	Name	Description
D7-D6	Reserved	Reserved: This bit should be written "0".
D5-D0	CCn	The charge current from the terminal CSn is set. 0.556 x CCn x VDD [uA] When automatic setting is valid (Addr 0x5F ACE bit = "1"), these bits are updated after the setting is completed. This value may not be correct during the automatic setting.

These bits can not be changed by the serial I/F in run-mode.

Charge Time Register (CTn: n=0, 2, 4, 6, 8, 10, 12, 14)

Address 0x55-0x5C (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Charge Time	Reserved	CTn+1[2]	CTn+1[1]	CTn+1[0]	Reserved	CTn[2]	CTn[1]	CTn[0]

Bits	Name	Description
D7,D3	Reserved	Reserved: This bit should be written "0".
D6-D4 D2-D0	CTn+1 CTn	The charge time at the terminal CSn is set. 0.25us~32us = 0.25us x 2^{CTn} When automatic setting is valid (Addr 0x5F ACE bit = "1"), these bits are updated after the setting is completed. This value may not be correct during the automatic setting.

These bits can not be changed by the serial I/F in run-mode.

GPIO Date Register (GPDT)

Address 0x5D (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Data Register	GPDT[7]	GPDT[6]	GPDT[5]	GPDT[4]	GPDT[3]	GPDT[2]	GPDT[1]	GPDT[0]

Bits	Name	Description
D7-D0	GPDT	GPIO Output Data Setting When the touch status is output (SRC1-0 bits = "01", "10", "11"), the output is valid according to GPDT7-0 bits = "1".

GPIO Enable Register (GPEN)

Address 0x5E (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
GPIO Enable Register	GPEN[7]	GPEN[6]	GPEN[5]	GPEN[4]	GPEN[3]	GPEN[2]	GPEN[1]	GPEN[0]

Bits	Name	Description
D7-D0	GPEN	GPIO Enable Exclusive control is provided for the sense terminal select (SCC Register NCH bit). When a pin has already been selected as GPIO, the sense terminal selection is invalid.

Auto Calibration Control Register (ACC)

Address 0x5F (W/R) Default 0x06

Description	D7	D6	D5	D4	D3	D2	D1	D0
Auto Calibration Control	ACE	RCE	RIM	CCO	VS[3]	VS[2]	VS[1]	VS[0]

Bits	Name	Description
D7	ACE	The automatic setting of the charge current and the charge time is enabled. The charge current and the charge time is set automatically at the first measurement, and each register is updated. When the function of automatic setting is valid, the VS3-0 bits must be configured.
D6	RCE	The automatic reconfiguration is enabled. The reconfiguration is operated automatically when the measurement data is over the upper limit.
D5	RIM	Reference value setting of the reconfiguration 0: The first measurement value is set as the initial value of the reference after reconfiguration. 1: 31/32 of the first measurement value is set as the initial value of the reference after reconfiguration.
D4	CCO	Automatic Setting of the Charge Current Only The charge time is not automatically configured, and it is set to the value of CT register. Only charge current is automatically set.
D3-D0	VS	The Lowest Operation Voltage Setting The best charge current and charge time in the power supply voltage selected with these bits are automatically configured. At the power supply voltage selected by these bits, the charge current and the charge time are automatically optimized. The initial value is “0110”. (1.71V ~1.9V)

These bits can not be changed by the serial I/F in run-mode.

VS[3:0]	Lowest Operation Voltage	Upper Limit Voltage of Sense Terminals	Setting Voltage
0000-0101	Reserved	Reserved	Reserved
0110	VDD ≥ 1.71V	1.50V	1.35V
0111	VDD ≥ 1.9V	1.70V	1.53V
1000	VDD ≥ 2.1V	1.90V	1.71V
1001	VDD ≥ 2.3V	2.10V	1.89V
1010	VDD ≥ 2.5V	2.30V	2.07V
1011	VDD ≥ 2.7V	2.50V	2.25V
1100	VDD ≥ 2.9V	2.70V	2.43V
1101	VDD ≥ 3.1V	2.90V	2.61V
1110	VDD ≥ 3.3V	3.10V	2.79V
1111	VDD ≥ 3.5V	3.30V	2.97V

Table 9. Reference Value of Automatic Setting

Auto Calibration Status Register (ACS)

Address 0x60 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Auto Calibration Status	ACS[15]	ACS[14]	ACS[13]	ACS[12]	ACS[11]	ACS[10]	ACS[9]	ACS[8]

Address 0x61 (R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Auto Calibration Status	ACS[7]	ACS[6]	ACS[5]	ACS[4]	ACS[3]	ACS[2]	ACS[1]	ACS[0]

Bits	Name	Description
15-0	ACS	Automatic Setting Status When the automatic setting is failed or the measurement data is over the upper limit, these bits are set. When the reconfiguration is valid (Addr 0x5E RCE bit = "1"), these bits are cleared by the successful reconfiguration.

Multi Touch inhibit Register (MTI)

Address 0x62 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Multi Touch Inhibit	MTI[15]	MTI[14]	MTI[13]	MTI[12]	MTI[11]	MTI[10]	MTI[9]	MTI[8]

Address 0x63 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Multi Touch Inhibit	MTI[7]	MTI[6]	MTI[5]	MTI[4]	MTI[3]	MTI[2]	MTI[1]	MTI[0]

Bits	Name	Description
15-0	MTI	Prohibition of Multi Touch Sense terminals to prohibit the multi touch function are selected by these bits. The operational mode without the multi touch function is controlled by RCH bit and LCH bit of address "0x70".

IRQ Control Register (IRQCn: n=0~2)

These are the control registers of the IRQ pins. When the IRQ pins are used as GPIO, the bit allocation is different.

IRQ Interrupt Register (When GPEN bit = "0")

Address 0x64/0x68/0x6C (W/R) Default 0x08

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ Interrupt	GPEN	CLRM	HIGH	DRV[1]	DRV[0]	DSTR	PE	PU

Address 0x65/0x69/0x6D (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ Interrupt	DRDY	TOUCH	REL	ACF	RANGE	GPIN	Reserved	TSL

Bits	Name	Description
D7	GPEN	GPIO Enable This bit should be set to "0" in the IRQ operation.
D6	CLRM	Clearance Setting of IRQ Status (Addr 0x03 IRQ2-0 bits) 0: Read Clear of IRQ Status 1: Write Clear of IRQ Status (Clear to write "1" to IRQ2-0 bits) IRQ status is cleared in the edge operation. The status is not changed in the level operation.
D5	HIGH	Polarity selection of IRQ pins 0: Active Low 1: Active High] IRQ pins are always non-active in the shutdown mode.
D4-D3	DRV	Output Driver Setting 00: CMOS Output 01: Low Side Output: When Output is "H", Hi-z (Open Drain) 10: High Side Output: When Output is "L", Hi-z (Open Drain) 11: CMOS Output (Same as 00 Setting)
D2	DSTR	The Driving ability of the GPIO output driver is set. 0: 1/3 drive 1: full drive
D1	PE	Pull-up, Pull-down Enable 0: Invalid 1: Valid. The direction is fixed by PU bit.
D0	PU	Pull-up / Pull-down Selector 0: Pull-down 1: Pull-up

Bits	Name	Description
D7	DRDY	Permission of Data Ready Interrupt This interrupt is generated at the end of a measurement. The measurement value should be read from CSDn register (Addr 0x05-0x24). The interrupt interval is "Sampling Rate x Number of Sample". The "Number of Sample" is set by NF2S bits in Addr 0x70.
D6	TOUCH	Permission of Touch Interrupt The intended terminal can be configured by IRQ mask register (Addr 0x66-0x67, 0x6A-0x6B, 0x6E-0x6F).
D5	REL	Permission of Release Interrupt The intended terminal can be configured by IRQ mask register (Addr 0x66-0x67, 0x6A-0x6B, 0x6E-0x6F).
D4	ACF	Permission of Automatic Configuration Fail Interrupt When the measurement value on automatic configuration is out of the stipulated range, this interrupt is generated.
D3	RANGE	Permission of Upper Limit Over Interrupt When the measurement value is over the upper limit in a measurement operation, this interrupt is generated.
D2	GPIN	Permission of GPIO Input Interrupt When the interrupt function is configured by GPIO control registers (Addr 0x35/0x37/…/0x43 IRQC bit),this interrupt is generated by the factor occurrence.
D1	Reserved	Reserved: This bit should be written "0".
D0	TSL	Level Output Operational Mode Selection of Touch Status 0: Edge Operation The IRQ pin responds to the edge for the interrupt factor selected by DRDY bit, TOUCH bit, REL bit, ACF bit, RANGE bit, and GPIN bit. The clearance setting, polarity setting, driver setting, and etc. are configured by Addr 0x65/0x69/0x6D. 1: Level Operation Touch function or release function is selected by TOUCH bit and REL bit. The intended terminal can be configured by IRQ mask register (Addr 0x66-0x67, 0x6A-0x6B, 0x6E-0x6F). The other interrupt factor cannot be selected. The polarity setting, driver setting, and etc. are configured by Addr 0x65/0x69/0x6D. The status cannot be cleared unlike the edge operation. The IRQ Status (IRQ2-0 bit of Addr 0x03) returns the input level of the IRQ pin.

IRQ GPIO Register (GPEN bit = "1")

Address 0x64/0x68/0x6C (W/R) Default 0x08

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ GPIO	GPEN	DIR	DAT	DRV[1]	DRV[0]	DSTR	PE	PU

Address 0x65/0x69/0x6D (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ GPIO	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bits	Name	Description
D7	GPEN	GPIO Enable This bit should be set to "1" at the GPIO operation.
D6	DIR	GPIO Input/Output Selection 0: Input Configuration 1: Output Configuration
D5	DAT	GPIO Output Data When GPIO is output configuration, the output data is setting by this bit.
D4-D3	DRV	Output Driver Setting 00: CMOS Output 01: Low Side Output: When Output is "H", Hi-z (Open Drain) 10: High Side Output: When Output is "L", Hi-z (Open Drain) 11: CMOS Output (Same as 00 Setting)
D2	DSTR	The Driving ability of the GPIO output driver is set. 0: 1/3 drive 1: full drive
D1	PE	Pull-up, Pull-down Enable 0: Invalid 1: Valid. The direction is fixed by PU bit.
D0	PU	Pull-up / Pull-down Selector 0: Pull-down 1: Pull-up

Bits	Name	Description
D7-D0	Reserved	Reserved: This bit should be written "0".

IRQ Mask Register (IRQMn: n=0~2)

Address 0x66/0x6A/0x6E (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ Mask	IRQM[15]	IRQM[14]	IRQM[13]	IRQM[12]	IRQM[11]	IRQM[10]	IRQM[9]	IRQM[8]

Address 0x67/0x6B/0x6F (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
IRQ Mask	IRQM[7]	IRQM[6]	IRQM[5]	IRQM[4]	IRQM[3]	IRQM[2]	IRQM[1]	IRQM[0]

Bits	Name	Description
15-0	IRQM	Intended channel setting of Touch/Release Interrupt 0: No Target of Interrupt 1: Target of Interrupt

Noise Filter Control Register (NFC)

Address 0x70 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Noise Filter Control	NF2S[1]	NF2S[0]	NF1S[1]	NF1S[0]	RIM[1]	RIM[0]	LCH	RCH

Bits	Name	Description
D7-D6	NF2S	Number of samples at the noise filter (the second filter) 00: 4 samples 01: 6 samples 10: 10 samples 11: 18 samples
D5-D4	NF1S	Number of samples at the noise filter (the first filter) 00: 4 samples 01: 6 samples 10: 10 samples 11: 18 samples
D3-D2	RIM	Initial Reference Setting Selection 00: User Setting (reference value set by Addr 0x80-0x9F REFn bits) 01: First Measurement Value as a Reference 10: 31/32 of First Measurement Value as a Reference 11: 30/32 of First Measurement Value as a Reference
D1	LCH	Priority Setting of sense terminals without multi touch function 0: The sense terminal to touch most strongly is selected. 1: The sense terminal of the youngest number is selected.
D0	RCH	Release Operation Setting of sense terminals without multi touch function 0: The next touch judgment is not executed until all the sense terminals are released once. 1: When the sense terminal that is judged as touched is released, the next touch judgment is executed.

These bits can not be changed by the serial I/F in run-mode.

Debounce Control Register (DEB)

Address 0x71 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Debounce Control	DEBT[3]	DEBT[2]	DEBT[1]	DEBT[0]	DEBR[3]	DEBR[2]	DEBR[1]	DEBR[0]

Bits	Name	Description
D7-D4	DEBT	Debounce Count Setting of the touch judgment When the touch recognition is consecutive, it is judged as "Touched". The consecutive time is set by these bits.
D3-D0	DEBR	Debounce Count Setting of the release judgment When the release recognition is consecutive, it is judged as "Released". The consecutive time is set by these bits.

The condition to use both the multi touch prohibition function and the debounce function: DEBT ≥ DEBR
These bits can not be changed by the serial I/F in run-mode.

Environment Filter Control Register (EFC)

Address 0x72 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Environment Filter Control	EUP[5]	EUP[4]	EUP[3]	EUP[2]	EUP[1]	EUP[0]	EUR[1]	EUR[0]

Address 0x73 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Environment Filter Control	EDP[5]	EDP[4]	EDP[3]	EDP[2]	EDP[1]	EDP[0]	EDR[1]	EDR[0]

Bits	Name	Description
D7-D2	EUP	Operation Interval of the Environmental correction filter (measurement > reference) Operation at Each "Output Rate × (1+EUP)", (EUP = 0~63) Output Rate = Sampling Rate × NF2S (Addr 0x70)
D1-D0	EUR	Operation Coefficient of the Environmental correction filter (measurement > reference) reference = reference – (reference – measurement) / (2^(EUR+1)), (EUR = 0~3)

This bits can not be changed by the serial I/F in run-mode.

Bits	Name	Description
D7-D2	EDP	Operation Interval of the Environmental correction filter (measurement < reference) Operation at Each "Output Rate × (1+EDP)", (EDP = 0~63) Output Rate = Sampling Rate × NF2S (Addr 0x70)
D1-D0	EDR	Operation Coefficient of the Environmental correction filter (measurement < reference) reference = reference – (reference – measurement) / (2^(EDR+1)), (EDR = 0~3)

These bits can not be changed by the serial I/F in run-mode.

Sampling Rate & Sense Channel Control Register (SCC)

Address 0x74 (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Sampling Rate & Sense Channel Control	TSR[2]	TSR[1]	TSR[0]	NCH[4]	NCH[3]	NCH[2]	NCH[1]	NCH[0]

Bits	Name	Description
D7-D5	TSR	Measurement Sampling Rate Setting fs = 4ms x 2^{TSR} (4ms~512ms)
D4-D0	NCH	Measurement Channel Setting Exclusive control is provided for GPIO enable function (Addr 0x5E). When a pin has already been selected as GPIO, the sense terminal selection is invalid. Refer to Table 10 for the selection setting.

TSR can be changed in run mode.

NCH	Sense Setting Terminal	NCH	Sense Setting Terminal
00000	No Selection (Shutdown mode)	01001	CS0 ~ CS8
00001	CS0	01010	CS0 ~ CS9
00010	CS0 ~ CS1	01011	CS0 ~ CS10
00011	CS0 ~ CS2	01100	CS0 ~ CS11
00100	CS0 ~ CS3	01101	CS0 ~ CS12
00101	CS0 ~ CS4	01110	CS0 ~ CS13
00110	CS0 ~ CS5	01111	CS0 ~ CS14
00111	CS0 ~ CS6	10000 - 11111	CS0 ~ CS15
01000	CS0 ~ CS7		

Table 10. Sense Setting Terminal

Soft Reset Register (SRST)

Address 0x7E (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Soft Reset	SRST[7]	SRST[6]	SRST[5]	SRST[4]	SRST[3]	SRST[2]	SRST[1]	SRST[0]

Bits	Name	Description
D7-D0	SRST	When "SRST=0x55" is written, reset is generated. All registers become the initial values. This register is read as "0x00".

Reference Data Register (REFn: n=0~15)

Address 0x80/0x82/…/0x9E (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Reference Data	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	REFn[9]	REFn[8]

Address 0x81/0x83/…/0x9F (W/R) Default 0x00

Description	D7	D6	D5	D4	D3	D2	D1	D0
Reference Data	REFn[7]	REFn[6]	REFn[5]	REFn[4]	REFn[3]	REFn[2]	REFn[1]	REFn[0]

Bits	Name	Description
15-10	Reserved	Reserved: This bit should be written "0".
9-0	REFn	Reference value for each sense terminal

SYSTEM DESIGN

Figure 18 and Figure 19 show the system connection diagram for the AK4160. An evaluation board [AKD4160] demonstrates the optimum layout, power supply arrangements and measurement results.

<16ch Touch Switch>

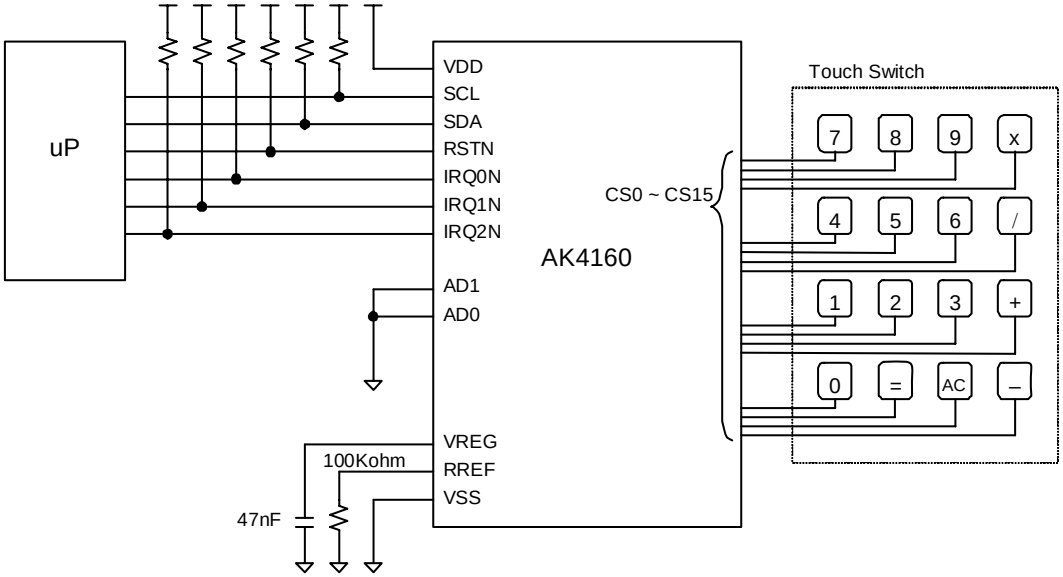


Figure 18. Typical Connection Diagram for 16ch Touch Switch

<8ch Touch Switch & 8ch LED Display >

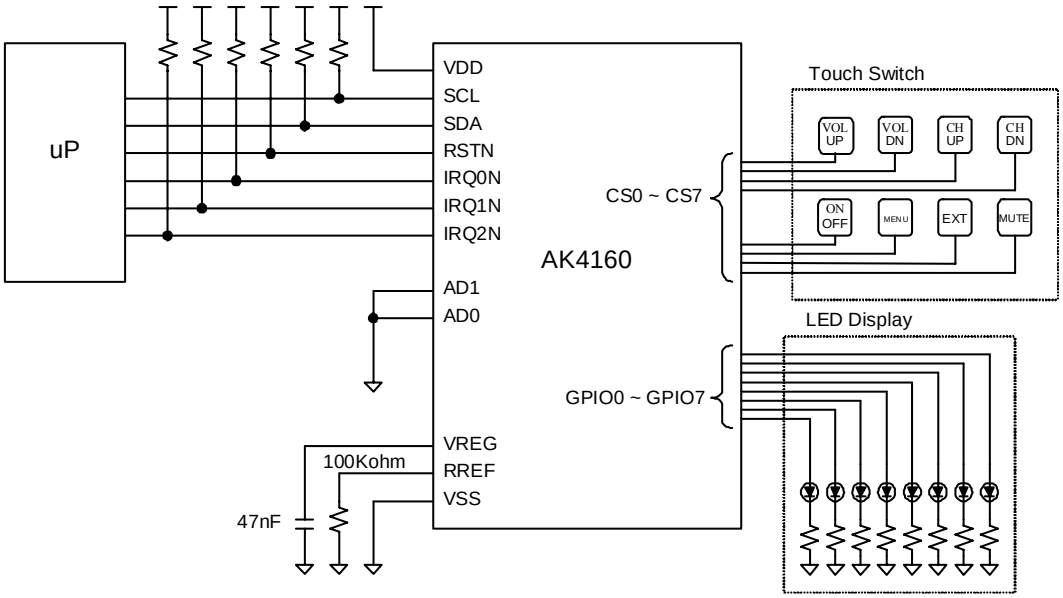


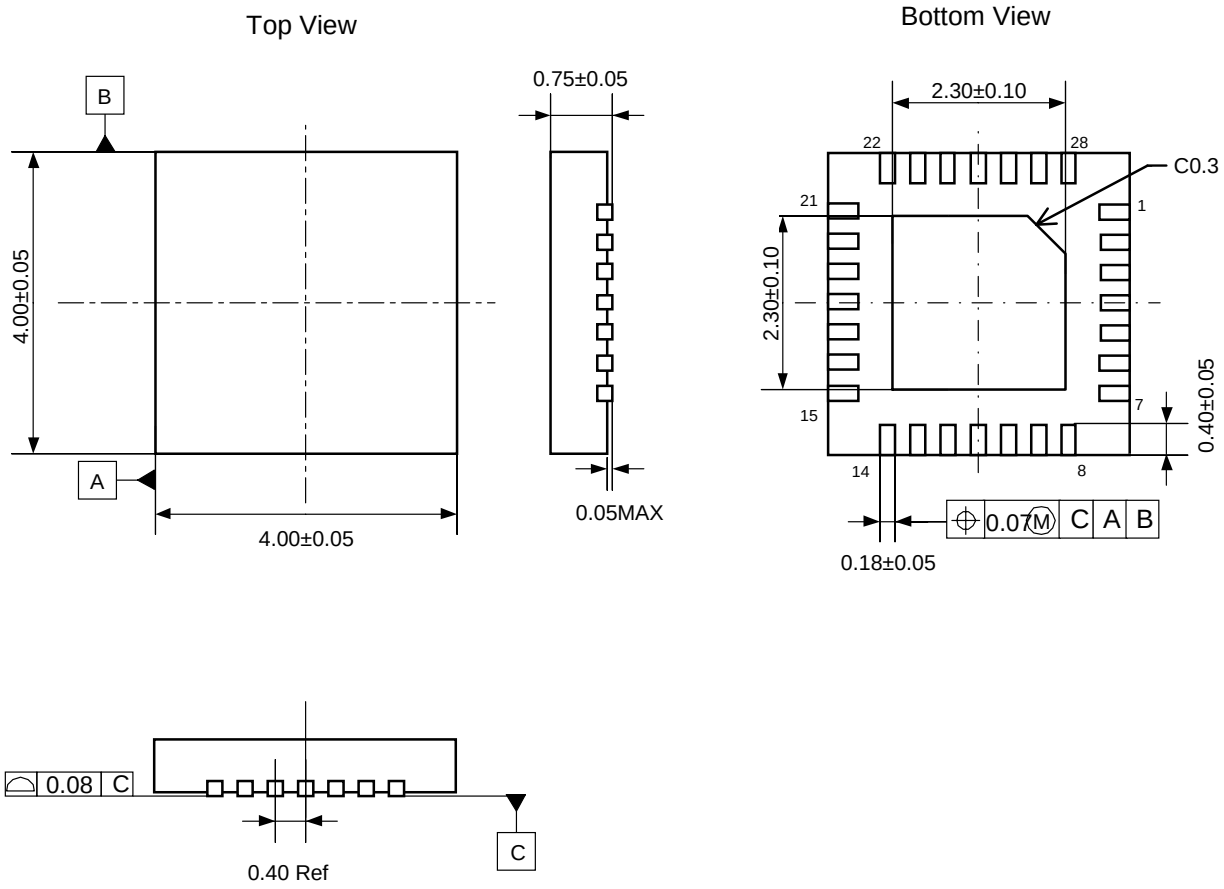
Figure 19. Typical Connection Diagram for 8ch Touch Switch & 8ch LED Display

Note:

- These figures are the connection diagram when the AD0 pin = "L" and the AD1 pin = "L". In case of the AD0 pin = "H" or the AD1 pin = "H", their pin must be connected to VDD.
- VSS of the AK4160 should be distributed separately from the ground of external controllers.
- All digital input pins (SCL, SDA, AD0, AD1, RSTN pins) must not be left floating.

PACKAGE

28pin QFN (Unit: mm)

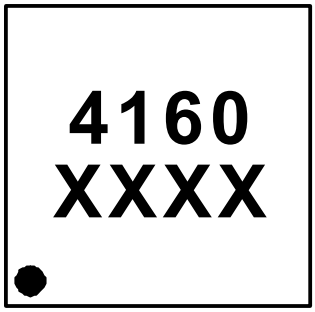


Note: The thermal die pad must be open or connected to the ground.

■ Package & Lead frame material

Package molding compound: Epoxy Resin, Halogen (Br, Cl) Free
Lead frame material: Cu Alloy
Lead frame surface treatment: Solder Plate

MARKING



Date Code: XXXX (4 digits)
Pin #1 indication

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
11/07/25	00	First Edition		
11/11/24	01	Specification Addition	6	DC CHARACTERISTICS Pull-up Current were added: 5uA (min), 200uA (max) Pull-down Current were added: -200uA (min), -5uA (max)
		Error Correction	34	Register definition Operation interval expression (EUP) was changed: Output Rate/(1+EUP) → Output Rate×(1+EUP) Operation interval expression (EDP) was changed: Output Rate/(1+EDP) → Output Rate×(1+EDP)

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