

### FEATURES

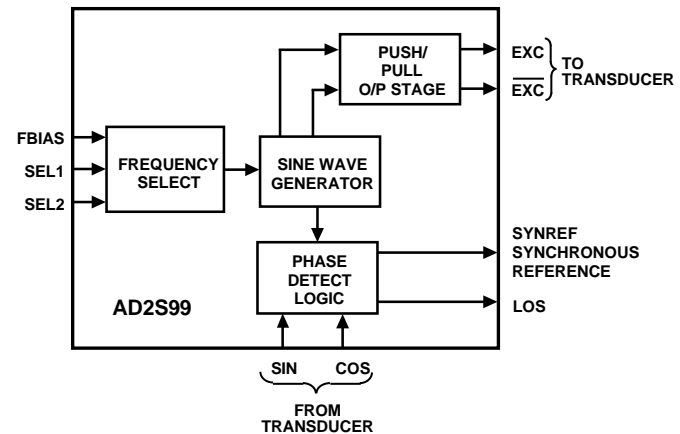
**Programmable Sinusoidal Oscillator**  
**Synthesized Synchronous Reference Output**  
**Programmable Output Frequency Range: 2 kHz–20 kHz**  
**“Loss-of-Signal” Indicator**  
**20-Pin PLCC Package**  
**Low Cost**

### APPLICATIONS

Excitation Source for:

**Resolvers**  
**Synchros**  
**LVDTs**  
**RVDTs**  
**Pressure Transducers**  
**Load Cells**  
**AC Bridges**

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The AD2S99 programmable sinusoidal oscillator provides sine wave excitation for resolvers and a wide variety of ac transducers. The AD2S99 also provides a synchronous reference output signal (3 V p-p square wave) that is phase locked to its SIN and COS inputs. In an application, the SIN and COS inputs are connected to the transducer's secondary windings.

The synchronous reference output compensates for temperature and cabling dependent phase shifts and eliminates the need for external preset phase compensation circuits. The synchronous reference output can be used as a zero crossing reference for resolver-to-digital converters such as Analog Devices' AD2S80A, AD2S82A, AD2S83 and AD2S90.

The AD2S99 is packaged in a 20-pin PLCC and operates over  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### PRODUCT HIGHLIGHTS

#### Dynamic Phase Compensation

The AD2S99 dynamically compensates for any phase variation in a transducer by phase locking its synchronous reference output to the transducer's secondary windings.

#### Programmable Excitation Frequency

The excitation frequency is easily programmed to 2 kHz, 5 kHz, 10 kHz, or 20 kHz by using the frequency select pins. Intermediate frequencies are available by adding an external resistor.

#### Signal Loss Detection

The AD2S99 has the ability to detect if both the transducer secondary winding connections become disconnected from its SIN and COS inputs. The "LOS" output pin pulls high when a signal loss is detected.

#### Integration

The AD2S99 integrates the transducer excitation, synchronous reference, and loss of signal detection functions into a small, cost effective package.

### REV. B

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# AD2S99—SPECIFICATIONS ( $V_S = \pm 4.75\text{ V to } \pm 5.25\text{ V @ } -40^\circ\text{C to } +85^\circ\text{C unless otherwise noted}$ )

| Parameter   | Min      | Typ      | Max       | Units   | Test Conditions  |
|---|----------|----------|-----------|---------|--|
| FREQUENCY OUTPUT RANGE                              |          |          |           |         | SEL1 SEL2  |
| 2 kHz   |          | 2000     |           | Hz      | $V_{SS}$ $V_{SS}$  |
| 5 kHz   |          | 5000     |           | Hz      | $V_{SS}$ GND   |
| 10 kHz  |          | 10000    |           | Hz      | GND $V_{SS}$   |
| 20 kHz  |          | 20000    |           | Hz      | GND GND  |
| ACCURACY  |          |          |           |         |  |
| Frequency   |          |          | $\pm 10$  | %       | AP Grade @ +25°C   |
|   |          |          | $\pm 20$  | %       | AP Grade -40°C to +85°C  |
|   |          |          | $\pm 5$   | %       | BP Grade @ +25°C   |
|   |          |          | $\pm 10$  | %       | BP Grade -40°C to +85°C  |
| Amplitude   |          | $\pm 3$  | $\pm 10$  | %       | AP Grade @ +25°C   |
|   |          |          | $\pm 20$  | %       | AP Grade -40°C to +85°C  |
|   |          | $\pm 3$  | $\pm 5$   | %       | BP Grade @ +25°C   |
|   |          |          | $\pm 10$  | %       | BP Grade -40°C to +85°C  |
| Power Supply Rejection Ratio                        |          | 0.002    |           | V p-p/V | Output Variation as Function of Change in Power Supply Voltage |
| ANALOG OUTPUTS                                      |          |          |           |         |  |
| Amplitude   |          |          |           |         |  |
| EXC, $\overline{\text{EXC}}$                        |          | 2        |           | V rms   | EXC to GND, $\overline{\text{EXC}}$ to GND                     |
| SYNREF  |          | $\pm 3$  |           | V p-p   | Square Wave  |
| SYNREF OFFSET                                       |          |          | $\pm 200$ | mV      |  |
| Current Drive Capability                            |          |          |           |         |  |
| EXC, $\overline{\text{EXC}}$ $V_S = \pm 5\text{ V}$ |          |          | 8         | mA rms  | $R_{LOAD} = 500\ \Omega$ $\overline{\text{EXC}}$ to EXC        |
| Capacitive Drive                                    |          |          | 1000      | pF      | $C_{LOAD} = 1000\text{ pF}$                                    |
| Total Harmonic Distortion                           |          |          |           |         |  |
| EXC, $\overline{\text{EXC}}$                        |          |          | -25       | dB      |  |
| ANALOG INPUTS SIN, COS                              |          |          |           |         |  |
| Amplitude   | 1.8      | 2.0      | 2.2       | V rms   |  |
| Phase Lock Range                                    | -45      |          | +45       | Degrees |  |
| Additional Phase Delay                              |          |          | $\pm 10$  | Degrees | AP Grade   |
|   |          |          | $\pm 10$  | Degrees | BP Grade   |
| FREQUENCY SELECT INPUTS                             |          |          |           |         |  |
| SEL1, SEL2 <sup>1</sup>                             | $V_{SS}$ |          | AGND      | V dc    |  |
| LOS OUTPUT  |          |          |           |         |  |
| Output Low Voltage                                  |          |          | 0.7       | V dc    | $I_{OL} = 400\ \mu\text{A}$                                    |
| Output High Voltage                                 |          | $V_{DD}$ |           | V dc    | 50 k $\Omega$ Pull Up to $V_{DD}$ (Open Drain Output)          |
| SIN, COS LOS Threshold                              | 0.5      | 0.6      | 0.8       | V rms   |  |
| POWER SUPPLIES                                      |          |          |           |         |  |
| $V_{DD}$  | +4.75    |          | +5.25     | V dc    |  |
| $V_{SS}$  | -4.75    |          | -5.25     | V dc    |  |
| Quiescent Current $I_{DD}$ , $I_{SS}$               |          | $\pm 8$  | $\pm 15$  | mA      | No Load  |
| TEMPERATURE RANGE                                   |          |          |           |         |  |
| Operating   | -40      |          | +85       | °C      |  |
| Storage   | -65      |          | +150      | °C      |  |

## NOTES

<sup>1</sup>Frequency select pins SEL1 and SEL2 must be connected to appropriate voltage levels before power is applied.

Specifications subject to change without notice.

# AD2S99

## ABSOLUTE MAXIMUM RATINGS\*

|   |                            |
|---|----------------------------|
| V <sub>DD</sub> .....                     | +7 V                       |
| V <sub>SS</sub> .....                     | -7 V                       |
| Operating Temperature .....               | -40°C to +85°C             |
| Storage Temperature .....                 | -65°C to +150°C            |
| Analog Input Voltages (SIN and COS) ..... | V <sub>SS</sub> - 0.3 V    |
| .....                                     | to V <sub>DD</sub> + 0.3 V |
| Frequency Select (SEL1, SEL2) .....       | V <sub>SS</sub> - 0.4 V    |
| .....                                     | to AGND + 0.4 V            |

\*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

|  |                         |
|--|-------------------------|
| Power Supply Voltage (V <sub>DD</sub> to V <sub>SS</sub> ) ..... | ±4.75 V to ±5.25 V      |
| Analog Input Voltage (SIN and COS) .....                         | 2 V rms ±10%            |
| Frequency Select (SEL1 and SEL2) .....                           | V <sub>SS</sub> to AGND |
| Operating Temperature Range .....                                | -40°C to +85°C          |

## ORDERING GUIDE

| Model    | Temperature Range | Package Option* |
|----------|-------------------|-----------------|
| AD2S99AP | -40°C to +85°C    | P-20A           |
| AD2S99BP | -40°C to +85°C    | P-20A           |

\*P = PLCC.

## PIN DESIGNATIONS

| Pin No.         | Mnemonic                | Description  |
|-----------------|-------------------------|--|
| 1               | SEL2                    | Frequency Select 2   |
| 2               | SEL1                    | Frequency Select 1   |
| 3               | FBIAS                   | External Frequency Adjust Pin                                |
| 5               | SIN                     | Resolver Output SIN  |
| 6 <sup>1</sup>  | DGND                    | Digital Ground   |
| 7               | COS                     | Resolver Output COS  |
| 10              | SYNREF                  | Synthesized Reference Output                                 |
| 11              | LOS                     | Indicates When Both the SIN and COS Are Below the Threshold. |
| 12              | V <sub>DD</sub>         | Positive Power Supply  |
| 16 <sup>1</sup> | AGND                    | Analog Ground  |
| 17              | EXC                     | Resolver Reference One                                       |
| 18              | $\overline{\text{EXC}}$ | Resolver Reference Two <sup>3</sup>                          |
| 19 <sup>2</sup> | V <sub>SS</sub>         | Negative Power Supply  |
| 20 <sup>2</sup> | V <sub>SS</sub>         | Negative Power Supply  |

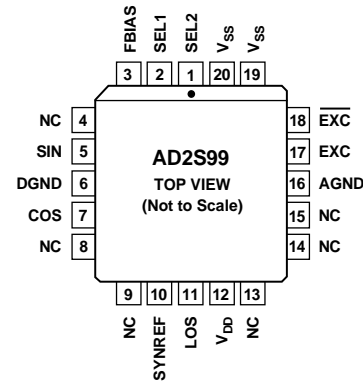
## NOTES

<sup>1</sup>Pins 6 and 16 must be connected together.

<sup>2</sup>Pins 19 and 20 must be connected together.

<sup>3</sup>Resolver Reference two ( $\overline{\text{EXC}}$ ) is 180° phase advanced with respect to Resolver Reference one (EXC).

## PIN CONFIGURATION



NC = NO CONNECT

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD2S99 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





## AD2S99/AD2S90 TYPICAL CONFIGURATION

Figure 3 shows a typical circuit configuration for the AD2S99 Oscillator and the AD2S90 Resolver-to-Digital Converter. The maximum level of the SIN and COS input signals to the AD2S90 should be 2 V rms  $\pm$  10%. All the analog ground signals should be star connected to the AD2S90 AGND pin. If shielded twisted pair cables are used for the resolver signals, the

shields should also be terminated at the AD2S90 AGND pin. The SYNREF output of the AD2S99 should be connected to the REF input pin of the AD2S90 via a 0.1  $\mu$ F capacitor with a 100 k $\Omega$  resistor to GND. This is to block out any dc offset in the SYNREF signal. For more detailed information please refer to the AD2S90 data sheet.

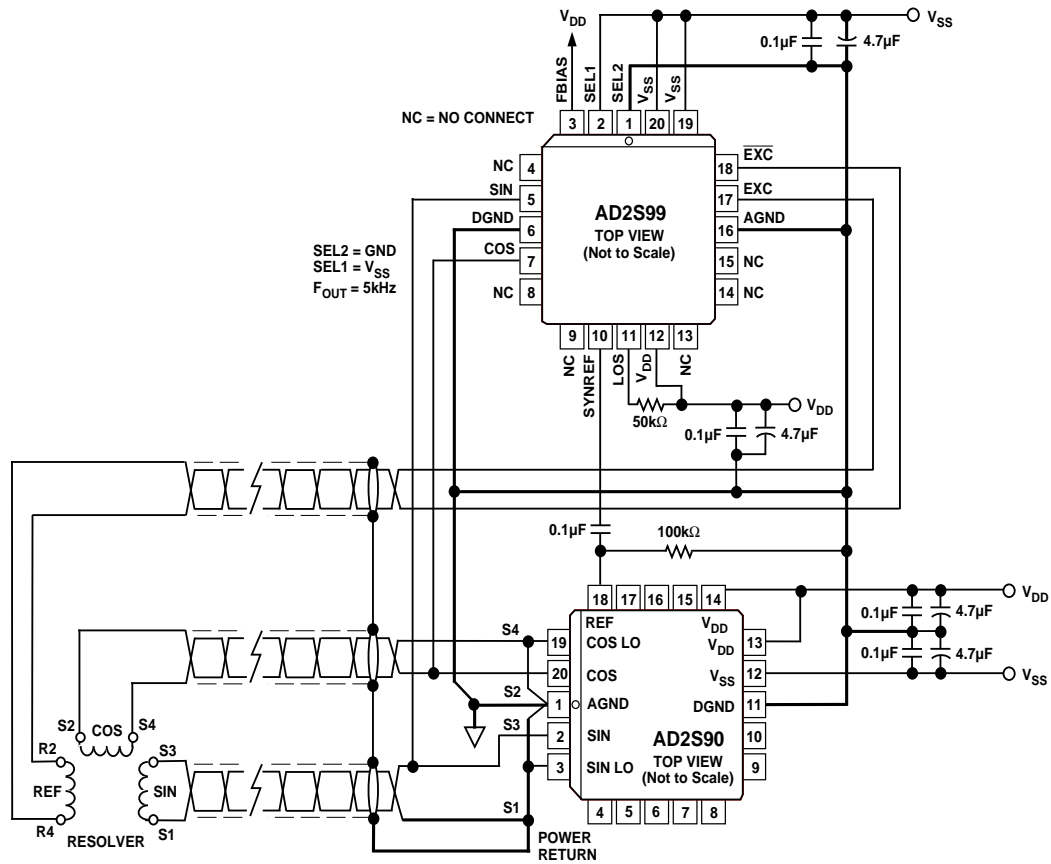


Figure 3. AD2S99 and AD2S90 Example Configuration

# AD2S99

## AD2S99/AD2S82A TYPICAL CONFIGURATION

Figure 4 shows a typical circuit configuration for the AD2S99 Oscillator and the AD2S82A Resolver-to-Digital Converter. The maximum level of the SIN and COS input signals to the AD2S82A should be 2 V rms  $\pm$ 10%. All the analog ground signals should be star connected to the AD2S82A AGND pin. If shielded twisted pair cables are used for the resolver signals, the shields should also be terminated at the AD2S82A AGND pin.

Coupling capacitor C3, and resistor to GND R3, between the SYNREF output of the AD2S99 and the REF input pin of the AD2S82A are optional. For additional information on selecting component values for the AD2S82A, please refer to the AD2S82A data sheet or the application note "Passive Component Selection and Dynamic Modeling for the AD2S80 Series Resolver-to-Digital Converters" (AN-266).

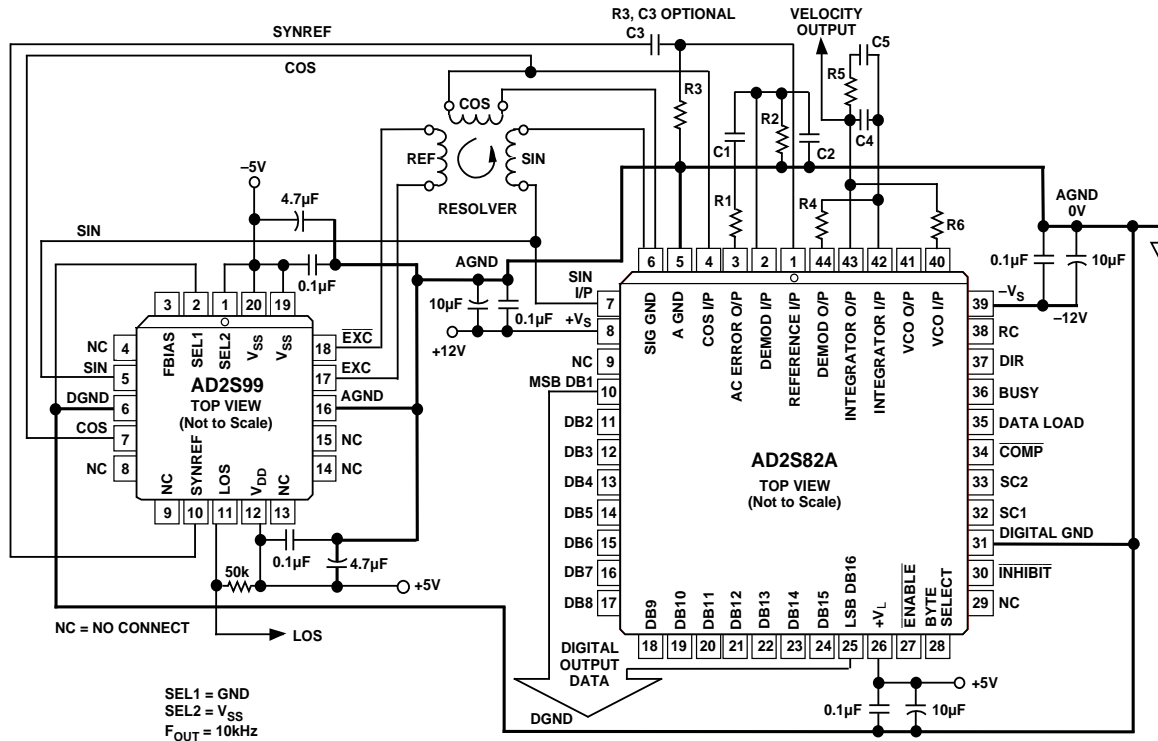


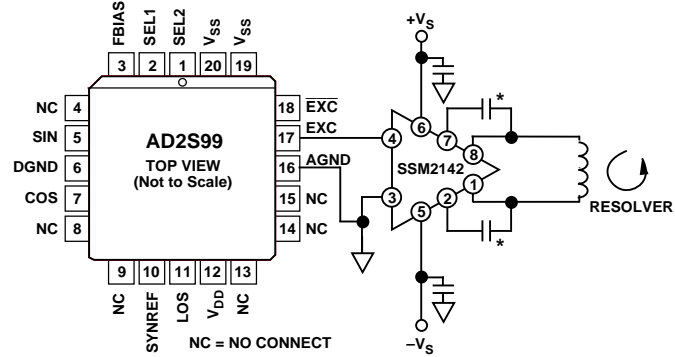
Figure 4. AD2S99 and AD2S82A Example Configuration



# AD2S99



Figure 6. Sample Buffer Configuration



\*OPTIONAL; CONSULT APPROPRIATE ANALOG DEVICES DATA SHEET.

Figure 8. The SSM2142 as a Single Ended to Differential Driver

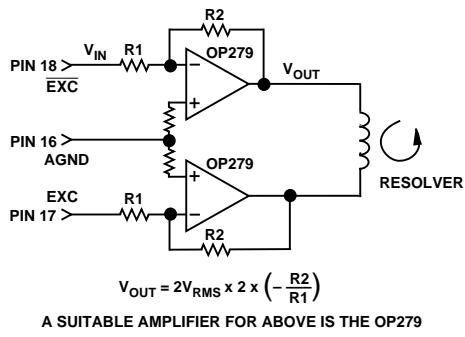
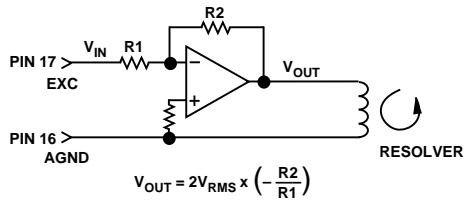
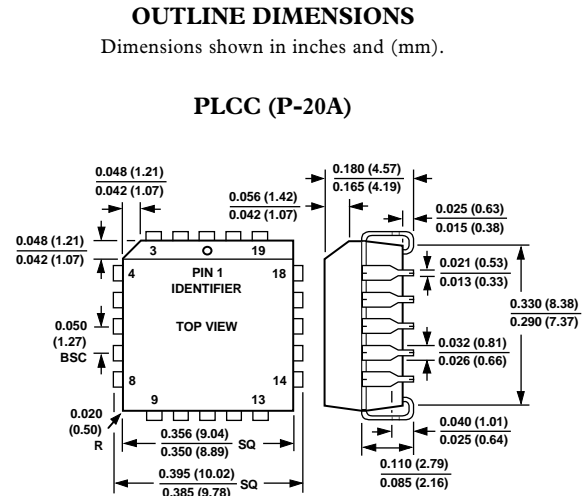


Figure 7. Sample Buffer Configurations



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