

82C54

CMOS Programmable Interval Timer

The AMD 82C54 is a high-performance, CMOS version of the industry-standard 8254 counter/timer which is designed to solve the timing-control problems common in microcomputer system design. It provides three independent 16-bit Counters—each capable of handling clock inputs up to 12.5 MHz. All modes are software-programmable. The 82C54 is pin-compatible with the NMOS 8254 and is a superset of the 8253.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

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MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Compatible with all Intel and most other microprocessors
- High-speed, zero-wait-state operation with 10-MHz 8086/88 and 80186/188
- Three independent 16-bit counters
- Handles inputs from DC to 8 MHz
 - 10 MHz for 82C54-2
 - 12.5 MHz for 82C54-12

- Low-power CMOS
 - I_{CC} = 50 μA military standby current I_{CC}
- Completely TTL compatible
- Six programmable counter modes
- Binary or BCD counting
- Status read-back command
- Available in 24-pin DIP

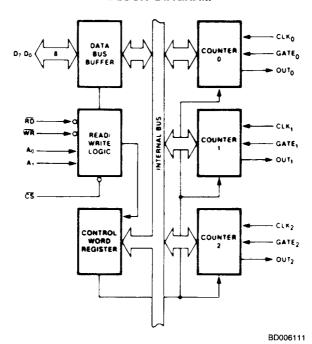
GENERAL DESCRIPTION

The AMD 82C54 is a high-performance, CMOS version of the industry-standard 8254 counter/timer which is designed to solve the timing-control problems common in microcomputer system design. It provides three independent 16-bit Counters—each capable of handling clock inputs up to 12.5 MHz. All modes are software-programmable. The 82C54 is pin-compatible with the NMOS 8254 and is a superset of the 8253.

Six programmable-timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications as well.

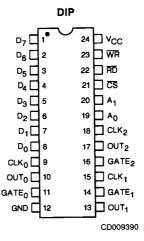
The 82C54 is fabricated with AMD's CMOS technology providing low-power consumption with performance equal to or greater than the equivalent NMOS product. The 82C54 is available in 24-pin DIP package.

BLOCK DIAGRAM



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CONNECTION DIAGRAM Top View



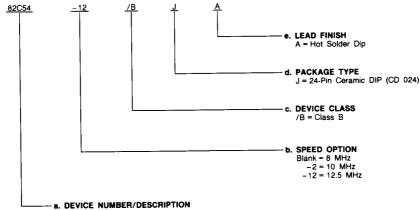
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: a. Device Number

- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



82C54 CMOS Programmable Interval Timer

Valid Combinations		
82C54		
82C54-2	/BJA	
82C54-12	T	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature65 to	+ 150°C
Voltage on Any Pin	
with Respect to GND0.5 to	+7.0 V
Power Dissipation	1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices			
Temperature (T _C)55	to	+	125°C
Supply Voltage (V _{CC})	.5	٧	±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V _{IL}	Input LOW Voltage			-0.5*	0.8	V
VIH	Input HIGH Voltage			2.2	V _{CC} + 0.5 V*	V
VOL	Output LOW Voltage	I _{OL} = 2.0 mA		1	.45	V
Voн	Output HIGH Voltage	I _{OH} = -400 μA		2.4		V
I _{IL}	Input Load Current	VIN = VCC to 0 V	1		± 10	μΑ
IOFL	Output Float Leakage Current	V _{OUT} = V _{CC} to 0 V			±10	μΑ
		8 MHz		20		
Icc	Operating Power-Supply Current (Note 1)	CLK Freq 10 M	10 MHz		20	mA
	12.5	12.5 MHz		20		
ICCSB	Standby Power-Supply Current (Note 2)	CLK CO. DC., S. F. H., N. Inpers/Data Bus HIGH, All Quiputs Floating			±50	μΑ

CAPACITANCE (T_C = 25°0 V_G GND = 0 V)

Parameter Symbol	Description	Test Conditions	Min.	Max.	Units
C _{IN} +	Input Capacitance	fc = 1 MHZ		10*	pF
C _{I/O †}	I/O Capacitance	Unmeasured pins		20*	pF
C _{OUT} †	Output Capacitance	returned to GND		20*	pF

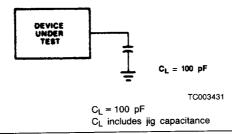
^{*} Guaranteed by design; not tested.

Notes: 1. ICC is measured in a dynamic condition with no output loads applied and inputs at rail levels.

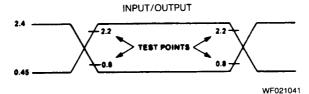
 Standby I_{CC} is measured in a static condition (CLK = DC) with no output loads applied, and CS and all inputs/ databus at the V_{CC} rail level.

[†] Not included in Group A tests.

SWITCHING TEST CIRCUIT



SWITCHING TEST WAVEFORM



A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.2 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1).

Parameter		8 MHz		10 MHz		12.5 MHz			
No.	Symbol	Parameter Description	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ C	CYCLE	-							
1	t _{AR}	Address Stable Before RD ↓	45		30		25		ns
2	t _{SR}	CS Stable Before RD ↓	0		0		0		ns
3	t _{RA}	Address Hold Time After RD ↑	0		0		0		ns
4	t _{RR}	RD Pulse Width	150		95		90		ns
5	tRD	Data Delay from RD ↓		120		85		80	ns
6	t _{AD}	Data Delay from Address		220		185		150	ns
7	t _{DF}	RD ↑ to Data Floating	5	90	5	65	5	55	ns
8	t _{RV}	Command Recovery Time	200		165		135		ns
WRITE	CYCLE							<u> </u>	
9	t _{AW}	Address Stable Before WR ↓	0				0		ns
10	tsw	CS Stable Before WR ↓	0		J		0	†	ns
11	t _{WA}	Address Hold Time After WR ↑	0	X	0		0		ns
12	tww	WR Pulse Width	1	2	95		80		ns
13	t _{DW}	Data Setup Time Before WR ↑	1	1	95		80		ns
14	t _{WD}	Data Hold Time After WR ↑	0		0		0		ns
15	t _{RV}	Command Recovery Time	200		165		135		ns
CLOCK	AND GATE CY	/CLE							
16	tCLK	Clock Period	125	DC	100	DC	80	DC	ns
17	tpwH	HIGH Pulse Width (N. e 3)	60		30		30		ns
18	tpwL	LOW Pulse Width Note 3)	60		50		40		ns
19	t _R	Clock Ris 1 e Note 4)		25		25		25	ns
20	tF	Clock 2 (Note 4)		25		25		25	ns
21	tgw	Gale With HIGH	50		50		40		ns
22	t _{GL}	Gate Width LOW	50		50		40		ns
23	t _{GS}	Gate Setup Time to CLK ↑	50		40		30		ns
24	tgн	Gate Hold Time After CLK ↑ (Note 2)	50		50		40		ns
25	t _{OD}	Output Delay from CLK ↓		150		100		80	ns
26	tong	Output Delay from Gate ↓		120		100		80	ns
27	twc	CLK Delay for Loading	0	55	0	55	0	45	ns
28	twG	Gate Delay for Sampling	-5	50	- 5	40	-5	35	ns
29	two	Out Delay from Mode Write		260		240		200	ns
30	t _{CL}	CLK Set Up for Count Latch	- 4	45	- 4	40	-4	35	ns

Notes: 1. Timings measured at V_{OH} = 2.2 V, V_{OL} = 0.8 V. C_L = 100 pF ±20 pF.

In Modes 1 and 5, triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the 82C54-2) of the rising clock edge may not be detected.

^{3.} LOW-going glitches that violate tpWH, tpWL may cause errors requiring Counter re-programming.

^{4.} Clock rise and fall times are tested at 5 ns, guaranteed by Teradyne J941 test equipment.