HARRIS SEMICONDUCTOR

HSP45116

Numerically Controlled Oscillator/Modulator

May 1996

Features

- NCO and CMAC on One Chip
- 15MHz, 25.6MHz, 33MHz Versions
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.008Hz Tuning Resolution at 33MHz
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

Applications

- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HSP45116VC-15	0 to 70	160 Ld MQFP	Q160.28x28
HSP45116VC-25	0 to 70	160 Ld MQFP	Q160.28x28
HSP45116GC-15	0 to 70	145 Ld CPGA	G145.A
HSP45116GC-25	0 to 70	145 Ld CPGA	G145.A
HSP45116GC-33	0 to 70	145 Ld CPGA	G145.A
HSP45116GI-15	-40 to 85	145 Ld CPGA	G145.A
HSP45116GI-25	-40 to 85	145 Ld CPGA	G145.A
HSP45116GI-33	-40 to 85	145 Ld CPGA	G145.A
HSP45116GM-15/883	-55 to 125	145 Ld CPGA	G145.A
HSP45116GM-25/883	-55 to 125	145 Ld CPGA	G145.A
HSP45116AVC-52 †	0 to 70	160 Ld MQFP	Q160.28x28

†This part has its own data sheet under HSP45116A, AnswerFAX document no. 4156.

Description

The Harris HSP45116 combines a high performance quadrature numerically controlled oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the block diagram, the HSP45116 is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/Cosine Section with an external complex vector.

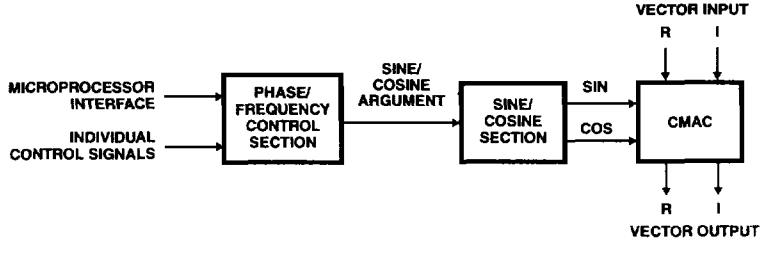
The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32 bits, which results in frequency resolution better than 0.008Hz at 33MHz. The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be down converted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal.

5 STANDARD PRODUCTS

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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