

ISL68137

Digital Dual Output, 7-Phase Configurable PWM Controller with Adaptive Voltage Scaling Bus (AVSBus)

FN8757
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The [ISL68137](#) is a digital dual output, flexible multiphase ($X+Y \leq 7$) PWM controller with Adaptive Voltage Scaling Bus (AVSBus) interface. The ISL68137 can be configured to support any desired phase assignments up to a maximum of seven phases across the two outputs ($X+Y$). For example, 6+1, 5+2, 4+2, 3+3, 3+2, or even a single output as a 7+0 configuration are supported. The flexible phase arrangement, combined with PMBus and AVSBus interfaces, allows the device to support any demanding power supply requirement. The ISL68137 with AVSBus complements PMBus by providing a common interface that accelerates point-to-point communication between the controller and the load to statically and dynamically control the processor voltage, thus delivering a balanced and power-efficient solution. AVSBus can be used exclusively after the device is configured using PMBus. The ISL68137 uses Intersil's proprietary linear synthetic digital current modulation scheme to achieve the industry's best combination of transient response and ease of tuning, while addressing the challenges of modern multiphase designs.

Device configuration and telemetry monitoring is accomplished using Intersil's intuitive PowerNavigator™ GUI. The ISL68137 device supports on-chip nonvolatile memory to store various configuration settings that are user selectable through pin-strap, giving system designers increased power density to configure and deploy multiple configurations. The device supports an automatic phase add/drop feature to allow maximum efficiency across all load ranges. Thresholds for automatic phase add/drop are user programmable using the powerful PowerNavigator GUI.

The ISL68137 supports a comprehensive fault management system to enable the design of highly reliable systems. From a multitiered overcurrent protection scheme, to the configurable power-good and output overvoltage/undervoltage fault thresholds and temperature monitoring, almost any need is accommodated.

With minimal external components, easy configuration, robust fault management, and highly accurate regulation capability, implementing a high-performance multiphase regulator has never been easier.

Applications

- Networking equipment
- Telecom and datacom equipment
- Server and storage equipment
- Point-of-load power supply (Memory, DSP, ASIC, FPGA)

Features

- PMBus 1.3 and AVSBus compliant
 - Telemetry - V_{IN} , V_{OUT} , I_{OUT} , power IN/OUT, temperature, and various fault status registers
 - Individual AVSBus interface enables high speed voltage changes
- Advanced linear digital modulation scheme
 - Zero latency synthetic current control for excellent HF current balance
 - Dual-edge modulation for fastest transient response
- Auto phase add/drop for excellent load vs efficiency profile
- Flexible phase configuration
 - 7+0, 6+1, 5+2, 4+3 phase operation
 - Operation using less than seven phases between two outputs is also supported
- Diode braking for overshoot reduction
- Differential remote voltage sensing supports $\pm 0.5\%$ closed loop system accuracy over load, line, and temperature
- Highly accurate current sensing for excellent load-line regulation and accurate OCP
 - Supports ISL99227 60A smart power stages
 - Supports DCR sense with integrated temperature compensation
- Supports phase doubler (ISL6617A) for up to 14-phase operation
- Comprehensive fault management enables high reliability systems
 - Pulse-by-pulse phase current limiting
 - Total output current protection
 - Output and input OV/UV
 - Open voltage sense detect
 - Black box recording capability for faults
- Intuitive configuration using the [PowerNavigator](#) GUI
 - NVM to store up to eight configurations
- Pb-free (RoHS compliant)

Related Literature

- For a full list of related documents, visit our website
 - [ISL68137](#) product page

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Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (RoHS COMPLIANT) | PKG. DWG. # |
|--------------------------------|--------------|---------------------|-----------------------------|----------------|
| ISL68137IRAZ | ISL68137 IRZ | -40 to +85 | 48 Ld 6x6 QFN | L48.6x6B |

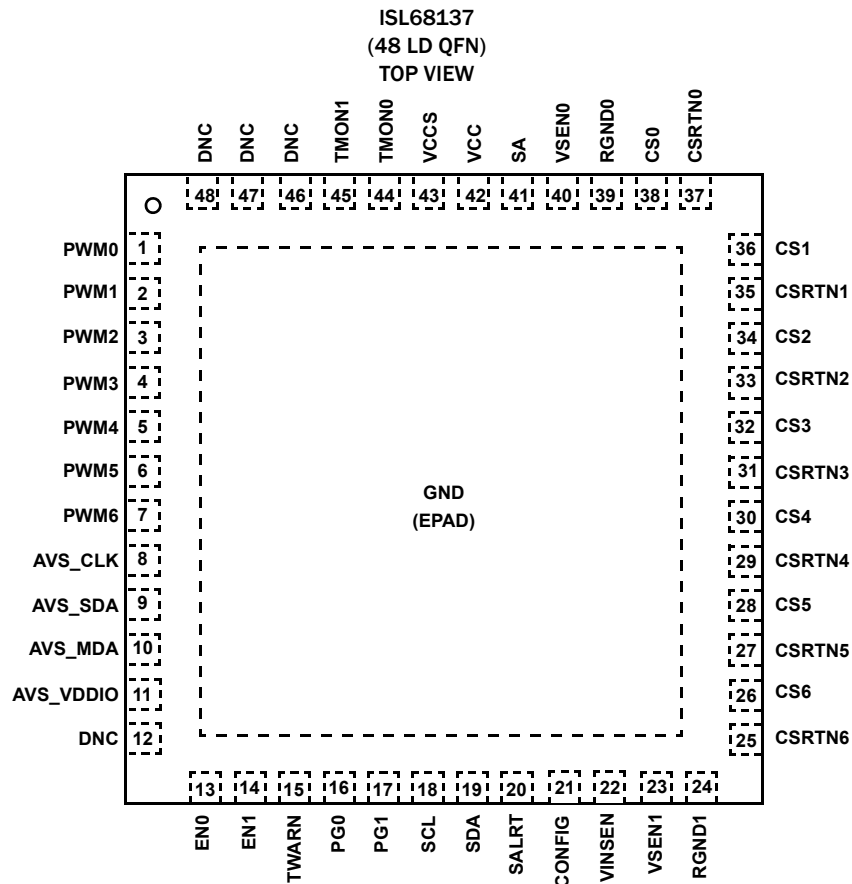
NOTES:

1. Add "-T" suffix for 4k unit or "-T7A" suffix for 250 unit tape and reel options. Refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for [ISL68137](#). For more information on MSL, see [TB363](#).

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

| PART NUMBER | PHASE CONFIGURATION OUTPUT X/OUTPUT Y | SPECIFICATION SUPPORTED | PACKAGE |
|-------------|--|-------------------------|-------------------|
| ISL68137 | $X+Y \leq 7$ | PMBus/AVSBus | QFN 48 Ld, 6x6mm |
| ISL68134 | $X+Y \leq 4$ | PMBus/AVSBus | TQFN 40 Ld, 5x5mm |
| ISL68127 | $X+Y \leq 7$ | PMBus | QFN 48 Ld, 6x6mm |
| ISL68124 | $X+Y \leq 4$ | PMBus | TQFN 40 Ld, 5x5mm |

Pin Configuration



Functional Pin Descriptions

Refer to [Table 4 on page 21](#) for design layout considerations.

| PIN NUMBER | PIN NAME | DESCRIPTION |
|----------------------------|------------|---|
| 7, 6, 5, 4, 3, 2, 1 | PWM[6:0] | Pulse width modulation outputs. Connect these pins to the PWM input pins of 3.3V logic compatible Intersil smart power stages, driver IC(s), or power stages. |
| 8 | AVS_CLK | AVSBus clock input pin. Connect to ground if not used. |
| 9 | AVS_SDA | AVSBus data output pin. Leave open if not used. |
| 10 | AVS_MDA | AVSBus data input pin. Connect to ground if not used. |
| 11 | AVS_VDDIO | AVSBus reference voltage input pin. Leave open if not used. |
| 12, 46, 47, 48 | DNC | Do not connect any signals to these pins. |
| 13 | EN0 | Input pin used for enable control of Output 0. Active high. Connect to ground if not used. |
| 14 | EN1 | Input pin used for enable control of Output 1. Active high. Connect to ground if not used. |
| 15 | TWARN | Thermal warning flag. This open-drain output will be pulled low in the event of a sensed over-temperature at TMON pins without disabling the regulators. Maximum pull-up voltage is V_{CC} . |
| 16 | PG0 | Open-drain, power-good indicators for Output 0. Maximum pull-up voltage is V_{CC} . |
| 17 | PG1 | Open-drain, power-good indicators for Output 1. Maximum pull-up voltage is V_{CC} . |
| 18 | SCL | Serial clock signal pin for SMBus interface. Maximum pull-up voltage is V_{CC} . |
| 19 | SDA | Serial data signal pin for SMBus interface. Maximum pull-up voltage is V_{CC} . |
| 20 | SALRT | Serial alert signal pin for SMBus interface. Maximum pull-up voltage is V_{CC} . |
| 21 | CONFIG | Configuration ID selection pin. See Table 3 for more details. |
| 22 | VINSEN | Input voltage sense pin. Connect to VIN through a resistor divider (typically 40.2k/10k) with a 10nF decoupling capacitor. |
| 23 | VSEN1 | Positive differential voltage sense input for Output 1. Connect to positive remote sensing point. Connect to ground if not used. |
| 24 | RGND1 | Negative differential voltage sense input for Output 1. Connect to negative remote sensing point. Connect to ground if not used. |
| 25, 27, 29, 31, 33, 35, 37 | CSRTN[6:0] | The CS and CSRTN pins are current sense inputs to individual phase differential amplifiers. Unused phases should have their respective current sense inputs grounded. The ISL68137 supports smart power stage, DCR, and resistor sensing. Connection details depend on current sense method chosen. |
| 26, 28, 30, 32, 34, 36, 38 | CS[6:0] | |
| 39 | RGND0 | Negative differential voltage sense input for Output 0. Connect to negative remote sensing point. Connect to ground if not used. |
| 40 | VSEN0 | Positive differential voltage sense input for Output 0. Connect to positive remote sensing point. Connect to ground if not used. |
| 41 | SA | PMBus Address selection pin. See Table 2 on page 13 for more details. |
| 42 | VCC | Chip primary bias input. Connect this pin directly to a +3.3V supply with a high quality MLCC bypass capacitor. |
| 43 | VCCS | Internally generated 1.2V LDO logic supply from VCC. Decouple with 4.7 μ F or greater MLCC (X5R or better). |
| 44 | TMON0 | Input pin for external temperature measurement at Output 0. Supports diode based temperature sensing as well as smart power stage sensing. Refer to section "Temperature Compensation" on page 16 for more information. |
| 45 | TMON1 | Input pin for external temperature measurement at Output 1. Supports diode based temperature sensing as well as smart power stage sensing. Refer to section "Temperature Compensation" on page 16 for more information. |
| EPAD | GND | Package pad serves as GND return for all chip functions. Connect directly to system GND plane with multiple thermal vias. |

Driver, DrMOS, and Smart Power Stage Recommendation

| INTERSIL PART NUMBER | QUIESCENT CURRENT (mA) | GATE DRIVE VOLTAGE (V) | NUMBER OF DRIVERS | COMMENTS |
|----------------------|------------------------|------------------------|-------------------|---|
| ISL99227 | 4.85 | 5 | Single | 60A, 5x5 smart power stage |
| ISL99140 | 0.19 | 5 | Single | 40A, 6x6 DrMOS |
| ISL6596 | 0.19 | 5 | Single | Connect ISL6596 VCTRL to 3.3V |
| ISL6617A | 5 | N/A | N/A | Phase doubler with 5V PWM output to be compatible with a 60A DrMOS or with 60A smart power stage. Supports up to a 14-phase design. |

Internal Block Diagram

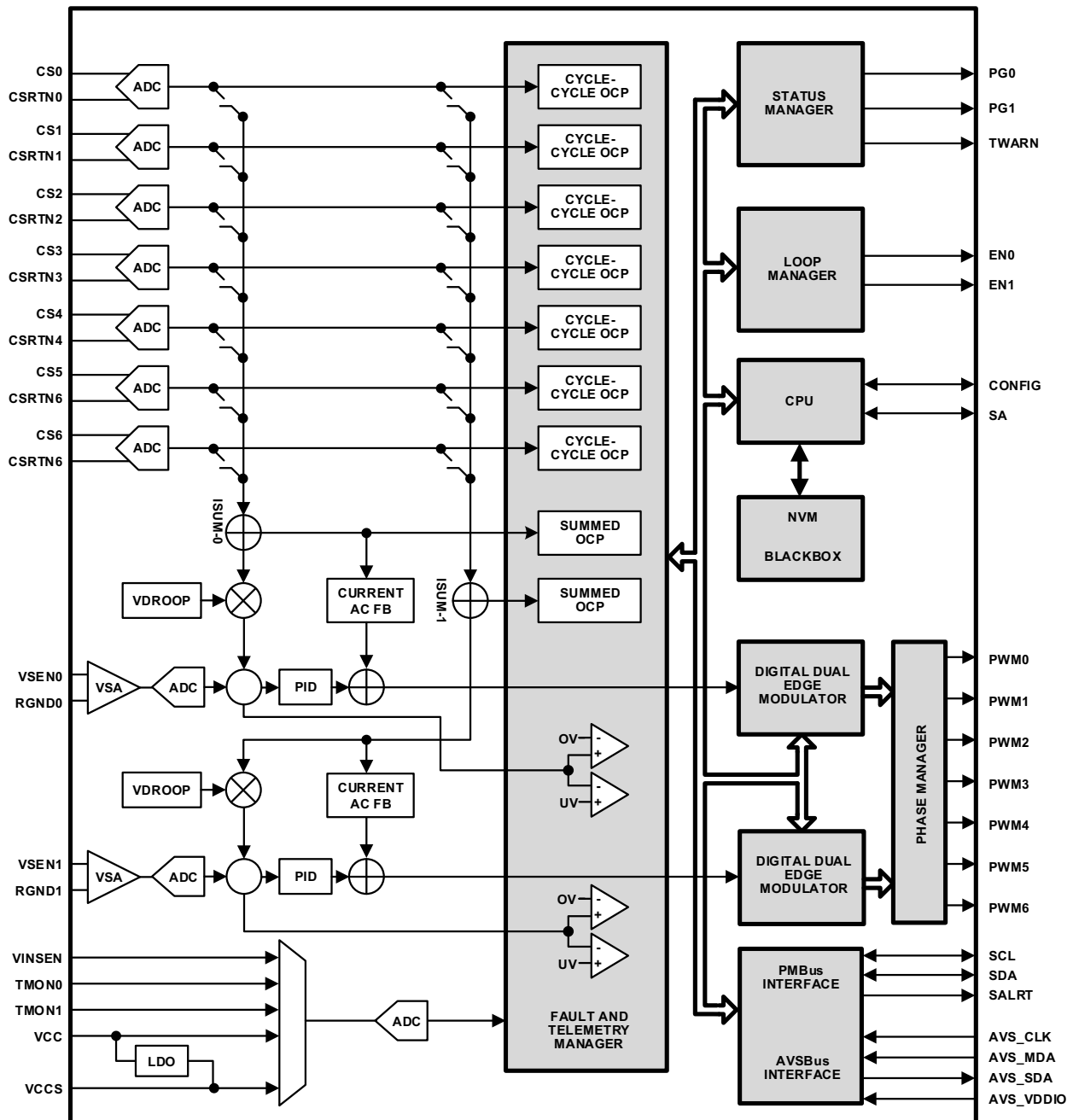


FIGURE 1. INTERNAL BLOCK DIAGRAM

Typical Application: 6+1 Configuration with ISL99227 SPS

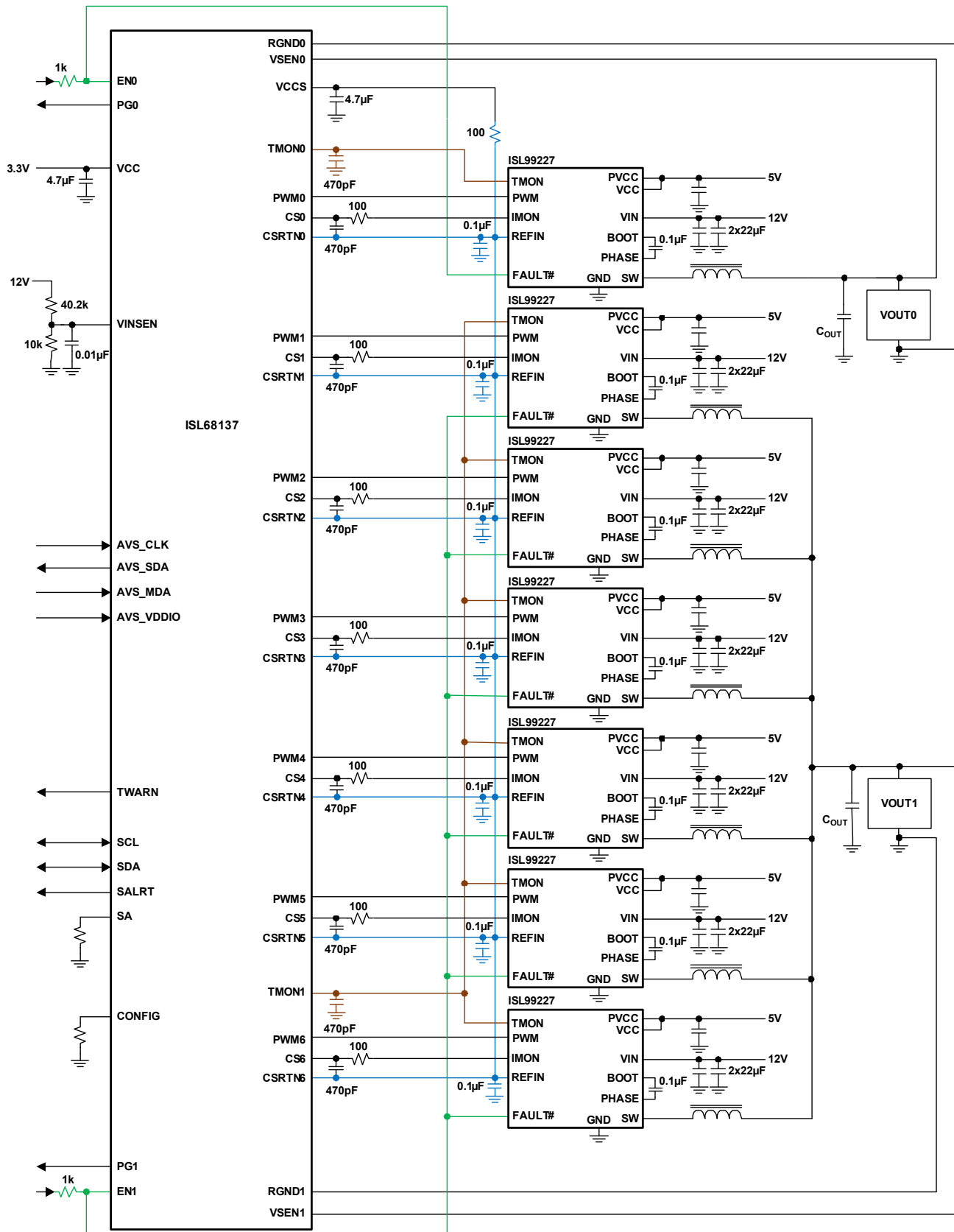


FIGURE 2. TYPICAL APPLICATION: 6+1 CONFIGURATION WITH ISL99227 SPS

Typical Application: 4+3 Configuration with ISL99227 SPS

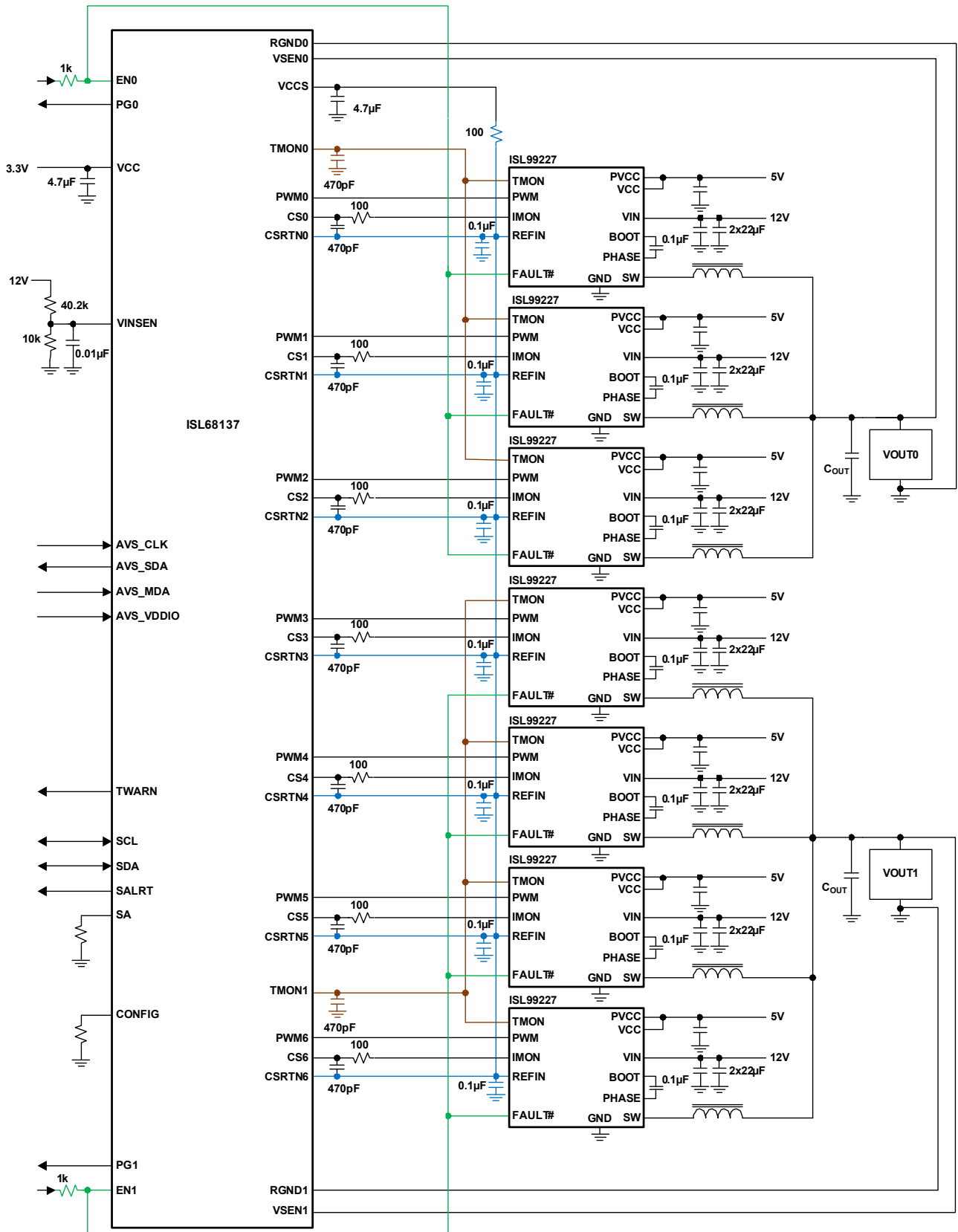


FIGURE 3. TYPICAL APPLICATION: 4+3 CONFIGURATION WITH ISL99227 SPS

Typical Application: 5+2 Configuration with DCR Sensing

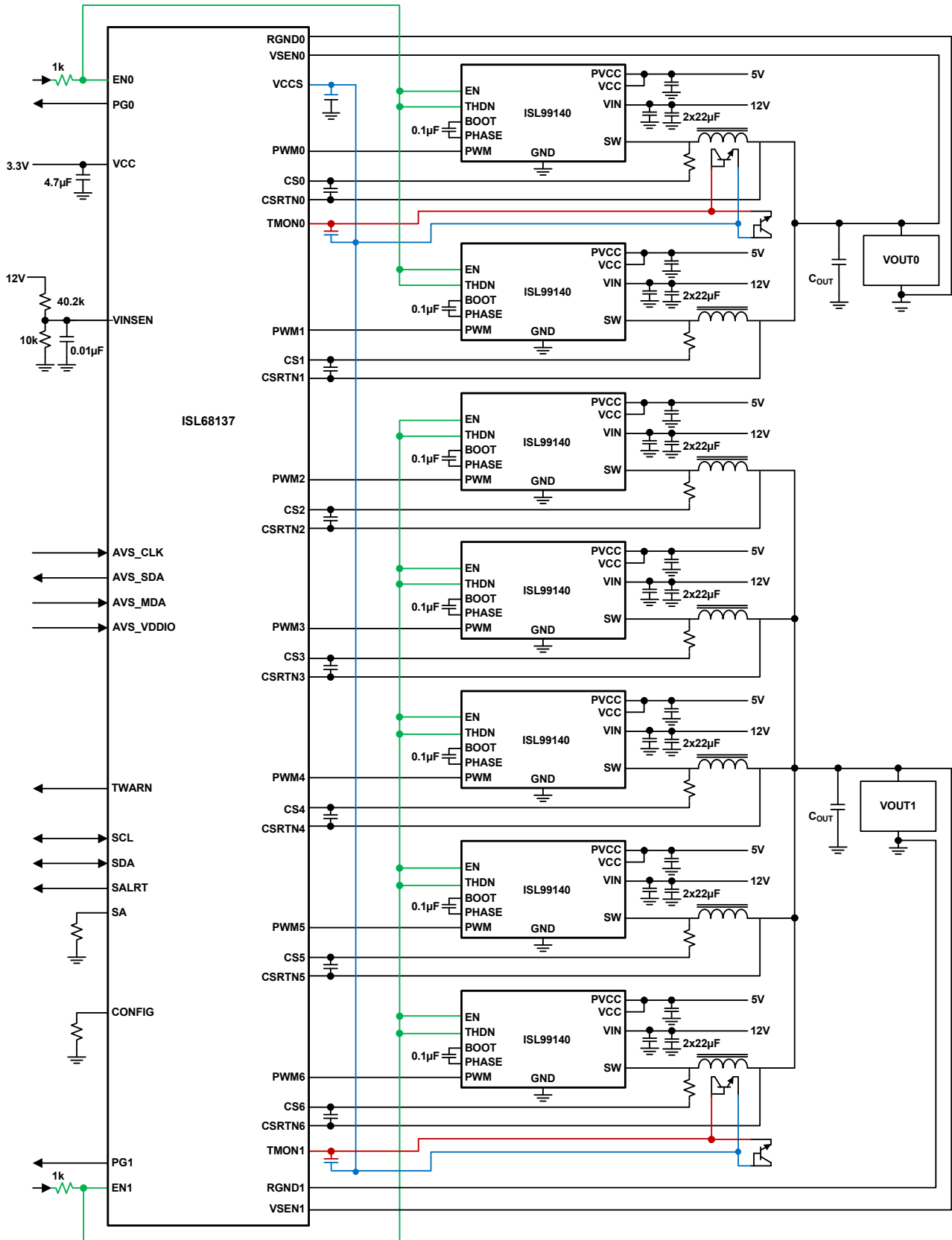


FIGURE 4. TYPICAL APPLICATION: 5+2 CONFIGURATION WITH DCR SENSING

Typical Application: Phase Doubler

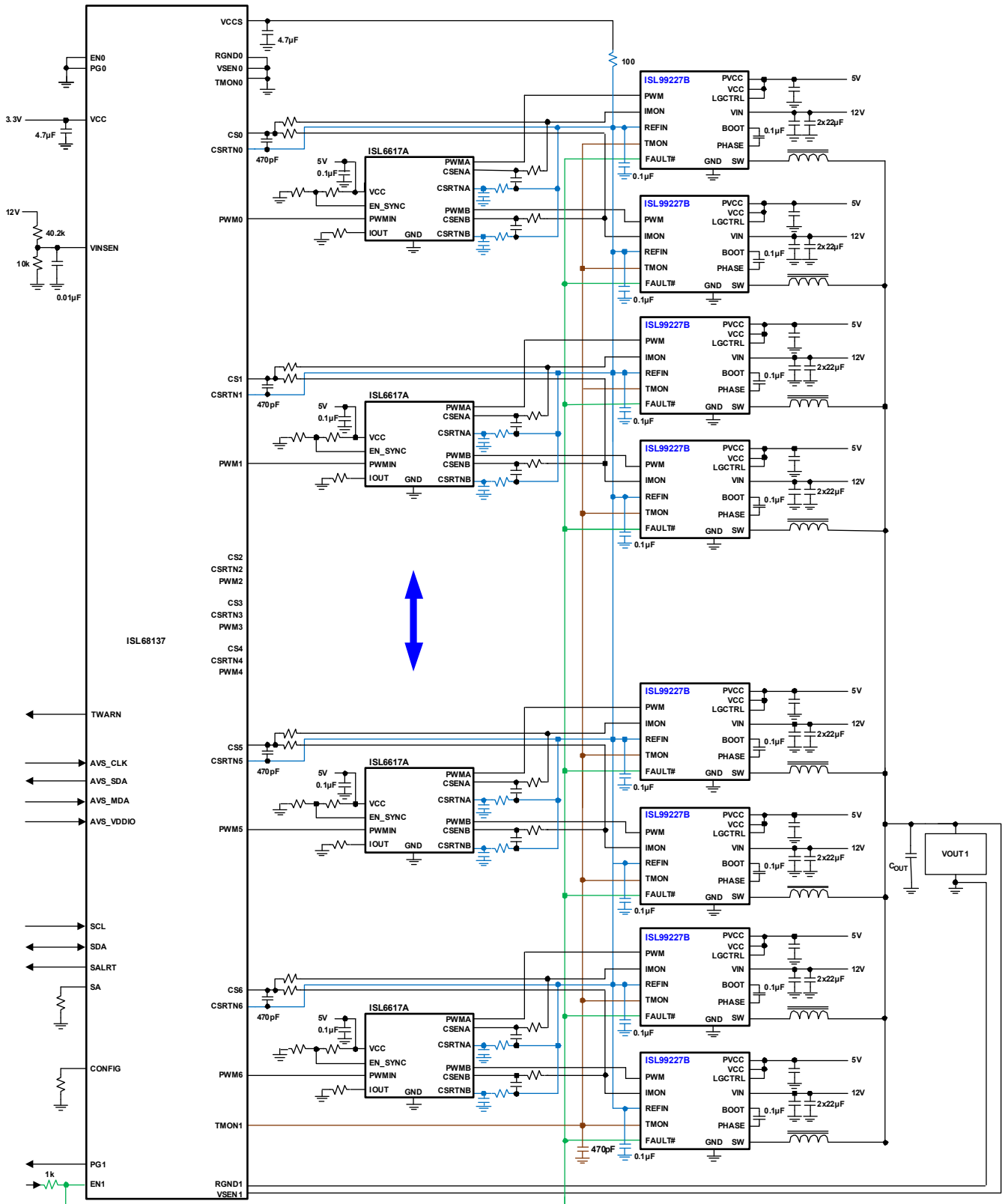


FIGURE 5. TYPICAL APPLICATION: PHASE DOUBLER

Absolute Maximum Ratings

| | |
|---|----------------------------|
| VCC | +4.3V |
| VCCS | +1.6V |
| All Other Pins | (GND - 0.3V) to VCC + 0.3V |
| ESD Rating: | |
| Human Body Model (Tested per JS-001-2014) | 2kV |
| Charged Device Model (Tested per JS-002-2014) | 1kV |
| Latch-Up (Tested per JEDEC-78E; Class 2, Level A) | 100mA |

Thermal Information

| | | |
|-----------------------------------|---------------------------|----------------------|
| Thermal Resistance (Notes 4, 5) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 48 Ld 6x6 QFN Package | 27 | 1 |
| Maximum Junction Temperature | +150°C | |
| Maximum Storage Temperature Range | -65°C to +150°C | |
| Pb-Free Reflow Profile | see TB493 | |

Recommended Operating Conditions

| | |
|---------------------|----------------|
| Supply Voltage, VCC | +3.3V ±5% |
| Ambient Temperature | -40°C to +85°C |
| Output Voltage | 0V to 3.05V |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See [TB379](#).
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications Recommended operating conditions, VCC = 3.3V, unless otherwise specified. **Boldface limits apply across the operating temperature range -40°C to +85°C.**

| PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|--|-----------------|-----------|-----------------|------|
| VCC SUPPLY CURRENT | | | | | |
| Nominal Supply Current | VCC = 3.3VDC; EN1/2 = VIH, fSW = 400kHz | | 90.5 | | mA |
| Shutdown Supply Current | VCC = 3.3VDC; EN1/2 = 0V, no switching | | 11.4 | | mA |
| VCCS LDO SUPPLY | | | | | |
| Output Voltage | | 1.20 | 1.25 | 1.30 | V |
| Maximum Current Capability | Excluding internal load | 50 | | | mA |
| POWER-ON RESET AND INPUT VOLTAGE LOCKOUT | | | | | |
| VCC Rising POR Threshold | | | 2.7 | 2.9 | V |
| VCC Falling POR Threshold | | 1.0 | | | V |
| Enable (EN0 and EN1) Input High Level | | 2.55 | | | V |
| Enable (EN0 and EN1) Input Low Level | | | | 0.8 | V |
| Enable (EN0 and EN1) LOW to HIGH Ramp Delay (TON_DELAY) | | 200 | | | µs |
| POR to Initialization Complete Time | | | 30 | 40 | ms |
| OUTPUT VOLTAGE CHARACTERISTICS (Note 6) | | | | | |
| Output Voltage Adjustment Range | | 0.25 | | 3.05 | V |
| Output Voltage Set-Point Accuracy | Set-point 0.8V to 3.05V | -0.5 | | 0.5 | % |
| | Set-point 0.25V to <0.8V | -5 | | 5 | mV |
| VOLTAGE SENSE AMPLIFIER | | | | | |
| Open Sense Current | Only during open pin check of initialization | | 22 | | µA |
| Input Impedance (VSEN - RGND) | | | 200 | | kΩ |
| Maximum Common-Mode Input | | | VCC - 0.2 | | V |
| Maximum Differential Input (VSEN - RGND) | | | | 3.05 | V |
| CURRENT SENSE AND OVERCURRENT PROTECTION | | | | | |
| Maximum Common-Mode Input (SPS mode) | CSRTNx - GND | | 1.6 | | V |
| Maximum Common-Mode Input (DCR mode) | CSRTNx - GND | | 3.3 | | V |

Electrical Specifications Recommended operating conditions, $V_{CC} = 3.3V$, unless otherwise specified. **Boldface limits apply across the operating temperature range $-40^{\circ}C$ to $+85^{\circ}C$.** (Continued)

| PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|--|---|------------------------------------|----------------|-----------------|-------------|
| Current Sense Accuracy | ISEN to ADC accuracy | -2 | | 2 | % |
| Average Overcurrent Threshold Resolution | | | 0.1 | | A |
| Cycle-by-Cycle Current Limiting Threshold Accuracy | | | 0.1 | | A |
| DIGITAL DROOP | | | | | |
| Droop Resolution | | | 0.01 | | mV/A |
| OSCILLATORS | | | | | |
| Accuracy of Switching Frequency Setting | When set to 500kHz | 480 | 500 | 520 | kHz |
| Accuracy of Switching Frequency Setting | | -4 | | 4 | % |
| Switching Frequency Range | | 0.2 | | 1.0 | MHz |
| SOFT-START RATE AND VOLTAGE TRANSITION RATE | | | | | |
| Minimum Soft-Start Ramp Rate | Programmable minimum rate | | 20 | | μs |
| Maximum Soft-Start Ramp Rate | Programmable maximum rate | | 10 | | ms |
| Soft-Start Ramp Rate Accuracy | | -4 | | 4 | % |
| Minimum Transition Rate | Programmable minimum rate | | 0.1 | | mV/ μs |
| Maximum Transition Rate | Programmable maximum rate | | 100 | | mV/ μs |
| Transition Rate Accuracy | | -4 | | 4 | % |
| PWM OUTPUT | | | | | |
| PWMx Output High Level | $I_{OUT} = 4mA$ | $V_{CC} - 0.4$ | | | V |
| PWMx Output Low Level | $I_{OUT} = 4mA$ | | | 0.4 | V |
| PWMx Output Tri-State I_{OL} | $V_{OH} = V_{CC}$ | | | 1 | μA |
| PWMx Output Tri-State I_{OH} | $V_{OL} = 0V$ | -1 | | | μA |
| THERMAL MONITORING AND PROTECTION | | | | | |
| Temperature Sensor Range | | -50 | | 150 | $^{\circ}C$ |
| Temperature Sensor Accuracy | TMON to ADC accuracy | -4.5 | | 4.5 | % |
| TWARN Output Low Impedance | | 4 | 9 | 13 | Ω |
| TWARN Hysteresis | | | 3 | | $^{\circ}C$ |
| POWER-GOOD AND PROTECTION MONITORS | | | | | |
| PG Output Low Voltage | $I_{OUT} = 8mA$ load | | | 0.4 | V |
| PG Leakage Current | With pull-up resistor externally connected to VCC | | 0.5 | 1.0 | μA |
| Overvoltage Protection Threshold Resolution | | | 1 | | mV |
| Undervoltage Protection Threshold Resolution | | | 1 | | mV |
| Overvoltage Protection Threshold when Disabled | | | $V_{CC} - 0.2$ | | V |
| INPUT VOLTAGE SENSE | | | | | |
| Input Voltage Accuracy | VINSEN to ADC accuracy | -2.5 | | 2.5 | % |
| Input Voltage Protection Threshold Resolution | | | 1 | | mV |
| AVSBus | | | | | |
| AVSBus VDDIO Input Voltage Range | | 0.90 | | 3.63 | V |
| AVSBus CLK, MDA, Input High Level | | $0.6 * V_{DDIO}$ | | | V |

Electrical Specifications Recommended operating conditions, $V_{CC} = 3.3V$, unless otherwise specified. **Boldface limits apply across the operating temperature range $-40^{\circ}C$ to $+85^{\circ}C$.** (Continued)

| PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|----------------------------------|-----------------|------------------------------------|-----|------------------------------------|------|
| AVSBus CLK, MDA, Input Low Level | | | | $0.4 * V_{DDIO}$ | V |
| AVSBus SDA, Output High Level | | $0.8 * V_{DDIO}$ | | | V |
| AVSBus SDA, Output Low Level | | | | $0.2 * V_{DDIO}$ | V |
| AVSBus CLK Maximum Frequency | | 50 | | | MHz |
| AVSBus CLK Minimum Frequency | | | | 5 | MHz |
| SMBus/PMBus | | | | | |
| SALERT, SDA Output Low Level | $I_{OUT} = 4mA$ | | | 0.4 | V |
| SCL, SDA Input High Level | | 1.55 | | | V |
| SCL, SDA Input Low Level | | | | 0.8 | V |
| SCL, SDA Input Hysteresis | | | 2 | | mV |
| SCL Maximum Frequency | | 0.05 | | 2.00 | MHz |

NOTES:

- 6. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
- 7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Curves

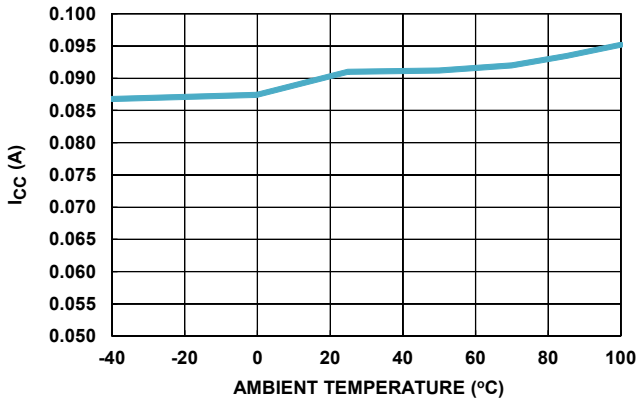


FIGURE 6. NOMINAL SUPPLY CURRENT vs TEMPERATURE

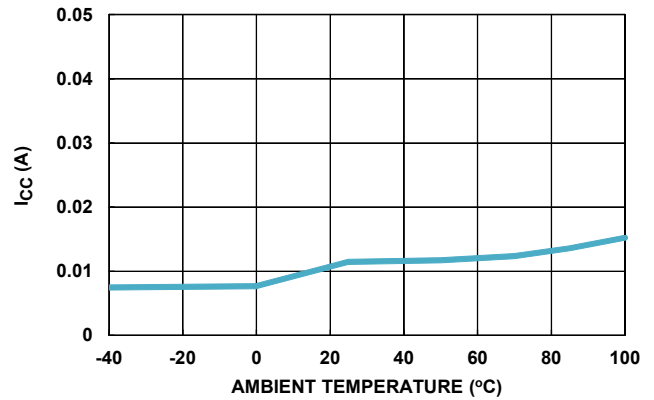


FIGURE 7. SHUTDOWN SUPPLY CURRENT vs TEMPERATURE

Functional Description

Overview

The ISL68137 is a digital dual output 7-phase PWM controller that can be programmed for single output 7+0, dual output 6+1, 5+2, or 4+3 phase operation. Operation using less than seven phases between two outputs is also supported. Existing digital multiphase solutions use analog comparator based schemes (nonlinear) to bolster the inadequate transient response common to many digital multiphase solutions. The ISL68137 uses a linear voltage regulation scheme to address transient loads. As a result, it is much easier for users to configure and validate their designs when compared with nonlinear schemes. By combining a proprietary low noise and zero latency digital current sense scheme with cutting edge digital design techniques, Intersil is able to meet transient demands without resorting to nonlinear schemes. In addition, the ISL68137 can store up to eight user configurations in NVM and allows the user to select the desired configuration through pin-strap (CONFIG). The result is a system that is easy to configure and deploy.

The ISL68137 supports several performance enhancing features. These include AVSBus control, diode braking, automatic phase dropping, DCR/resistor/smart power stage current sense support, load line regulation, and multiple temperature sensing options.

To facilitate configuration development, the PowerNavigator GUI provides a step-by-step arrangement for setup and parametric adjustment. After a configuration has been set, the user can employ PowerNavigator to monitor telemetry or use the PMBus interface directly based on the supported command set.

PWM Modulation Scheme

The ISL68137 uses Intersil's proprietary linear synthetic current modulation scheme to improve transient performance. This is a unique constant frequency, dual edge PWM modulation scheme with both PWM leading and trailing edges being independently moved to give the best response to transient loads. Current balance is an inherent part of the regulation scheme. The modulation scheme is capable of overlapping pulses if the load profile demands such operation. In addition, the modulator is capable of adding or removing pulses from a given cycle in response to regulation demands while still managing maximum average frequency to safe levels. For DC load conditions the operating frequency is constant.

PMBus Address Selection

When communicating with multiple PMBus devices on a single bus, each device must have its own unique address so the host can distinguish between the devices. The device address can be set using a 1% resistor on the SA pin according to the pin-strap options listed in [Table 2](#).

TABLE 2. RESISTOR VALUES TO ADDRESS MAPPING

| R SA (Ω) | PMBus ADDRESS | R SA (Ω) | PMBus ADDRESS |
|----------|---------------|----------|---------------|
| 0 | 60h | 1500 | 50h |
| 180 | 61h | 1800 | 51h |
| 330 | 64h | 2200 | 54h |
| 470 | 65h | 2700 | 55h |
| 680 | 40h | 3300 | 58h |
| 820 | 41h | 3900 | 59h |
| 1000 | 44h | 4700 | 5Ch |
| 1200 | 45h | 5600 | 5Dh |

Phase Configuration

The ISL68137 supports up to two regulated outputs through seven configurable phases. Either output is capable of controlling up to seven phases in any arbitrary mix. Phase assignments are accomplished through the PowerNavigator GUI.

Although the device supports arbitrary phase assignment, it is good practice to assign phases to Output 1 in descending sequential numerical order starting from Phase 6. For example, a 4-phase rail could consist of phases 6, 5, 4, and 3. For Output 0, phases would be assigned starting from Phase 0 in ascending sequential numerical order.

Automatic Phase Add and Drop

To produce the most optimal efficiency across a wide range of output loading, the modulator supports automatic dropping or adding of phases. Use of automatic phase dropping is optional. If automatic phase dropping is enabled, the number of active phases at any time is determined solely by load current. During operation, phases of Output 1 will drop beginning with the lowest phase number assigned. Phase dropping begins with the highest assigned phase number. [Figure 8](#) illustrates the typical characteristic of efficiency vs load current vs phase count.

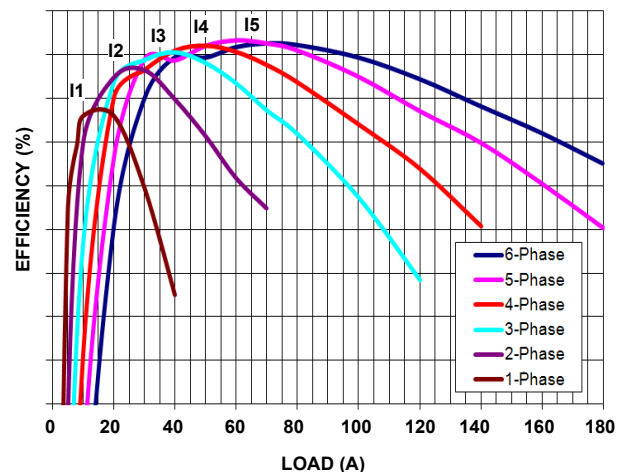


FIGURE 8. EFFICIENCY vs PHASE NUMBER

Phases are dropped one at a time with a user programmed drop delay between drop events. As an example, suppose the delay is set to 1ms and three phases are active. If the load suddenly drops to a level needing only one phase, the ISL68137 will begin by dropping a phase after 1ms. An additional phase will be dropped each 1ms thereafter until only one phase remains.

In addition to the described load current add/drop thresholds, the fast phase add function provides a very rapid response to transient load conditions. This feature continuously monitors the system regulation error and if it exceeds the user set threshold, all dropped phases will be readied for use. In this way, there is no delay if all phases are needed to support a load transient. The fast phase add threshold is set in the PowerNavigator GUI. The output current threshold for adding and dropping phases can also be configured.

To ensure dropped phases have sufficient boot capacitor charge to turn on the high-side MOSFET after a long period of disable, a boot refresh circuit turns on the low-side MOSFET of each dropped phase to refresh the boot capacitor. The frequency of the boot refresh is programmable using PowerNavigator.

Output Voltage Configuration

Output voltage set points and thresholds for each output can be configured with the PowerNavigator GUI. Parameters such as output voltage, V_{OUT} margin high/low, and V_{OUT} OV/UV fault thresholds can be configured with the GUI. Additionally, output voltage and margin high/low can be adjusted during regulation using PMBus command $V_{OUT_COMMAND}$, $V_{OUT_MARGIN_HIGH}$, and $V_{OUT_MARGIN_LOW}$ for further tuning. The following V_{OUT} relationships must be maintained for correct operation:

$V_{OUT_OV_FAULT_LIMIT} > V_{OUT_COMMAND}$
 ($V_{OUT_MARGIN_HIGH}$ and $V_{OUT_MARGIN_LOW}$, if used) $>$
 $V_{OUT_UV_FAULT_LIMIT}$. Additionally, the V_{OUT} commands are bounded by V_{OUT_MAX} and V_{OUT_MIN} to provide protection against incorrect set points being sent to the device. The ISL68137 also incorporates AVSBus functionality for high speed changes to the V_{OUT} target.

Switching Frequency

The switching frequency is user configurable over a range of 200kHz to 1MHz.

Current Sensing

The ISL68137 supports DCR, resistor, and smart power stage current sensing. Connection to the various sense elements is accomplished through the CS and CSRTN pins. Current sensing inputs are high impedance differential inputs to reject noise and ground related inaccuracies.

To accommodate a wide range of effective sense resistance, information about the effective sense resistance and required per phase current capability is used by the GUI to properly configure the current sense circuitry.

INDUCTOR DCR SENSING

DCR sensing takes advantage of the fact that an inductor winding has a resistive component (DCR) that will drop a voltage proportional to the inductor current. [Figure 9](#) shows that the DCR is treated as a lumped element with one terminal inaccessible for measurement. Fortunately, a simple R-C network as shown in [Figure 10](#) is capable of reproducing the hidden DCR voltage. By simply matching the R-C time constant to the L/DCR time constant, it is possible to precisely recreate the DCR voltage across the capacitor. This means that $V_{DCR}(t) = V_C(t)$, thus preserving even the high frequency characteristic of the DCR voltage.

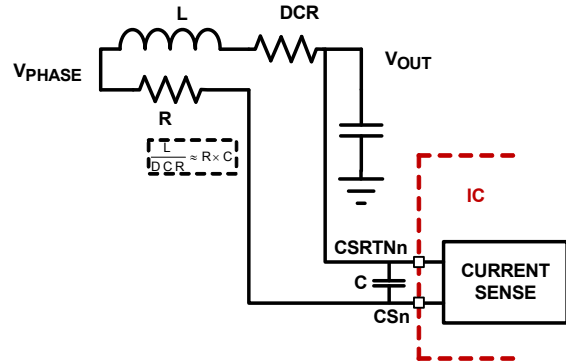


FIGURE 9. DCR SENSING CONFIGURATION

Modern inductors often have such low DCR values that the resulting signal is $<10\text{mV}$. To avoid noise problems, care must be taken in the PCB layout to properly place the R-C components and route the differential lines between controller and inductor.

[Figure 9](#) shows one PCB design method that places the R component near the inductor VPHASE and the C component very close to the IC pins. This minimizes routing of the noisy VPHASE and maximizes filtering near the IC. Route the lines between the inductor and IC as a pair on a single layer directly to the controller. Care must be taken to avoid routing the pair near any switching signals including Phase, PWM etc. This is the method used by Intersil on evaluation board designs.

This method is sensing the resistance of a metal winding in which the DCR value will increase with temperature. This must be compensated or the sensed (and reported) current will increase with temperature. To compensate the temperature effect, the ISL68137 provides temperature sensing options and an internal methodology to apply the correction.

RESISTIVE SENSING

For more accurate current sensing, a dedicated current sense resistor R_{SENSE} in series with each output inductor can serve as the current sense element. This technique, however, reduces the overall converter efficiency due to the additional power loss on the current sense element R_{SENSE} .

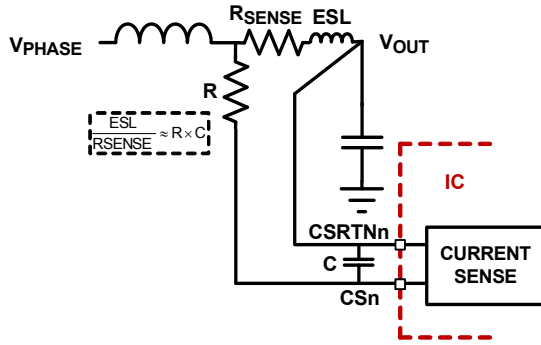


FIGURE 10. SENSE RESISTOR IN SERIES WITH INDUCTOR

A current sensing resistor has a distributed parasitic inductance, known as Equivalent Series Inductance (ESL), typically less than 4nH. Consider the ESL as a separate lumped quantity, as shown in Figure 10. The phase current I_L , flowing through the inductor, will also pass through the ESL. Similar to DCR sensing described previously, a simple R-C network across the current sense resistor extracts the R_{SENSE} voltage. Simply match the ESL/R_{SENSE} time constant to the R-C time constant.

Figure 11 shows the sensed waveforms with and without matching RC when using resistive sense. PCB layout should be treated similar to that described for DCR sense.

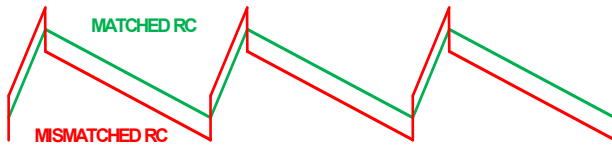


FIGURE 11. VOLTAGE ACROSS R WITH AND WITHOUT RC

L/DCR OR ESL/R_{SEN} MATCHING

Assuming the compensator design is correct, Figure 12 shows the expected load transient response waveforms if L/DCR or ESL/R_{SEN} is matching the R-C time constant. When the load current I_{OUT} has a square change, the output voltage V_{OUT} also has a square response, except for the potential overshoot at load release. However, there is always some uncertainty in the true parameter values involved in the time constant matching and therefore, fine-tuning is generally required.

If the R-C time constant is too large or too small, $V_C(t)$ will not accurately represent real-time $I_{OUT}(t)$ and will worsen the transient response. Figure 13 shows the load transient response when the R-C timing constant is too small. In this condition, V_{OUT} will sag excessively upon load insertion and may create a system failure or early overcurrent trip. Figure 14 shows the transient response when the R-C timing constant is too large. V_{OUT} is sluggish in drooping to its final value. Use these general guides if fine-tuning is needed.

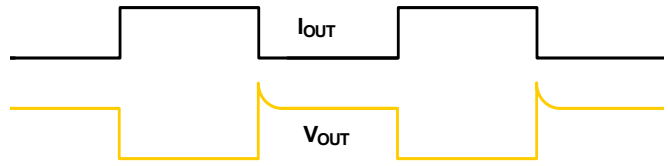


FIGURE 12. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

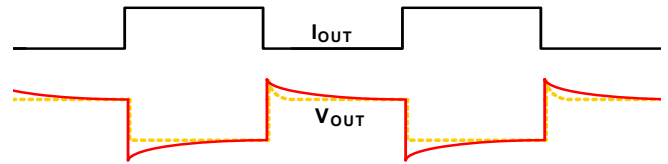


FIGURE 13. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL

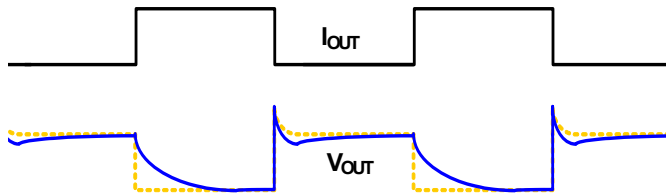


FIGURE 14. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

SPS CURRENT SENSING

SPS current sense is accomplished by sensing each SPS IMON output individually using VCCS as a common reference. Connect all SPS IREF input pins and all ISL68137 CSRTNn input pins together and tie them to VCCS, then connect the SPS IMONn output pins to the corresponding ISL68137 CSn input pins. The signals should be run as differential pairs from the SPS back to the ISL68137.

Temperature Sensing

The ISL68137 supports temperature sensing through BJT or smart power stage sense elements. Support for BJT sense elements uses the well known delta Vbe method and allows up to two sensors (MMBT3906 or similar) on each temperature sense input, TMON0 and TMON1. Support for smart power stage uses a linear conversion algorithm and allows one sensor reading per pin. The conversion from voltage to temperature for smart power stage sensing is user programmable using the PowerNavigator GUI.

SPS temperature sensing measures the temperature dependent voltage output on the SPS TMON pin. All of the SPS devices attached to the Output 0 rail have their TMON pins connected to the ISL68137 TMON0 pin. All of the SPS devices attached to the Output 1 rail have their TMON pins connected to the ISL68137 TMON1 pin. The reported temperature is that of the highest temperature SPS of the group.

In addition to the external temperature sense, the IC senses its own die temperature, which can be monitored using PowerNavigator.

Sensed temperature is used in the system for faults, telemetry and temperature compensation of sensed current.

Temperature Compensation

The ISL68137 supports inductor DCR sensing, which generally requires temperature compensation due to the copper wire used to form inductors. Copper has a positive temperature coefficient of approximately 0.39%/°C. Because the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR.

Compensating current sense for temperature variation generally requires that the current sensing element temperature and its temperature coefficient is known. Although temperature coefficient is generally obtained easily, the actual current sense element temperature is essentially impossible to measure directly. Instead, a temperature sensor (a BJT for the ISL68137) placed near the inductors is measured and the current sense element (DCR) temperature is calculated from that measurement. Calculating current sense element temperature is equivalent to applying gain and offset corrections to the temperature sensor measurement and the ISL68137 supports both corrections.

Figure 15 depicts the block diagram of temperature compensation. A BJT placed near the inductors used for DCR sensing is monitored by the IC using the well known delta Vbe method of temperature sensing. T_{SENSE} is the direct measured temperature of the BJT. Because the BJT is not directly sensing DCR, corrections must be made so that T_{DCR} reflects the true DCR temperature. Corrections are applied according to the relationship shown in Equation 1, where k_{SLOPE} represents a gain scaling and T_{OFFSET} represents an offset correction. These parameters are provided by the designer using the PowerNavigator GUI:

$$T_{DCR} = k_{SLOPE} \cdot T_{SENSE} + T_{OFFSET} \tag{EQ. 1}$$

After T_{DCR} has been determined, the compensated DCR value can be determined according to Equation 2, where DCR₂₅ is the DCR at +25°C and T_C is the temperature coefficient of copper (3900 ppm/°C). T_{DCR} = T_{ACTUAL} here:

$$DCR_{CORR} = DCR_{25} \cdot (1 + T_C \cdot (T_{ACTUAL} - 25)) \tag{EQ. 2}$$

Thus, the temperature-compensated DCR is now used to determine the actual value of current in the DCR sense element.

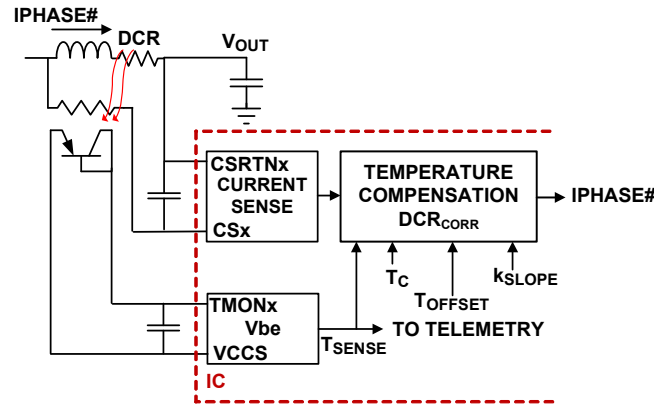


FIGURE 15. BLOCK DIAGRAM OF TEMPERATURE COMPENSATION

In the physical PCB design, the temperature sense diode (BJT) is placed close to the inductor of the phase that is never dropped during automatic phase drop operation. Additionally, a filter capacitor no larger than 500pF should be added near the IC between each TMON pin and VCCS. This is shown in Figure 16.

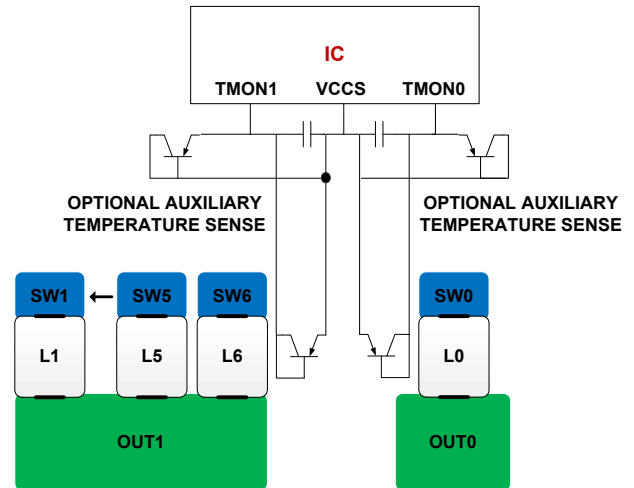


FIGURE 16. RECOMMENDED PLACEMENT OF BJT

Lossless Input Current and Power Sensing

Input current telemetry is provided using an input current synthesizer. By using the IC's ability to precisely determine its operational conditions, input current can be synthesized to a high degree of accuracy without the need for a lossy sense resistor. Fine-tuning of offset and gain are provided for in the GUI. Note that input current sense fine-tuning must be done after output current sense setup is finalized. With a precise knowledge of input current and voltage, input power can be computed.

Input current and power telemetry is accessed using PMBus and easily monitored in the PowerNavigator GUI. V_{IN} is monitored directly by the VINSEN pin through a 1:5 resistor divider as shown in Figure 17.

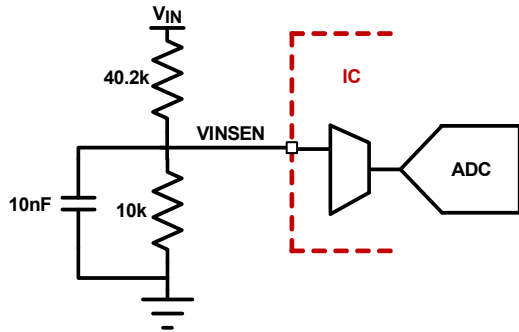


FIGURE 17. INPUT VOLTAGE SENSE CONFIGURATION

Voltage Regulation

Output voltage is sensed through the remote sense differential amplifier and digitized. From this point, the regulation loop is entirely digital. Traditional PID controls are used in conjunction with several enhanced methods to compensate the voltage regulation loop and tune the transient response.

Current Feedback

Current feedback in a voltage regulator is often used to ease the stability design of the voltage feedback path. Additionally, many microprocessors require the voltage regulator to have a controlled output resistance (known as load-line or droop regulation) and this is accomplished using current feedback.

For applications requiring droop regulation, the designer simply specifies the output resistance desired using the PowerNavigator GUI.

Current feedback stability benefits are available for rails that do not specify droop regulation such as system agent. For these applications, the designer can enable AC current feedback in the GUI. With this configuration, the DC output voltage will be steady regardless of load current.

Power-On Reset (POR)

Initialization of the ISL68137 begins after V_{CC} crosses its rising POR threshold. When POR conditions are met, the internal 1.2V LDO is enabled and basic digital subsystem integrity checks begin. During this process, the controller will load the selected user configuration from NVM as indicated by the CONFIG pin resistor value, read VIN UVLO thresholds from memory and start the telemetry subsystem. With telemetry enabled, V_{IN} can be monitored to determine when it exceeds its user programmable rising UVLO threshold. When V_{CC} and V_{IN} satisfy their respective voltage conditions, the controller is in its shutdown state. It will transition to its active state and begin soft-start when the state of EN0/EN1 command a start-up. While in shutdown mode, the PWM outputs are held in a high-impedance state to ensure the drivers remain off.

Soft-Start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for an output to ramp to its target value after the delay period has expired. These features can be used as part of an

overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ISL68137 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp-up/down times can be configured using PowerNavigator GUI. The device needs approximately 200 μ s after enable to initialize before starting to ramp up. When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is recommended to set the ramps to a non-zero value to prevent inadvertent fault conditions due to excessive inrush current.

Stored Configuration Selection

As many as eight configurations can be stored and used at any time using the on-board nonvolatile memory. Configurations are assigned an identifier number between 0 and 7 at power-up. The device will load the configuration indicated by the 1% resistor value detected on the CONFIG pin. Resistor values are used to indicate use of one of the eight possible configurations. [Table 3](#) shows the resistor value corresponding to each configuration identifier.

TABLE 3. RESISTOR VALUES TO CONFIGURATION MAPPING

| R CONFIG (Ω) | CONFIG ID |
|--------------------------|--------------|
| 6800 | 0 |
| 1800 | 1 |
| 2200 | 2 |
| 2700 | 3 |
| 3300 | 4 |
| 3900 | 5 |
| 4700 | 6 |
| 5600 | 7 |

Only the most recent configuration with a given number can be loaded. The device supports a total of eight stored operations. As an example, a configuration with the identifier 0 could be saved eight times or configurations with all eight identifiers could be stored one time each for a total of eight save operations.

PowerNavigator provides a simple interface to save and load configurations.

Fault Monitoring and Protection

The ISL68137 actively monitors temperature, input voltage, output voltage, and output current to detect and report fault conditions. Fault monitors trigger configurable protective measures to prevent damage to a load. The power-good indicators, PG0/PG1, are provided for linking to external system monitors.

A high level of flexibility is provided in the ISL68137 fault logic. Faults can be enabled or disabled individually. Each fault type can also be configured to either latch off or retry indefinitely.

Power-Good Signals

The PGO/PG1 pins are open-drain, power-good outputs that indicate completion of the soft-start sequence and output voltage of the associated rail within the expected regulation range.

The PG pins can be associated or disassociated with a number of the available fault types. This allows a system design to be tailored for almost any condition. In addition, these power-good indicators will be pulled low when a fault (OCP or OVP) condition or UV condition is detected on the associated rail.

Output Voltage Protection

Output voltage is measured at the load sensing points differentially for regulation and the same measurement is used for OVP and UVP. The fault thresholds are set using PMBus commands. Figure 18 shows a simplified OVP/UVP block diagram. The output voltage comparisons are done in the digital domain.

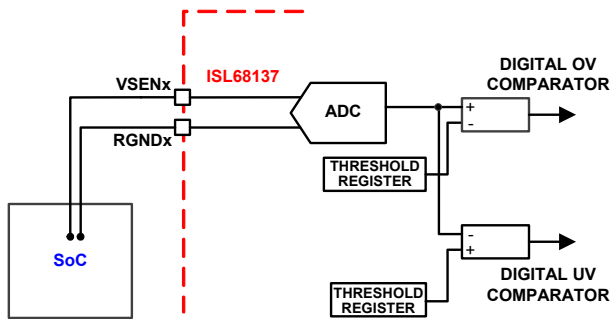


FIGURE 18. OVP, UVP COMPARATORS

The device responds to an output overvoltage condition by disabling the output, declaring a fault, setting the SALRT pin, setting the PG pin and then pulsing the LFET until the output voltage has dropped below the threshold. Similarly, the device responds to an output undervoltage condition by disabling the output, declaring a fault, setting the SALRT pin and setting the PG pin. The output will not restart until the EN pin is cycled (unless the device is configured to retry).

In addition, the ISL68137 features open pin sensing protection to detect an open of the output voltage sensing circuit. When this condition is detected, controller operation is suspended.

Output Current Protection

The ISL68137 offers a comprehensive overcurrent protection scheme. Each phase is protected from both excessive peak current and sustained current. In addition, the system is protected from sustained total output overcurrent.

Figure 19 depicts a block diagram of the system total output current protection scheme. In this scheme, the phase currents are summed to form ISUM. ISUM is then fed to dual response paths allowing the user to program separate LPF, threshold and response time. One path is intended to allow response more quickly than the other path. With this system, the user can allow high peak total current for a short time and a lower level of current for a sustained time. Note that neither of these paths affect PWM activity on a cycle-by-cycle basis. The characteristics of each path are easily set in PowerNavigator.

In addition to total output current, the ISL68137 provides an individual phase peak current limit that will act on PWM in a cycle-by-cycle manner. This means that if a phase current is detected to exceed the OC threshold, the phase PWM signal will be inverted to move current away from the threshold. In addition to limiting positive or negative peak current on a cycle-by-cycle basis, individual phase OC can be configured to limit current indefinitely or to declare a fault after a programmable number of consecutive OC cycles. This feature is useful for applications in which a fault shutdown of the system would not be acceptable but some ability to limit phase currents is desired. Figures 22 and 23 on page 19 depict this operation. If configured for indefinite current limit, the converter will act as a current source and V_{OUT} will not remain at its regulation point. It should be noted that in this case, V_{OUT} OV or UV protection action may occur, which could shut the regulator down.

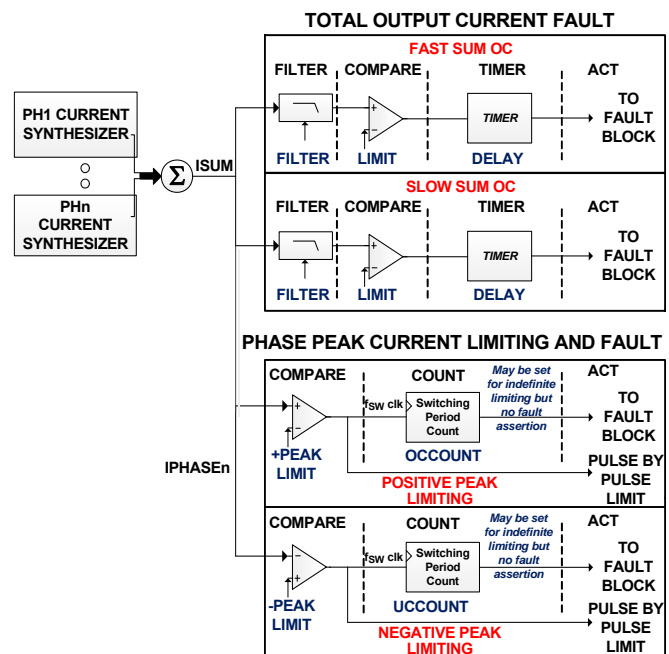


FIGURE 19. OCP FUNCTIONAL DIAGRAM

An example of the OCP_Fast and OCP_Slow waveforms are shown in [Figures 20](#) and [21](#).

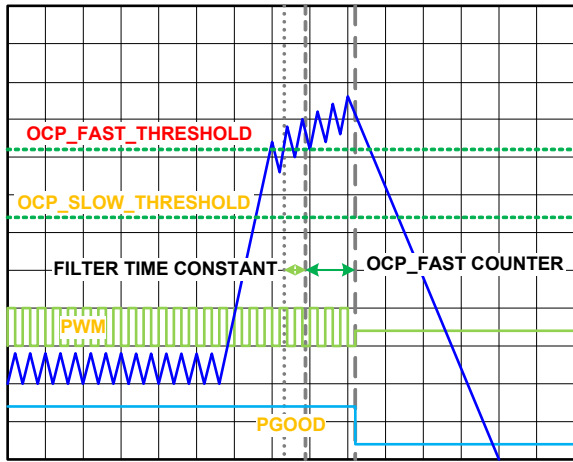


FIGURE 20. OCP_FAST

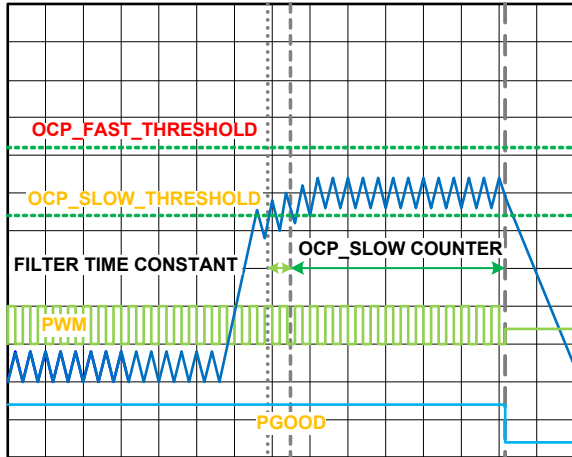


FIGURE 21. OCP_SLOW

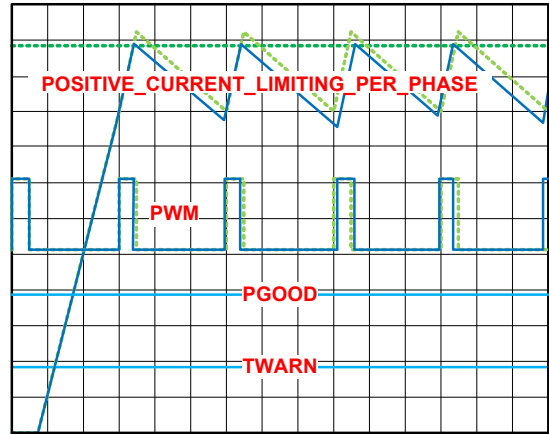


FIGURE 22. POSITIVE PEAK PHASE CURRENT LIMITING

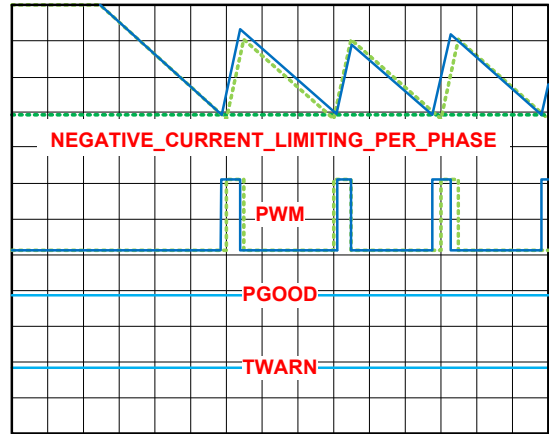


FIGURE 23. NEGATIVE PEAK PHASE CURRENT LIMITING

Smart Power Stage OC Fault Detect

Intersil Smart Power Stage (SPS) devices will output a large signal on their IMON lines if peak current exceeds their preprogrammed threshold. (For more detail about this functionality, refer to the relevant SPS datasheet.) The ISL68137 is equipped to detect this fault flag and immediately shut down. This detector is enabled on the GUI Overcurrent Fault setup screen.

This feature functions by detecting signals that exceed the current sense ADC full-scale range. If this detector is disabled while using an Intersil SPS, the SPS Fault# signal must be connected to the controller Enable pin of the associated rail. This will ensure that an SPS OC event will be detected and the converter will shut down.

Thermal Monitoring and Protection

The TWARN pin indicates the temperature status of the voltage regulator. The TWARN pin is an open-drain output and an external pull-up resistor is required. This signal is valid only after the controller is enabled.

The TWARN signal can be used to inform the system that the temperature of the voltage regulator is too high and the load should reduce its power consumption. TWARN only indicates a thermal warning, not a fault.

The thermal monitoring function block diagram is shown in [Figure 24](#). The ISL68137 has two over-temperature thresholds, which allow both warning and fault indications. Each temperature sensor threshold can be independently programmed in the PowerNavigator GUI. [Figure 25](#) shows the thermal warning to TWARN and [Figure 26](#) shows the over-temperature fault to shutdown. PGOOD and TWARN can be configured to indicate these warning and fault thresholds using the PowerNavigator GUI.

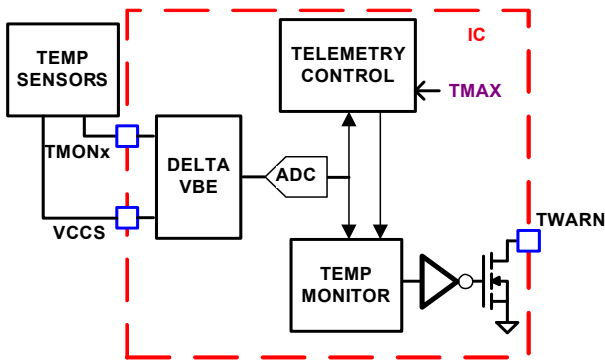


FIGURE 24. BLOCK DIAGRAM OF THERMAL MONITORING FUNCTION

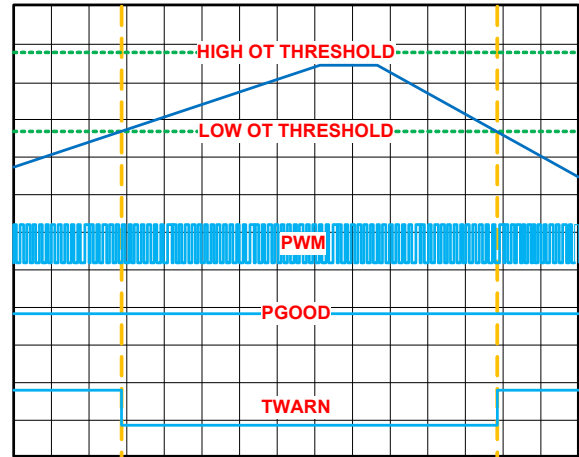


FIGURE 25. THERMAL WARNING TO TWARN

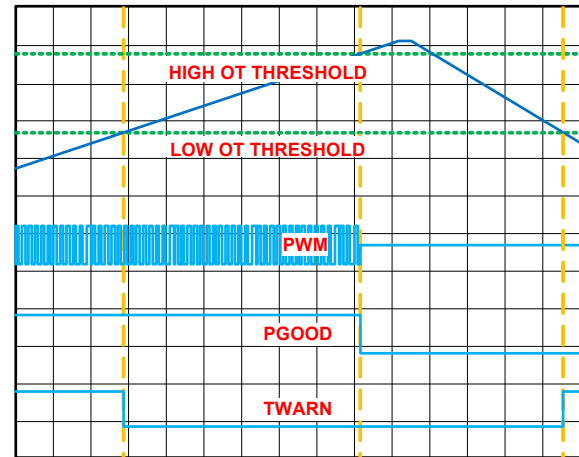


FIGURE 26. OVER-TEMPERATURE FAULT

Layout and Design Considerations

In addition to [TB379](#), the following PCB layout and design strategies are intended to minimize the noise coupling, the impact of board parasitic impedances on converter performance, and to optimize the heat dissipating capabilities of the printed circuit board. This section highlights some important practices, which should be followed during the layout process.

[Table 4](#) provides general guidance on best practices related to pin noise sensitivity. Use of good engineering judgment is required to implement designs based on criteria specific to the situation.

TABLE 4. PIN DESIGN AND/OR LAYOUT CONSIDERATIONS

| PIN NAME | NOISE SENSITIVE | DESCRIPTION |
|---------------------------------|-----------------|--|
| VINSEN | Yes | Connects to the resistor divider between VIN and GND (see Figure 17 on page 17). Filter VINSEN with 10nF to GND. |
| RGNDx VSENx | Yes | Treat each of the remote voltage sense pairs as differential signals in the PCB layout. They should be routed side by side on the same layer. They should not be routed in proximity to noisy signals like PWM or Phase. Tie to ground when not used. |
| PGx | No | Open-drain. 3.3V maximum pull-up voltage. Tie to ground when not used. |
| SCL, SDA, SALRT | Yes | 50kHz to 2MHz signal during communication, pair up with SALRT and route carefully. 20 mils spacing within SDA, SALRT, and SCL; and more than 30 mils to all other signals. Refer to the SMBus design guidelines and place proper termination resistance for impedance matching. Tie to ground when not used. |
| AVS_CLK, AVS_SDA, AVS_MDA | Yes | Up to 50MHz signals during communication, route carefully. 20 mils spacing within CLK, SDA, and MDA; and more than 30 mils to all other signals. Tie CLK and MDA to ground when not used. |
| TMONx | Yes | When diode sensing is used, VCCS is the return path for the delta Vbe currents. Use a separate VCCS route specifically for diode temp sense. A filter capacitor no greater than 500pF should be placed between each TMON pin and the VCCS pin near the IC. Tie to ground when not used. |
| TWARN | No | Open-drain. 3.3V maximum pull-up voltage. |
| VCC | Yes | Place at least 2.2µF MLCC decoupling capacitor directly at the pin. |
| VCCS | Yes | Place 4.7µF MLCC decoupling capacitor directly at the pin. |
| PWM | No | Avoid routing near noise sensitive analog lines such as current sense or voltage sense. |

TABLE 4. PIN DESIGN AND/OR LAYOUT CONSIDERATIONS (Continued)

| PIN NAME | NOISE SENSITIVE | DESCRIPTION |
|------------------|-----------------|--|
| CSx CSRTNx | Yes | Treat each of the current sense pairs as differential signals in the PCB layout. They should be routed side by side on the same layer. They should not be routed in proximity to noisy signals like PWM or Phase. Proper routing of current sense is perhaps the most critical of all the layout tasks. Tie to ground when not used. |
| GND | Yes | This EPAD is the return of PWM output drivers. Use four or more vias to directly connect the EPAD to the power ground plane. |
| General Comments | | The layer next to the top or bottom layer is preferred to be ground layers, while the signal layers can be sandwiched in the ground layers if possible. |

PMBus Operation

The ISL68137 PMBus slave address is pin selectable using the SA pin and resistor value described in [Table 2 on page 13](#). For proper operation, users should follow the PMBus protocol, as shown in [“PMBus Protocol” on page 23](#). The supported PMBus addresses are in 8-bit format (including write and read bit), see [Table 5](#). The least significant bit of the 8-bit address is for write (0h) and read (1h). PMBus commands are in the range from 0x00h to 0xFFh. For the ISL68137, Page 0 corresponds to Output 0 and Page 1 to Output 1. For reference purposes, the 7-bit format addresses are also summarized in [Table 5](#).

TABLE 5. PMBus 8-BIT AND 7-BIT FORMAT ADDRESS (HEX)

| 8-BIT | 7-BIT | 8-BIT | 7-BIT | 8-BIT | 7-BIT | 8-BIT | 7-BIT |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 80/81 | 40 | A0/A1 | 50 | B0/B1 | 58 | C0/C1 | 60 |
| 82/83 | 41 | A2/A3 | 51 | B2/B3 | 59 | C2/C3 | 61 |
| 88/89 | 44 | A8/A9 | 54 | B8/B9 | 5C | C8/C9 | 64 |
| 8A/8B | 45 | AA/AB | 55 | BA/BB | 5D | CA/CB | 65 |

The PMBus data formats follow PMBus specification version 1.3 and SMBus version 2.0.

Basic PMBus telemetry commands are summarized in [“PMBus Command Summary” on page 24](#).

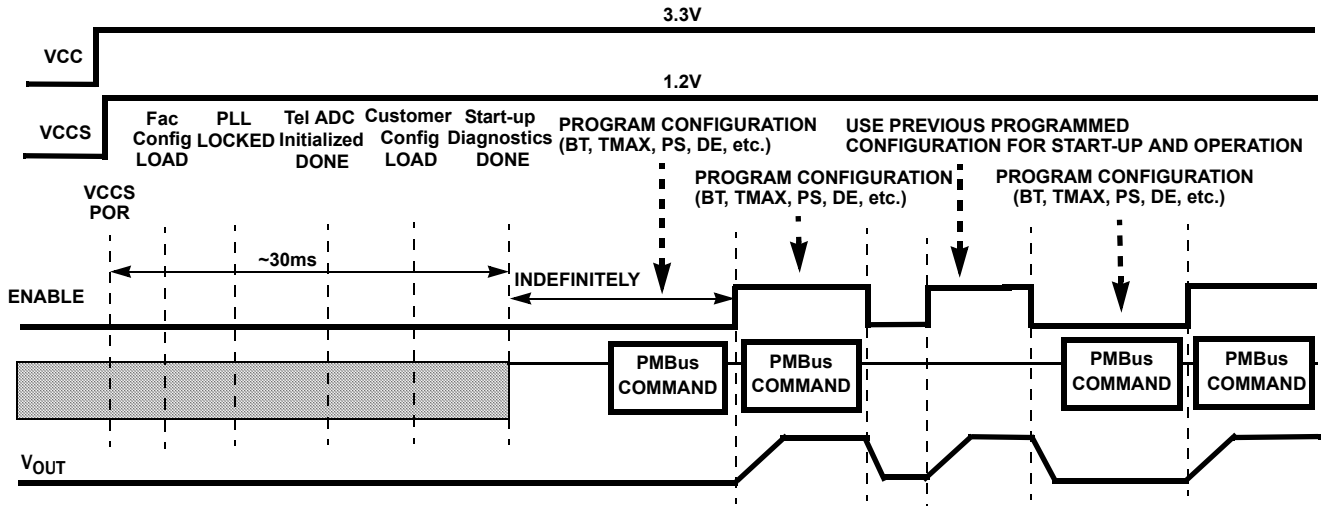
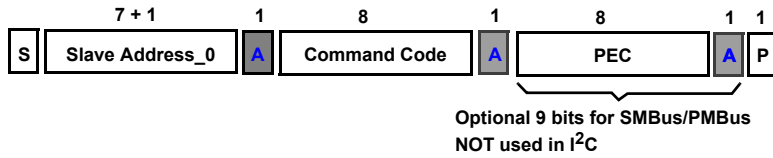


FIGURE 27. SIMPLIFIED PMBus INITIALIZATION TIMING DIAGRAM

PMBus Protocol

1. Send Byte Protocol



Example command: 03h Clear Faults
(This will clear all of the bits in Status Byte for the selected rail)

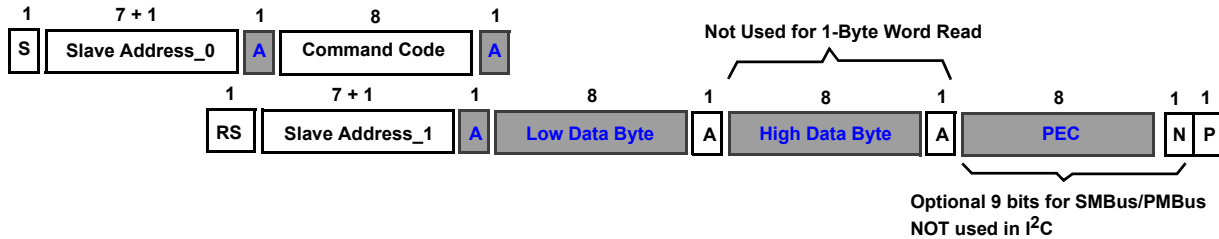
- S: Start Condition
 - A: Acknowledge ("0")
 - N: Not Acknowledge ("1")
 - W: Write ("0")
 - RS: Repeated Start Condition
 - R: Read ("1")
 - PEC: Packet Error Checking
 - P: Stop Condition
- Acknowledge or DATA from Slave, ISL68137 Controller

2. Write Byte/Word Protocol



Example command: 21h VOUT_COMMAND

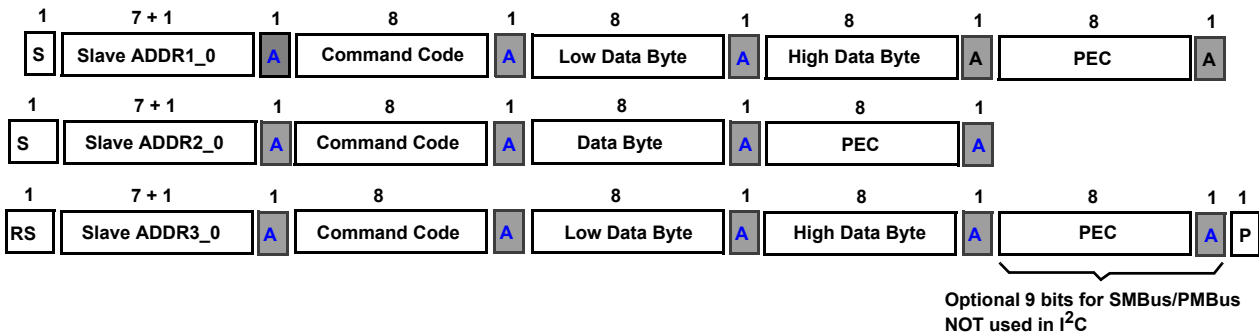
3. Read Byte/Word Protocol



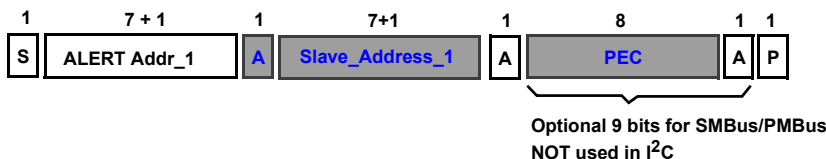
Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

STOP (P) bit is NOT allowed before the repeated START condition when "reading" contents of a register.

4. Group Command Protocol - No more than one command can be sent to the same Address



5. Alert Response Address (ARA, 0001_1001, 25h) for SMBus and PMBus, not used for I2C



PMBus Command Summary

| CODE | COMMAND NAME | DESCRIPTION | TYPE | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING |
|------|----------------------|---|-------|-------------|---------------|---------------------|
| 00h | PAGE | Selects Output 0, 1, or both | R/W | Bit | 00h | Page 0 |
| 01h | OPERATION | Enable/disable, margin settings | R/W | Bit | 08h | Off |
| 02h | ON_OFF_CONFIG | On/off configuration settings | R/W | Bit | 16h | ENABLE pin control |
| 03h | CLEAR_FAULTS | Clears all fault bits in all registers and releases the SALRT pin | Write | N/A | N/A | |
| 10h | WRITE_PROTECT | Write protection to sets of commands | R/W | Bit | 00h | No write protection |
| 20h | VOUT_MODE | Defines format for output voltage related commands | Read | Bit | 40h | Direct format |
| 21h | VOUT_COMMAND | Sets the nominal V_{OUT} target | R/W | Direct | 0384h | 900mV |
| 22h | VOUT_TRIM | Applies trim voltage to V_{OUT} set-point | R/W | Direct | 0000h | 0mV |
| 24h | VOUT_MAX | Absolute maximum voltage setting | R/W | Direct | 08FCh | 2300mV |
| 25h | VOUT_MARGIN_HIGH | Sets V_{OUT} target during margin high | R/W | Direct | 0640h | 1600mV |
| 26h | VOUT_MARGIN_LOW | Sets V_{OUT} target during margin low | R/W | Direct | 00FAh | 250mV |
| 27h | VOUT_TRANSITION_RATE | Slew rate setting for V_{OUT} changes | R/W | Direct | 0064h | 10mV/ μ s |
| 28h | VOUT_DROOP | Sets the loadline (V/I slope) resistance for the output | R/W | Direct | 0000h | 0 μ V/A |
| 2Bh | VOUT_MIN | Absolute minimum target voltage setting | R/W | Direct | 0000h | 0mV |
| 40h | VOUT_OV_FAULT_LIMIT | Sets the V_{OUT} overvoltage fault threshold | R/W | Direct | 076Ch | 1900mV |
| 44h | VOUT_UV_FAULT_LIMIT | Sets the V_{OUT} undervoltage fault threshold | R/W | Direct | 0000h | 0mV |
| 4Fh | OT_FAULT_LIMIT | Sets the over-temperature fault threshold | R/W | Direct | 007Dh | +125 °C |
| 51h | OT_WARN_LIMIT | Sets the over-temperature warning threshold | R/W | Direct | 07D0h | +2000 °C |
| 55h | VIN_OV_FAULT_LIMIT | Sets the V_{IN} overvoltage fault threshold | R/W | Direct | 36B0h | 14,000mV |
| 59h | VIN_UV_FAULT_LIMIT | Sets the V_{IN} undervoltage fault threshold | R/W | Direct | 1F40h | 8,000mV |
| 5Bh | IIN_OC_FAULT_LIMIT | Sets the I_{IN} overcurrent fault threshold | R/W | Direct | 0032h | 50A |
| 60h | TON_DELAY | Sets the delay time from enable to V_{OUT} rise | R/W | Direct | 0014h | 200 μ s |
| 61h | TON_RISE | Turn-on rise time | R/W | Direct | 01F4h | 500 μ s |
| 64h | TOFF_DELAY | Turn-off delay time | R/W | Direct | 0000h | 0 μ s |
| 65h | TOFF_FALL | Turn-off fall time | R/W | Direct | 01F4h | 500 μ s |
| 78h | STATUS_BYTE | First byte of STATUS_WORD | Read | Bit | N/A | N/A |
| 79h | STATUS_WORD | Summary of critical faults | Read | Bit | N/A | N/A |
| 7Ah | STATUS_VOUT | Reports V_{OUT} faults | Read | Bit | N/A | N/A |
| 7Bh | STATUS_IOUT | Reports I_{OUT} faults | Read | Bit | N/A | N/A |
| 7Ch | STATUS_INPUT | Reports input faults | Read | Bit | N/A | N/A |
| 7Dh | STATUS_TEMPERATURE | Reports temperature warnings/faults | Read | Bit | N/A | N/A |
| 7Eh | STATUS_CML | Reports communication, memory, logic errors | Read | Bit | N/A | N/A |
| 80h | STATUS_MFR_SPECIFIC | Reports specific events | Read | Bit | N/A | N/A |
| 88h | READ_VIN | Reports input voltage measurement | Read | Direct | N/A | N/A |
| 89h | READ_IIN | Reports input current measurement | Read | Direct | N/A | N/A |
| 8Bh | READ_VOUT | Reports output voltage measurement | Read | Direct | N/A | N/A |
| 8Ch | READ_IOUT | Reports output current measurement | Read | Direct | N/A | N/A |
| 8Dh | READ_TEMPERATURE_1 | Reports power stage temperature measurement | Read | Direct | N/A | N/A |

PMBus Command Summary (Continued)

| CODE | COMMAND NAME | DESCRIPTION | TYPE | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING |
|------|--------------------|---|-------|-------------|---------------|-----------------|
| 8Eh | READ_TEMPERATURE_2 | Reports TMON0 temperature measurement | Read | Direct | N/A | N/A |
| 8Fh | READ_TEMPERATURE_3 | Reports TMON1 temperature measurement | Read | Direct | N/A | N/A |
| 96h | READ_POUT | Reports output power | Read | Direct | N/A | N/A |
| 97h | READ_PIN | Reports input power | Read | Direct | N/A | N/A |
| 98h | PMBUS_REVISION | Reports specific events | Read | Bit | 33h | Revision 1.3 |
| ADh | IC_DEVICE_ID | Reports device identification information | Read | Bit | 49D22700h | ISL68137 |
| A Eh | IC_DEVICE_REV | Reports device revision information | Read | Bit | N/A | N/A |
| E7h | APPLY_SETTINGS | Instructs device to apply PMBus setting changes | Write | BIT | 01h | N/A |
| F2h | RESTORE_CONFIG | Allows selection of configurations from NVM | Write | BIT | N/A | N/A |

PMBus Use Guidelines

All commands can be read at any time.

Always disable the outputs when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, OPERATION.

PMBus Data Formats

Direct (D)

The Direct data format is a two byte two's complement binary integer.

Bit Field (BIT)

A breakdown of Bit Field is provided in ["PMBus Command Detail" on page 26](#).

PMBus Command Detail

PAGE (00h)

Definition: Selects Controller 0, Controller 1, or both Controllers 0 and 1 to receive commands. All commands following this command will be received and acted on by the selected controller or controllers.

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h

| COMMAND | PAGE (00h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BITS 7:4 | BITS 3:0 | PAGE |
|----------|----------|------|
| 0000 | 0000 | 0 |
| 0000 | 0001 | 1 |
| 1111 | 1111 | Both |

OPERATION (01h)

Definition: Sets enable state when configured for PMBus enable. Sets the source of the target V_{OUT} . The device always acts on faults during margin. The table below reflects the valid settings for the device.

Paged or Global: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 08h

| COMMAND | OPERATION (01h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| BIT NUMBER | PURPOSE | BIT VALUE | MEANING |
|------------|-----------------|-----------|---|
| Bits 7:6 | Enable/Disable | 00 | Immediate Off (decay) |
| | | 01 | Soft-Off (Use TOFF_DELAY and TOFF_FALL) |
| | | 10 | On |
| Bits 5:4 | VOUT Source | 00 | VOUT_COMMAND |
| | | 01 | VOUT_MARGIN_LOW |
| | | 10 | VOUT_MARGIN_HIGH |
| | | 11 | AVSBus Target Rail Voltage |
| Bits 3:2 | Margin Response | 10 | Act on Faults |
| Bit 1 | AVSBus Copy | 0 | VOUT_COMMAND remains unchanged |
| | | 1 | AVSBus Target Rail Voltage changes are copied to VOUT_COMMAND |
| Bit 0 | Not Used | 0 | Not Used |

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation of the OPERATION command and the ENABLE pin (EN). The below table reflects the valid settings for the device.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 16h (ENABLE pin control)

| COMMAND | ON_OFF_CONFIG (02h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | PURPOSE | BIT VALUE | MEANING |
|------------|----------------------------|-----------|--|
| 7:5 | Not Used | 000 | Not used |
| 4:2 | Sets the Source of Enable | 000 | Device always enabled regardless of pin or OPERATION command state |
| | | 101 | Device starts from Enable pin only |
| | | 110 | Device starts from OPERATION command only |
| | | 111 | Device starts from OPERATION command and Enable pin |
| 1 | Enable Pin Polarity | 1 | Active High only |
| 0 | Enable Pin Turn Off Action | 1 | Turn off immediately with decay |
| | | 0 | Use programmed TOFF_DELAY and TOFF_FALL settings |

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it is shut down, it will only clear the faults.

Paged or Global: Global

Data Length in Bytes: 0

Data Format: N/A

Type: Write Only

Default Value: N/A

WRITE_PROTECT (10h)

Definition: Sets the write protection of certain configuration commands.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h (Enable all writes)

| COMMAND | WRITE_PROTECT (10h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3:0 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| SETTINGS | PROTECTION |
|----------|---|
| 40h | Disables all writes except to WRITE_PROTECT, OPERATION, CLEAR_FAULTS, PAGE |
| 20h | Disables all writes except all above plus ON_OFF_CONFIG and V _{OUT} _COMMAND, V _{OUT} _TRIM |
| 00h | Enables all writes |

NOTE: Any settings other than the three shown in the table will result in an invalid data fault.

VOUT_MODE (20h)

Definition: Returns the supported V_{OUT} mode. This device only supports absolute direct mode.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 40h

Units: N/A

Equation: N/A

VOUT_COMMAND (21h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for PMBus nominal operation.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0384h (900mV)

Units: mV

Equation: V_{OUT}_COMMAND = (Direct value)

Range: V_{OUT}_MIN to V_{OUT}_MAX

| COMMAND | VOUT_COMMAND (21h) | | | | | | | | | | | | | | | |
|---------------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

VOUT_TRIM (22h)

Definition: Sets a fixed trim voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: $V_{OUT_TRIM} = (\text{Direct value})$

Range: $\pm 250\text{mV}$

| COMMAND | VOUT_TRIM (22h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VOUT_MAX (24h)

Definition: Sets the maximum allowed V_{OUT} target regardless of any other commands or combinations.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 08FCh (2300mV)

Units: mV

Equation: $V_{OUT_MAX} = (\text{Direct value})$

Range: 0mV to 3300mV

| COMMAND | VOUT_MAX (24h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin high.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0640h (1600mV)

Units: mV

Equation: $V_{OUT_MARGIN_HIGH} = (\text{Direct value})$

Range: V_{OUT_MIN} to V_{OUT_MAX}

| COMMAND | VOUT_MARGIN_HIGH (25h) | | | | | | | | | | | | | | | |
|---------------|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin low.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 00FAh (250mV)

Units: mV

Equation: $V_{OUT_MARGIN_LOW} = (\text{Direct value})$

Range: V_{OUT_MIN} to V_{OUT_MAX}

| COMMAND | VOUT_MARGIN_LOW (26h) | | | | | | | | | | | | | | | |
|---------------|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

VOUT_TRANSITION_RATE (27h)

Definition: Sets the output voltage rate of change during regulation. Changes to this setting require a write to the APPLY_SETTINGS command before the change will take effect.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0064h (10mV/μs)

Units: μV/μs

Equation: VOUT_TRANSITION_RATE = (Direct value)*100

Range: 100μV/μs to 100mV/μs

| COMMAND | VOUT_TRANSITION_RATE (27h) | | | | | | | | | | | | | | | |
|---------------|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

VOUT_DROOP (28h)

Definition: Sets the output voltage rate of change during regulation. Changes to this setting require a write to the APPLY_SETTINGS command before the change will take effect.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0μV/A)

Units: μV/A

Equation: VOUT_DROOP = (Direct value)*10

Range: 0μV/A to 16,000μV/A

| COMMAND | VOUT_DROOP (28h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VOUT_MIN (2Bh)

Definition: Sets the minimum allowed V_{OUT} target regardless of any other commands or combinations.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: $V_{OUT_MIN} = (\text{Direct value})$

Range: 0V to V_{OUT_MAX}

| COMMAND | VOUT_MIN (2Bh) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the output overvoltage fault threshold. Changes to this setting require a write to the `APPLY_SETTINGS` command before the change will take effect.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 076Ch (1900mV)

Units: mV

Equation: $V_{OUT_OV_FAULT_LIMIT} = (\text{Direct value})$

Range: 0V to V_{OUT_MAX}

| COMMAND | VOUT_OV_FAULT_LIMIT (40h) | | | | | | | | | | | | | | | |
|---------------|---------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0mV)

Units: mV

Equation: $V_{OUT_UV_FAULT_LIMIT} = (\text{Direct value})$

Range: 0V to V_{OUT_MAX}

| COMMAND | VOUT_UV_FAULT_LIMIT (44h) | | | | | | | | | | | | | | | |
|---------------|---------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

OT_FAULT_LIMIT (4Fh)

Definition: Sets the power stage over-temperature fault limit.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 007Dh (+125 °C)

Units: °C

Equation: $OT_FAULT_LIMIT = (\text{Direct value})$

Range: 0 °C to +2000 °C

| COMMAND | OT_FAULT_LIMIT (4Fh) | | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

OT_WARN_LIMIT (51h)

Definition: Sets the system over-temperature warn limit. If any measured temperature exceeds this value, the device will:

- Set the TEMPERATURE bit in STATUS_BYTE and STATUS_WORD
- Set the OT_WARNING bit in STATUS_TEMPERATURE
- Set the SALRT pin
- Set the TWARN pin

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 07D0h (+2000 °C)

Units: °C

Equation: OT_WARN_LIMIT = (Direct value)

Range: 0 to +2000 °C

| COMMAND | OT_WARN_LIMIT (51h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold. Changes to this setting require a write to the APPLY_SETTINGS command before the change will take effect.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 36B0h (14,000mV)

Units: mV

Equation: VIN_OV_FAULT_LIMIT = (Direct value)

Range: 0mV to 16,000mV

| COMMAND | VIN_OV_FAULT_LIMIT (55h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold. Also referred to as Undervoltage Lockout (UVLO). Changes to this setting require a write to the APPLY_SETTINGS command before the change will take effect.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 1F40h (8,000mV)

Units: mV

Equation: VIN_UV_FAULT_LIMIT = (Direct value)

Range: 0mV to 16,000mV

| COMMAND | VIN_UV_FAULT_LIMIT (59h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

IIN_OC_FAULT_LIMIT (5Bh)

Definition: Sets the I_{IN} overcurrent fault threshold. Changes to this setting require a write to the APPLY_SETTINGS command before the change will take effect.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0032h (50A)

Units: A

Equation: IIN_OC_FAULT_LIMIT = (Direct value)

Range: 0A to 50A

| COMMAND | IIN_OC_FAULT_LIMIT (5Bh) | | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Unsigned Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

TON_DELAY (60h)

Definition: Sets the delay time of V_{OUT} during enable.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0014h (200 μ s)

Units: μ s

Equation: $TON_DELAY = (Direct\ value) * 10$

Range: 200 μ s to 655,340 μ s

| COMMAND | TON_DELAY (60h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} during enable. Changes to this setting require a write to the APPLY_SETTINGS command before the change will take effect. This function uses the value of V_{OUT} to calculate rise time, so APPLY_SETTINGS must be sent after any change to the V_{OUT} target for accurate rise time.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (500 μ s)

Units: μ s

Equation: $TON_RISE = (Direct\ value)$

Range: 0 μ s to 10,000 μ s

| COMMAND | TON_RISE (61h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

TOFF_DELAY (64h)

Definition: Sets the delay time of V_{OUT} during disable.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0μs)

Units: μs

Equation: TOFF_DELAY = (Direct value)*10

Range: 0μs to 10,000μs

| COMMAND | TOFF_DELAY (64h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TOFF_FALL (65h)

Definition: Sets the fall time of V_{OUT} during disable. Changes to this setting require a write to the APPLY_SETTINGS command before the change will take effect. This function uses the value of V_{OUT} to calculate fall time, so APPLY_SETTINGS must be sent after any change to the V_{OUT} target for accurate fall time.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (500μs)

Units: μs

Equation: TOFF_FALL = (Direct value) *1

Range: 0μs to 10,000μs

| COMMAND | TOFF_FALL (65h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

STATUS_BYTE (78h)

Definition: Returns a summary of the unit's fault status. Based on the information in this byte, the host can get more information by reading the appropriate status registers. A fault in either output will be reported here.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Default Value: N/A

| COMMAND | STATUS_BYTE (78h) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|------------|-------------------|--|
| 7 | Not Used | Not used |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV_FAULT | An output overvoltage fault has occurred. |
| 4 | IOUT_OC_FAULT | An output overcurrent fault has occurred. |
| 3 | VIN_UV_FAULT | An input undervoltage fault has occurred. |
| 2 | TEMPERATURE | A temperature fault or warning has occurred. |
| 1 | CML | A communications, memory, or logic fault has occurred. |
| 0 | None of the Above | A status change other than those listed above has occurred. |

STATUS_WORD (79h)

Definition: Returns a summary of the device's fault status. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. A fault in either output will be reported here. The low byte of the STATUS_WORD contains the same information as the STATUS_BYTE (78h) command.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Default Value: N/A

| COMMAND | STATUS_WORD (79h) | | | | | | | | | | | | | | | |
|--------------|---------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | | | | | | | | | |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|------------|---------------------------|--|
| 15 | V _{OUT} | An output voltage fault has occurred. |
| 14 | I _{OUT} | An output current fault has occurred. |
| 13 | INPUT | An input voltage fault has occurred. |
| 12 | MFR_SPECIFIC | A manufacturer specific event has occurred. |
| 11 | POWER_GOOD # | The POWER_GOOD signal, if present, is negated. (Note 8) |
| 10:7 | Not Used | Not used |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | V _{OUT_OV_FAULT} | An output overvoltage fault has occurred. |
| 4 | I _{OUT_OC_FAULT} | An output overcurrent fault has occurred. |
| 3 | V _{IN_UV_FAULT} | An input undervoltage fault has occurred. |
| 2 | TEMPERATURE | A temperature fault or warning has occurred. |
| 1 | CML | A communications, memory, or logic fault has occurred. |
| 0 | None of the Above | A status change other than those listed above has occurred. |

NOTE:

8. If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good.

STATUS_VOUT (7Ah)**Definition:** Returns a summary of output voltage faults.**Paged or Global:** Paged**Data Length in Bytes:** 1**Data Format:** Bit Field**Type:** Read Only**Default Value:** N/A

| COMMAND | STATUS_VOUT (7Ah) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|------------|------------------|--|
| 7 | VOUT_OV_FAULT | Indicates an output overvoltage fault. |
| 6:5 | Not Used | Not used |
| 4 | VOUT_UV_FAULT | Indicates an output undervoltage fault. |
| 3 | VOUT_MAX Warning | Indicates an output voltage maximum warning. |
| 2:0 | Not Used | Not used |

STATUS_IOUT (7Bh)**Definition:** Returns a summary of output current faults.**Paged or Global:** Paged**Data Length in Bytes:** 1**Data Format:** Bit Field**Type:** Read Only**Default Value:** N/A

| COMMAND | STATUS_IOUT (7Bh) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|------------|--|
| 7 | An output overcurrent fault has occurred. |
| 6 | An output overcurrent and undervoltage fault has occurred. |
| 5:4 | Not used |
| 3 | A current share fault has occurred. |
| 2:0 | Not used |

STATUS_INPUT (7Ch)**Definition:** Returns a summary of input voltage faults.**Paged or Global:** Global**Data Length in Bytes:** 1**Data Format:** Bit Field**Type:** Read Only**Default Value:** N/A

| COMMAND | STATUS_INPUT (7Ch) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|------------|---|
| 7 | An input overvoltage fault has occurred. |
| 6:5 | Not used |
| 4 | An input undervoltage fault has occurred. |
| 3 | Not used |
| 2 | An input overcurrent fault has occurred. |
| 1:0 | Not used |

STATUS_TEMPERATURE (7Dh)**Definition:** Returns a summary of temperature related faults.**Paged or Global:** Global**Data Length in Bytes:** 1**Data Format:** Bit Field**Type:** Read Only**Default Value:** N/A

| COMMAND | STATUS_TEMPERATURE (7Dh) | | | | | | | |
|--------------|--------------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|------------|---|
| 7 | An over-temperature fault has occurred. |
| 6 | An over-temperature warning has occurred. |
| 5 | Not used |
| 4 | An under-temperature fault has occurred |
| 3:0 | Not used |

STATUS_CML (7Eh)

Definition: Returns a summary of any communications, logic and/or memory errors.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: N/A

| COMMAND | STATUS_CML (7Eh) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|------------|--|
| 7 | Invalid or unsupported PMBus Command was received. |
| 6 | The PMBus command was sent with invalid or unsupported data. |
| 5 | A packet error was detected in the PMBus command. |
| 4 | Memory fault detected. |
| 3 | Processor fault detected. |
| 2 | Not used |
| 1 | A communication fault other than the ones listed in this table has occurred. |
| 0 | A memory or logic fault not listed above was detected. |

STATUS_MFR_SPECIFIC (80h)

Definition: Returns the status of specific information detailed below.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: N/A

| COMMAND | STATUS_MFR_SPECIFIC (80h) | | | | | | | |
|--------------|---------------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT | MEANING |
|-----|------------------------|
| 7:2 | Not used |
| 1 | OTP NVM memory is full |
| 0 | Not used |

READ_VIN (88h)**Definition:** Returns the input voltage reading.**Paged or Global:** Global**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Default Value:** N/A**Units:** mV**Equation:** READ_VIN = (Direct value)

| COMMAND | READ_VIN (88h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_IIN (89h)**Definition:** Returns the input current reading.**Paged or Global:** Global**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Default Value:** N/A**Units:** A**Equation:** READ_IIN = (Direct value)/100

| COMMAND | READ_IIN (89h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_VOUT (8Bh)**Definition:** Returns the output voltage reading.**Paged or Global:** Paged**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Default Value:** N/A**Units:** mV**Equation:** READ_VOUT = (Direct value)

| COMMAND | READ_VOUT (8Bh) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_IOUT (8Ch)**Definition:** Returns the output current reading.**Paged or Global:** Paged**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Default Value:** N/A**Units:** A**Equation:** READ_IOUT = (Direct value)/10

| COMMAND | READ_IOUT (8Ch) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_TEMPERATURE_1 (8Dh)**Definition:** Returns the temperature reading of the power stage.**Paged or Global:** Paged**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Default Value:** N/A**Units:** °C**Equation:** READ_TEMPERATURE_1 = (Direct value)

| COMMAND | READ_TEMPERATURE_1 (8Dh) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_TEMPERATURE_2 (8Eh)**Definition:** Returns the temperature reading from a remote diode connected to TMON0 when configured for diode sensing.**Paged or Global:** Global**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Default Value:** N/A**Units:** °C**Equation:** READ_TEMPERATURE_2 = (Direct value)

| COMMAND | READ_TEMPERATURE_2 (8Eh) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_TEMPERATURE_3 (8Fh)

Definition: Returns the temperature reading from a remote diode connected to TMON1 when configured for diode sensing.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Default Value: N/A

Units: °C

Equation: READ_TEMPERATURE_3 = (Direct value)

| COMMAND | READ_TEMPERATURE_3 (8Fh) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_POUT (96h)

Definition: Returns the output power.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Default Value: N/A

Units: W

Equation: READ_POUT = (Direct value)

| COMMAND | READ_POUT (96h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

READ_PIN (97h)

Definition: Returns the input power.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Default Value: N/A

Units: W

Equation: READ_PIN = (Direct value)

| COMMAND | READ_PIN (97h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus specification to which the device is compliant.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

| COMMAND | PMBUS_REVISION (98h) | | | | | | | |
|---------------|----------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

| BITS 7:4 | PART 1 REVISION | BITS 3:0 | PART 2 REVISION |
|----------|-----------------|----------|-----------------|
| 0000 | 1.0 | 0000 | 1.0 |
| 0001 | 1.1 | 0001 | 1.1 |
| 0010 | 1.2 | 0010 | 1.2 |
| 0011 | 1.3 | 0011 | 1.3 |

IC_DEVICE_ID (ADh)

Definition: Returns device identification information.

Paged or Global: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: 49D22700h

| COMMAND | IC_DEVICE_ID (ADh) | | | |
|---------------|--------------------|--------------|-------------|----------|
| Format | Block Read | | | |
| Byte Position | 3 | 2 | 1 | 0 |
| Function | MFR code | ID High Byte | ID Low Byte | Reserved |
| Default Value | 49h | D2h | 27h | 00h |

IC_DEVICE_REV (AEh)

Definition: Returns device revision information.

Paged or Global: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: N/A

| COMMAND | IC_DEVICE_REV (AEh) | | | |
|---------------|---------------------|-----------------------|-------------------|-------------|
| Format | Block Read | | | |
| Bit Position | 23:16 | 15:8 | 7:4 | 3:0 |
| Function | Firmware Revision | Factory Configuration | Chip Foundry Site | IC Revision |
| Default Value | N/A | N/A | N/A | N/A |

APPLY_SETTINGS (E7h)

Definition: Instructs the controller to use new PMBus parameters. Send 01h to this command after making one or more changes to certain PMBus threshold commands that require rescaling of operational values. The commands that require this are VOUT_TRANSITION_RATE, VOUT_DROOP, VOUT_OV_FAULT_LIMIT, VIN_OV_FAULT_LIMIT, VIN_UV_FAULT_LIMIT, IIN_OC_FAULT_LIMIT, TON_RISE, and TOFF_FALL.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Bit

Type: Write Only

Default Value: 01h

Units: N/A

Equation: N/A

RESTORE_CONFIG (F2h)

Definition: Identifies the configuration to be restored from NVM and loads the store's settings into the device's active memory.

Paged or Global: Global

Data Length in Bytes: 1

Data Format: Bit

Type: Write Only

Default Value: N/A

| COMMAND | RESTORE_CONFIG (F2h) | | | | | | | |
|---------------|----------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|------------|-----------------|-----------------------------------|
| 7:4 | Reserved | Reserved |
| 3:0 | CONFIG | Selected configuration to restore |

Adaptive Voltage Scaling Bus (AVSBus) Functionality and Operation

The AVSBus interface provides a high speed (up to 50MHz) serial interface to the ISL68137, allowing implementation of advanced voltage scaling functions that support increased system efficiency and performance. Devices equipped with AVSBus master capability can use the interface to enable rapid supply voltage changes to support low power consumption modes as well as high performance modes. Due to the advanced digital regulation loop employed, the ISL68137 is well equipped to support very rapid transition rates. All commands are readable at all times, but they cannot be written unless the device is set to AVSBus control.

AVSBus Master Send Subframe

| FUNCTION | Start Code | R/W | Command Type | Command Code | Rail Select | Command Data | CRC |
|-------------|------------|--|------------------|--|--|--|-----|
| SIZE (bits) | 2 | 2 | 1 | 4 | 4 | 16 | 3 |
| SETTING | 01b | 00b = Write data and Commit 11b = Read Data | 0b = AVSBus Data | 0h = Target Rail Voltage 1h = Transition Rate 2h = Rail Current 3h = Temperature 4h = Voltage Reset Eh = AVSBus Status Fh = AVSBus Version | 0h = Rail 0 1h = Rail 1 Fh = Broadcast | Read = FFh Write = See "AVSBus Command Detail" on page 50 | |

AVSBus Slave Response Subframe

| FUNCTION | Slave Ack | 0b | Status Response | Command Data | Not used | CRC |
|-------------|---|----|---|--|--------------------|-----|
| SIZE (bits) | 2 | 1 | 5 | 16 | 5 | 3 |
| SETTING | 00b = Command acknowledged, action taken 01b = Command acknowledged, no action 10b = Bad CRC, no action 11b = Invalid request, no action | 0b | Bit 4 = VDONE. Sets to 1 when V_{OUT} target is reached Bit 3 = Status alert. Sets to 1 if a bit in AVSBus Status register (excluding from VDONE) has set Bit 2 = AVSBus control. Sets to 1 when AVSBus control is enabled Bits 1:0 = Not used | Write = FFh Read = See "AVSBus Command Detail" on page 50 | Not used 11111b | |

AVSBus Command Detail

TARGET RAIL VOLTAGE (0h)

Definition: Sets or reads the target rail voltage set point. 1mV per LSB. The initial set point is copied from the PMBus command VOUT_COMMAND when AVSBus operation is selected.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: Value of PMBus VOUT_COMMAND

Units: mV

Equation: TARGET RAIL VOLTAGE = (Direct value)

Range: Limited to the PMBus command values of VOUT_MIN and VOUT_MAX

| COMMAND | TARGET RAIL VOLTAGE (0h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

TRANSITION RATE (1h)

Definition: Sets or reads the rise and fall transition rates. 1mV/μs per LSB. The initial value matches PMBus transition rates until updated through AVSBus.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: Value of PMBus VOUT_TRANSITION_RATE for rise and fall

Units: mV/μs

Equation: TRANSITION RATE = (Direct value)

| COMMAND | TRANSITION RATE (1h) | | | | | | | | | | | | | | | |
|---------------|--|-----|-----|-----|-----|-----|-----|-----|--|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Rise Transition Rate, Two's Complement Integer | | | | | | | | Fall Transition Rate, Two's Complement Integer | | | | | | | |
| Default Value | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

RAIL CURRENT (2h)

Definition: Returns the output current reading. 10mA per LSB. A filter is applied to this reading, and it is configurable in PowerNavigator.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Default Value: N/A

Units: A

Equation: RAIL CURRENT = (Direct value)/100

| COMMAND | RAIL CURRENT (2h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

TEMPERATURE (3h)

Definition: Returns the power stage temperature reading. 0.1°C per LSB. This value is copied from the READ_TEMPERATURE_1 PMBus command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Default Value: N/A

Units: °C

Equation: TEMPERATURE = (Direct value)/10

| COMMAND | TEMPERATURE (3h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

VOLTAGE RESET (4h)

Definition: Sets TARGET RAIL VOLTAGE to match that of the VOUT_COMMAND PMBus command.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Write Only

Default Value: 00h

Units: N/A

| COMMAND | VOLTAGE RESET (4h) | | | | | | | | | | | | | | | |
|---------------|--------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
| Function | Send all 0's | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

AVSBUS STATUS (Eh)

Definition: Returns the device status. VDONE indicates that the V_{OUT} setting target has been reached. OT Warn indicates that one or more of the device's temperature measurements has exceeded the over-temperature warning threshold set by the OT_WARN_LIMIT PMBus command. The device sets the AVS_SDA line low to notify the host any time a bit in this register has been set.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Default Value: N/A

Units: N/A

| COMMAND | AVSBUS STATUS (Eh) | | | | |
|---------------|--------------------|----------|----------|---------|----------|
| Format | Bit Field | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11:0 |
| Access | R | R | R | R | R |
| Function | VDONE | Not Used | Not Used | OT Warn | Not Used |
| Default Value | N/A | 0 | 0 | N/A | 0 |

AVSBUS VERSION (Fh)

Definition: Returns the version of the AVSBus specification to which the device is compliant. This device complies with Version 1.3.

Paged or Global: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Default Value: 00h

Units: N/A

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---------------|----------|---|
| Jun 26, 2017 | FN8757.1 | <p>Applied new header/footer.</p> <p>Updated Figure 5 on page 9.</p> <p>Updated "Enable (EN0 and EN1) Input High Level" spec on page 10, removed typical and added a min spec of 2.55V.</p> <p>Added "Enable (EN0 and EN1) Input Low Level" spec on page 10.</p> <p>On page 12, changed from "SCL, SDA Input High/Low Threshold" to "SCL, SDA Input High Level" removed typical and added Min spec of 1.55V.</p> <p>Added "SCL, SDA Input Low Level" spec on page 12.</p> <p>On pages 29 through 38, Updated the tables in the PMBus Command Detail section for the following commands, changed from "Two's Complement Integer" to "Unsigned Integer".</p> <p>- VOUT_COMMAND, VOUT_MAX, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_TRANSITION_RATE, VOUT_DROOP, VOUT_MIN, VOUT_OV_FAULT_LIMIT, VOUT_UV_FAULT_LIMIT, VIN_OV_FAULT_LIMIT, VIN_UV_FAULT_LIMIT, IIN_OC_FAULT_LIMIT, TON_DELAY, TON_RISE, TOFF_DELAY, and TOFF_FALL</p> <p>Updated "READ_PIN (97h)" on page 46 from Paged to Global.</p> <p>Updated "STATUS_CML (7Eh)" on page 43, changed Bit 1 meaning to "A communication fault other than the ones listed in this table has occurred."</p> <p>Updated "AVSBus Slave Response Subframe" on page 49. Bit numbers were off by one for the setting row.</p> <p>Updated About Intersil verbiage.</p> |
| Sept 27, 2016 | FN8757.0 | Initial Release |

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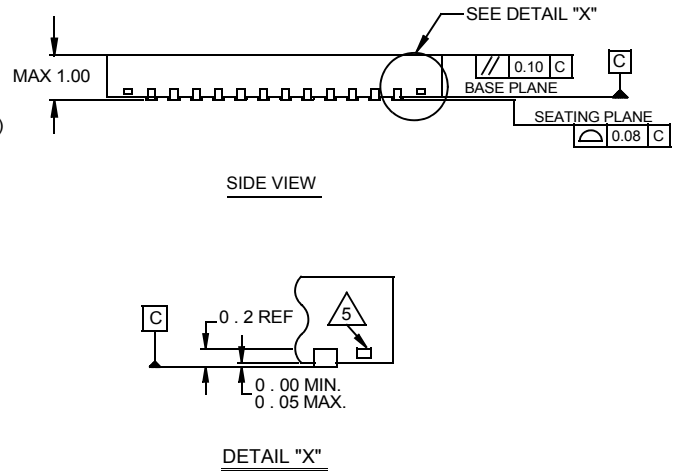
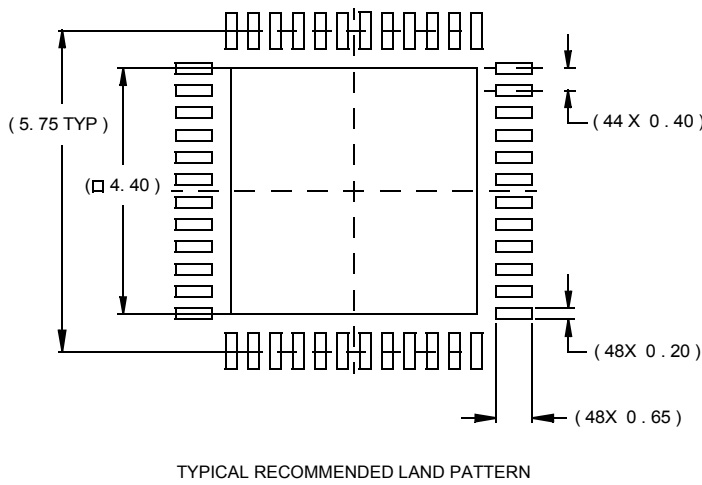
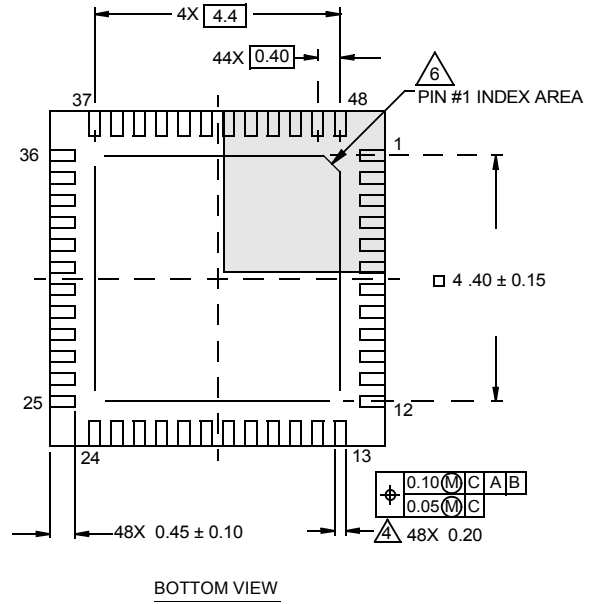
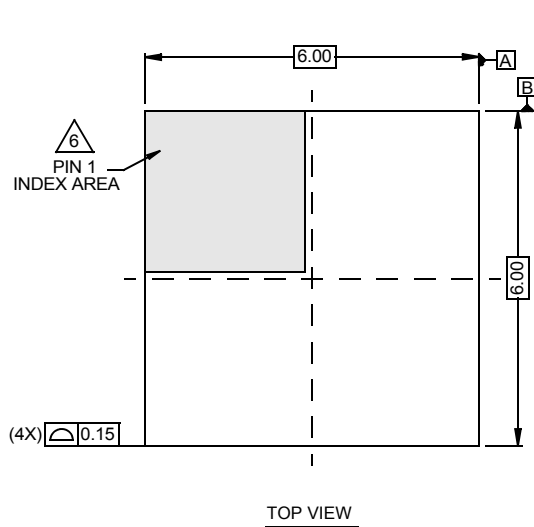
Package Outline Drawing

For the most recent package outline drawing, see [L48.6x6B](#).

L48.6x6B

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 9/09



NOTES:

- Dimensions are in millimeters.
Dimensions in () for Reference Only.
- Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
- Unless otherwise specified, tolerance : Decimal ± 0.05
- Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
- Tiebar shown (if present) is a non-functional feature.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.