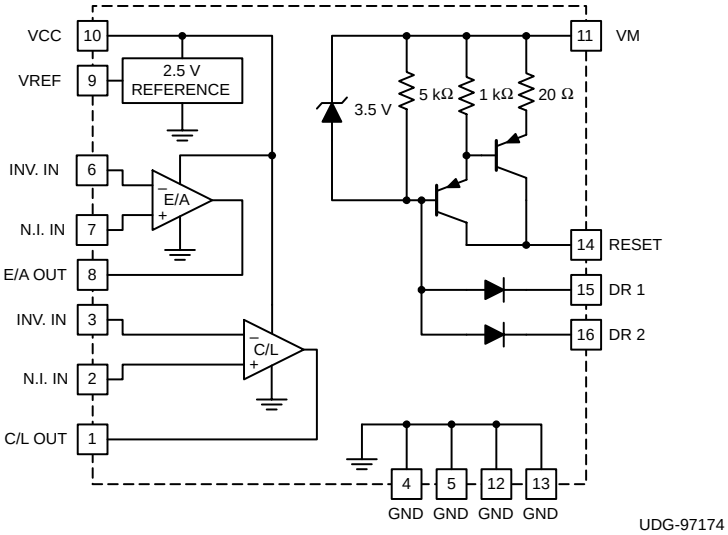
SLUS221A – APRIL 2000 – REVISED MAY 2001

MAGNETIC AMPLIFIER CONTROLLER

FEATURES

- **Independent 1% Reference**
- **Two Uncommitted, Identical Operational Amplifiers**
- **100-mA Reset Current Source With –120-V Capability**
- **5-V to 40-V Analog Operation**
- **5-W DIP Package**

BLOCK DIAGRAM



UDG-97174

DESCRIPTION

The UC3838 and the UC3838A family of magnetic amplifier controllers contains the circuitry to generate and amplify a low-level analog error signal along with a high voltage-compliant current source. This source provides the reset current necessary to enable a magnetic amplifier to regulate and control a power supply output in the range of 2 A to 20 A.

The UC3838A originally was a parametric improvement version of the UC3838 which since has been used for both versions. There is no difference between the *UC3838A* and *UC3838* version.

By controlling the reset current to a magnetic amplifier, this device defines the amount of volt-seconds the magnetic amplifier blocks before switching to the conducting state. Magnetic amplifiers are ideal for post-regulators for multiple-output power supplies where each output can be independently controlled with efficiencies up to 99%. With a square or pulse-width modulated input voltage, a magnetic amplifier blocks a portion of this input waveform, allowing just enough to pass to provide a regulated output. With the UC3838/A, only the magnetic amplifier coil, three diodes, and an output L-C filter are necessary to implement a complete closed-loop regulator.

AVAILABLE OPTIONS

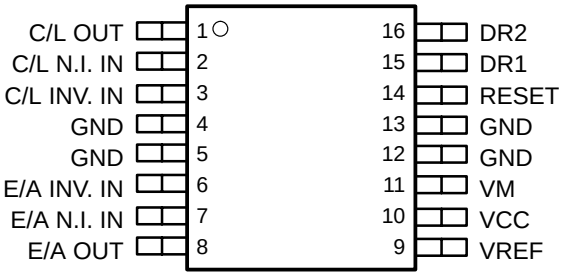
$T_A = T_J$	Packaged Devices		
	SOIC Wide (DW)	PDIP (N)	PLCC (Q)
–20°C to 85°C	UC2838DW	UC2838N	UC2838Q
	UC2838ADW	UC2838AN	UC2838AQ
0°C to 70°C	UC3838DW	UC3838N	UC3838Q
	UC3838ADW	UC3838AN	UC3838AQ

description (continued)

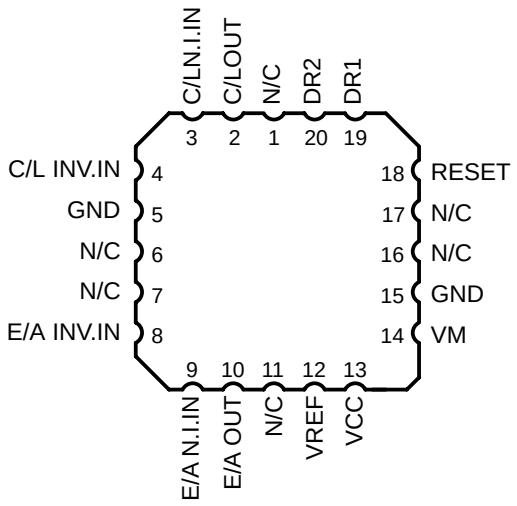
The UC3838/A contains a precision 2.5-V reference, two uncommitted high-gain operational amplifier and a high-gain PNP-equivalent current source which can deliver up to 100 mA of magnetic amplifier reset current and with –120-V capability.

These devices are available in a plastic batwing DIP (N), wide body SOIC (DW), and PLCC (Q) package for operation over a –20°C to 85°C temperature range.

DW AND N PACKAGES
(TOP VIEW)



Q PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 40 V
Magnetic amplifier source voltage, VM . . . . . 40 V
Reset output voltage, VR . . . . . –120 V
Total current source voltage, VM – VR . . . . . –140 V
Amplifier input range . . . . . –0.3 V to VCC
Reset input current, DR1 and DR2 . . . . . –10 mA
Power dissipation at T_A = 25°C
  Q, N, DW package . . . . . 2 W
Power dissipation at T (leads/case) = 25°C
  Q, N, DW package . . . . . 5 W
Operating temperature range, T_J . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature (soldering, 10 sec) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to ground pins. All currents are positive into the specified terminal. Consult packaging section of data book for thermal limitations and considerations of package.

electrical characteristics, T_A = –20°C to 85°C for the UC2838/A, and T_A = 0°C to 70°C for the UC3838/A, V_{CC} = 20 V, VM = 5 V, T_A = T_J, (unless otherwise stated)

reference

PARAMETER	TEST CONDITIONS	UC2838/UC2838A			UC3838/UC3838A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply current	V_{CC} = V_M = 40 V		4	8		4	8	mA
Reference output	T_A = 25°C	2.47	2.50	2.53	2.45	2.50	2.55	V
Line regulation	V_{CC} = 5 V to 30 V		1	5		1	10	mV
Load regulation	I_O = 0 mA to –2 mA		5	20		5	20	mV
Short-circuit current	VREF = 0 V		–30	–60		–30	–60	mA
Temperature stability	See Note 1		15	25		10	25	mV

NOTE: 1.These parameters are ensured by design but not 100% tested in production.

amplifier (each amplifier)

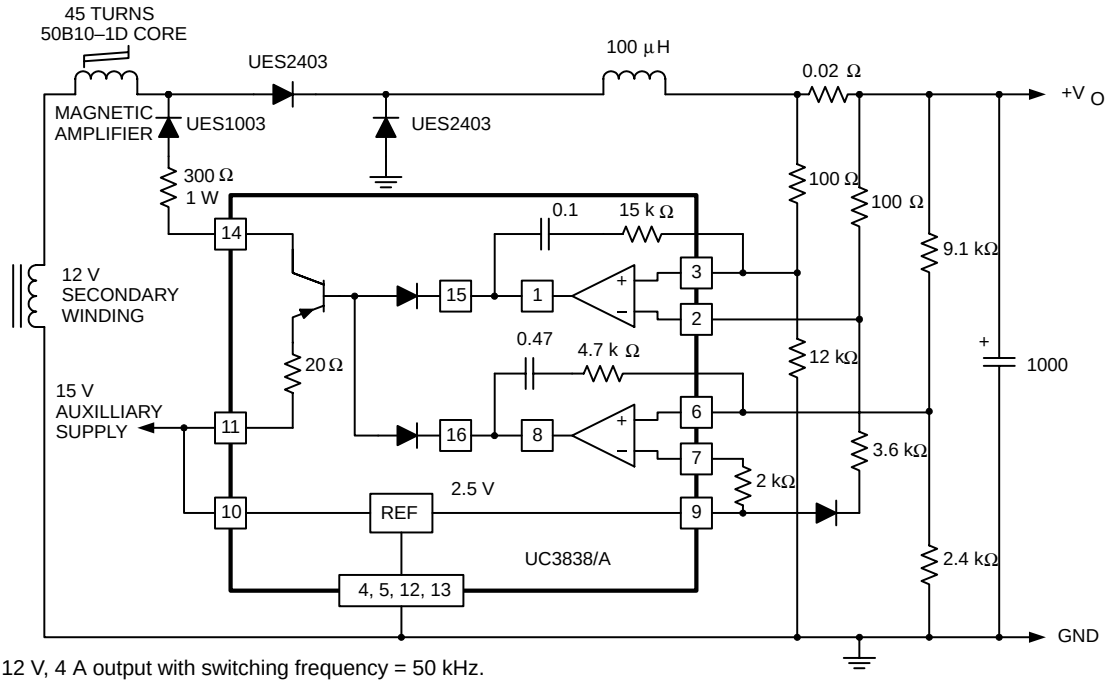
PARAMETER	TEST CONDITIONS	UC2838/UC2838A			UC3838/UC3838A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Offset voltage	V_{CM} = 2.5 V			5			10	mV
Input bias current	V_{IN} = 0 V			–1			–1	µA
Input offset voltage				100			100	nA
Minimum output swing		0.4		18	0.4		18	V
Output sink current	V_O = 5 V	1	10	30	1	10	30	mA
Output source current	V_O = 0 V	–1	–10	–20	–1	–10	–20	mA
A_{VOL} (open loop gain)	V_O = 1 V to 11 V	100	120		100	120		dB
C_{MRR} (common mode rejection ratio)	V_{IN} = 1 V to 11 V	70	80		70	80		dB
P_{SRR} (power supply rejection ratio)	V_{CC} = 10 V to 20 V	70	100		70	100		dB
Gain bandwidth	See Note 1	0.6	0.8		0.6	0.8		MHz

NOTE: 1.These parameters are ensured by design but not 100% tested in production.

reset drive

PARAMETER	TEST CONDITIONS	UC2838/UC2838A			UC3838/UC3838A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input leakage	V_{DR} = 40 V			10			10	µA
Output leakage	VR = –120 V			–100			–100	µA
Input current	I_R = –50 mA		–1	–2		–1	–2	mA
Maximum reset current	I_{DR} = –3 mA	–100	–120	–200	–100	–120	–200	mA
Transconductance	I_R = –10 mA to –50 mA	0.03	0.042	0.055	0.03	0.042	0.055	A/V

typical application



NOTE: 12 V, 4 A output with switching frequency = 50 kHz.

APPLICATION INFORMATION

GAIN MAGNITUDE/PHASE vs SIGNAL FREQUENCY

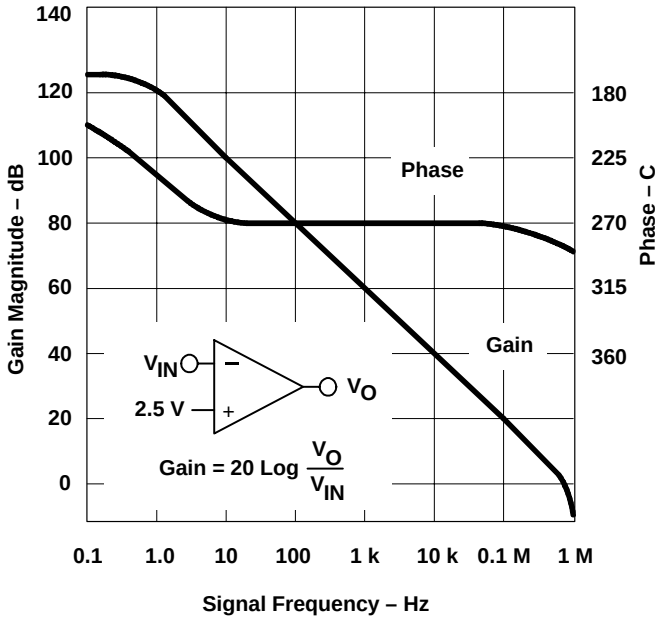


Figure 1.

GAIN MAGNITUDE vs SIGNAL FREQUENCY

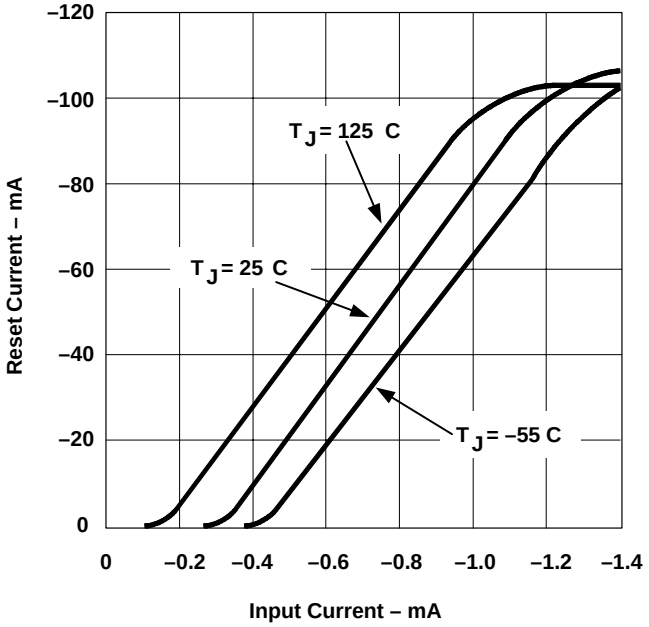


Figure 2.

APPLICATION INFORMATION

RESET CURRENT vs RESET VOLTAGE

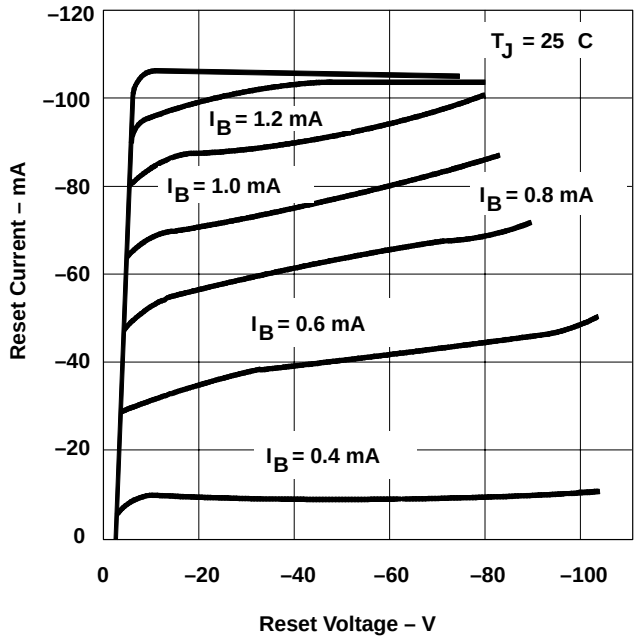


Figure 3.

GAIN MAGNITUDE/PHASE vs SIGNAL FREQUENCY

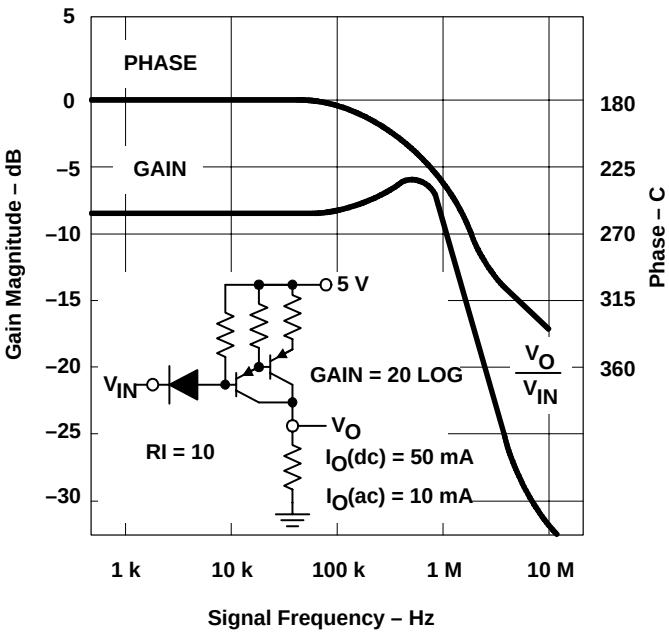


Figure 4.

RESET CURRENT vs INPUT CURRENT

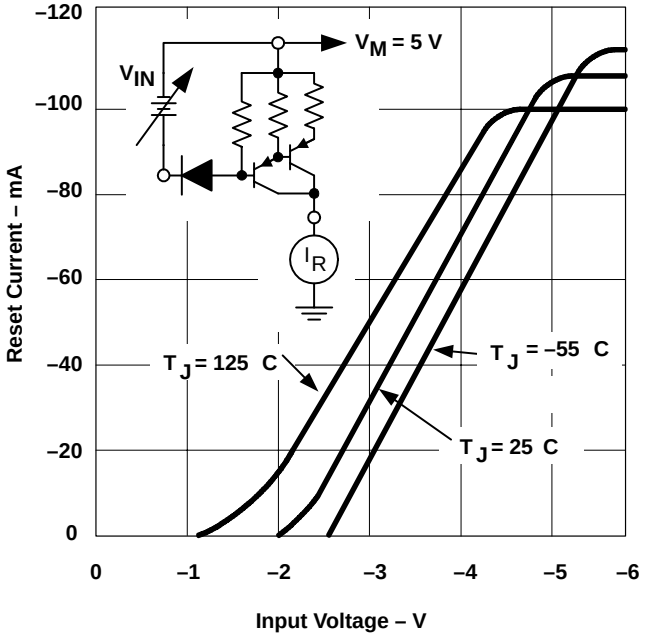


Figure 5.

REFERENCE VOLTAGE OUTPUT vs JUNCTION TEMPERATURE

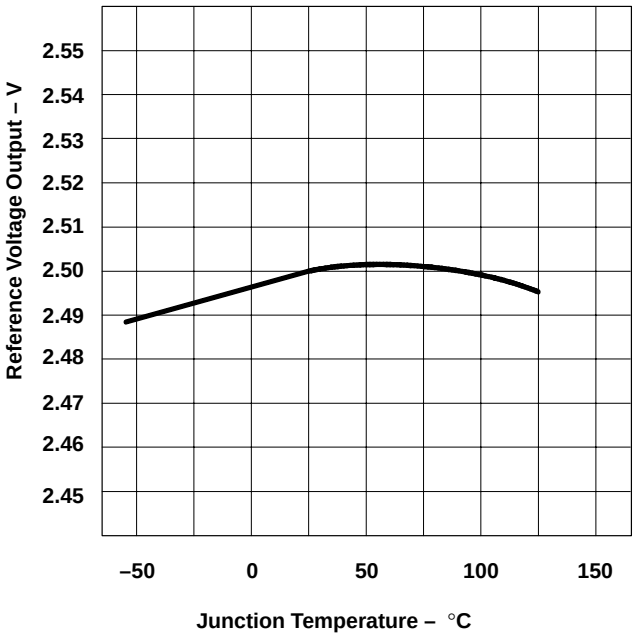


Figure 6.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UC2838AJ	NRND	CDIP	J	16		TBD	Call TI	Call TI	-40 to 85		
UC2838AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 85	UC2838AN	
UC2838ANG4	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 85		
UC2838AQ	NRND	PLCC	FN	20		TBD	Call TI	Call TI	-40 to 85		
UC2838AQTR	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI	-40 to 85		
UC3838ADW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF UC3838A :

- Military: UC1838A

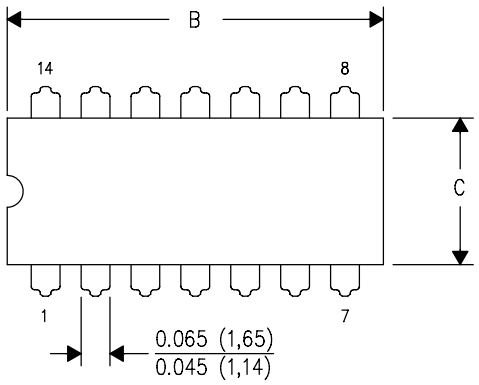
NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

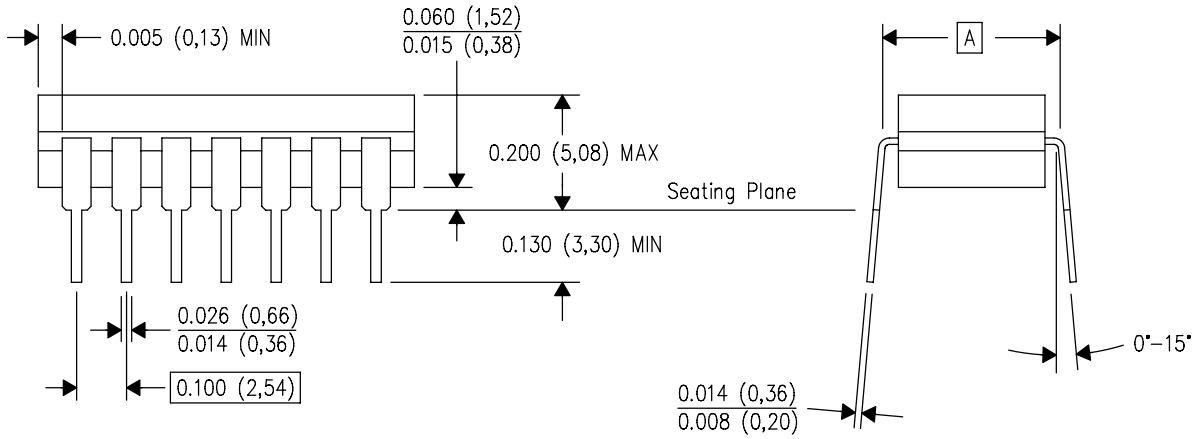
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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