Click here for production status of specific part numbers.

MAX5992A/MAX5992B

Multisource, High-Power, High-Performance Powered Device Controllers

General Description

The MAX5992A/MAX5992B multisource, high-power, high-performance powered device (PD) controllers provide a complete interface control for PDs to comply with the IEEE® 802.3af/at standard in a Power-over-Ethernet (PoE) system. The devices provide the PD with a detection signature, classification signature, and an isolation MOSFET driver with current-limit control. In addition, the intelligent maintain power signature (MPS) and active FET bridge control make the PD more power efficient. The devices feature a $\overline{SIG\_OK}$ output signal for high-power Multi-2P PD applications. The selectable inrush-current modes allow Multi-PD, fiber-to-the-home/fiber-to-the-building (FTTH/FTTB) operation in redundancy applications. The devices feature an input UVLO, wide hysteresis, and long deglitch time to compensate for twisted-pair cable resistive drop to assure glitch-free transition during power-on/power-off conditions. The devices can operate from a 20.8V low-voltage supply by a selectable UVLO. The devices can withstand up to 100V at the input.

The devices support a 2-Event classification method as specified in the IEEE 802.3at standard and provide a signal to indicate when probed by Type 2 power-sourcing equipment (PSE). The devices detect the presence of a wall adapter power-source connection and allow a smooth switchover from the PoE power source to the wall power adapter. Moreover, the selectable WAD_SEL supports seamless power transition from a wall adapter to PoE if PoE is already enabled.

The devices also provide a power-good (PG) signal, 2-level current limit, foldback, and overtemperature protection. A sleep mode feature provides low-power consumption while supporting MPS. An ultra-low power sleep mode feature further reduces power consumption to comply with ultra-low power requirements while still supporting MPS. The devices also feature an LED driver that is automatically activated during sleep/ultra-low power sleep/MPS mode. The MAX5992A has 38.6V PoE UVLO and the MAX5992B has 35.4V PoE UVLO and feature a 6.5s sleep mode delay.

The MAX5992A/MAX5992B are available in a 24-pin, 4mm x 4mm, TQFN power package and are rated over the -40°C to +85°C extended temperature range.

Features

- IEEE 802.3af/at Compliant
- UPoE Compatible
- High-Power 2x2P/Multi-PD Synchronization/Multi-PD Redundancy
- Integrated Active FET Bridge Control and Back-Powering Protection
- Selectable UVLO for Medical/Industrial Applications
- 2-Level Inrush-Current Control
- Intelligent MPS
- Simplified Wall Adapter Interface for Seamless Power Transition
- Ultra-Low-Power/Sleep Mode
- 2-Event Classification or an External Wall Adapter Indicator Output
- PoE Classification 0 to 5
- Gate Driver for External Isolation MOSFET
- Selectable Current Limit and Foldback
- RJ45 12V Supply Input
- 6.5s Sleep Mode Delay

Applications

- IEEE 802.3af/at-Powered Devices (PD)
- Universal Power-over-Ethernet (UPoE)
- Femtocell, Picocell, Microcell
- High-Power 2x2P PD
- Multi-PD Redundancy
- Fiber-to-the-Home/Building (FTTH/FTTB)
- IP Phones
- Wireless Access Nodes
- IP Security Cameras (IPC)
- WiMAX® Base Stations

***Ordering Information/Selector Guide* appears at end of data sheet.**

Absolute Maximum Ratings

V_{DD}, PDR1, PDR2 to V_{SS} ....-0.3V to +80V
DET, RTN, WAD, $\overline{\text{SIG\_OK}}$, V_{IN1}, V_{IN2},
LED, $\overline{\text{2EC}}$ to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
PG to V_{DD} ....-80V to +0.3V
GATE, NDR1, NDR2 to V_{SS} ....-0.3V to +14V
PDR1, PDR2 to V_{DD} ....-14V to +0.3V
CLS, SENSE, ADJ_UVLO, RDCY_SEL, $\overline{\text{SL}}$,
$\overline{\text{ULP}}$, CL_SEL, WAD_SEL to V_{SS} ....-0.3V to +6V
Maximum Input/Output Current (continuous)
PG from V_{DD} 10mA
Maximum Current from CLS (100ms maximum) 100mA
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN (derate 27.8mW/°C above +70°C)
(Note 1)..2222.2mW
Operating Temperature Range........................... -40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow).......................................+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 TQFN

Package Code	T2444+4
Outline Number	21-0139
Land Pattern Number	90-0022
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, $R_{\overline{SL}}$ = 60.4kΩ, all other pins unconnected. All voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DETECTION MODE							
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V to 10.1V (Note 2)				10	µA
Effective Differential Input Resistance	dR	V_{IN} = 1.4V up to 10.1V with 1V step, V_{DD} = RTN = WAD = PG = $\overline{2EC}$ (Note 3)		23.95	25.00	25.5	kΩ
CLASSIFICATION MODE							
Classification Disable Threshold	$V_{TH,CLS}$	V_{IN} rising (Note 4)		22.0	22.8	23.6	V
Classification Stability Time					0.2		ms
Classification Current	I_{CLASS}	V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG = $\overline{2EC}$	Class 0, R_{CLS} = 615Ω	0		3.96	mA
			Class 1, R_{CLS} = 118Ω	9.12		11.88	
			Class 2, R_{CLS} = 69.8Ω	17.2		19.8	
			Class 3, R_{CLS} = 45.3Ω	26.3		29.7	
			Class 4, R_{CLS} = 30.9Ω	36.4		43.6	
			Class 5, R_{CLS} = 21.5Ω	52.7		63.3	
TYPE 2 (802.3at) CLASSIFICATION MODE							
Mark Event Threshold	V_{THM}	V_{IN} falling		10.1	10.8	11.6	V
Hysteresis on Mark Event Threshold					0.84		V
Mark Event Current	I_{MARK}	V_{IN} falling to enter mark event, 5.2V ≤ V_{IN} ≤ 10.1V		1.0		3.5	mA
Reset Event Threshold	V_{THR}	V_{IN} falling		2.8	4	5.2	V
ISOLATION FET GATE DRIVER							
External Gate Drive Voltage	V_{GS}	Power-on mode, V_{GATE} - V_{SS}		8	9.5	11	V
Gate Pullup Current	I_{PU}	Power-on mode, V_{GATE} = V_{SS}		40	50	60	µA
Gate Pulldown Current	I_{PDW}	Power-on mode, V_{GATE} - V_{SS} = +2V, V_{SENSE} - V_{LIM} = +20mV		28	40	50	µA
Strong Pulldown Current	I_{PDS}	Power-on mode, V_{GATE} - V_{SS} = +2V, V_{SENSE} - V_{SS} = +1V			44		mA
POWER-ON MODE							
V_{IN} Voltage Range	V_{IN}	V_{DD} – V_{SS}				60	V
V_{IN} Overvoltage	V_{OV}	V_{IN} rising, external isolation MOSFET is turned off when V_{IN} > V_{OV}			65		V
V_{IN} Overvoltage Hysteresis	V_{HYST_OV}	V_{IN} falling			4.5		V
V_{IN} Overvoltage Deglitch Time		V_{IN} rising and falling			170		µs
V_{IN} Supply Current	I_Q	Power-on mode			1.5	2.5	mA

DC Electrical Characteristics (continued)

$V_{IN} = (V_{DD} - V_{SS}) = 48V$, $R_{DET} = 24.9k\Omega$, $R_{CLS} = 615\Omega$, $R_{\overline{SL}} = 60.4k\Omega$, all other pins unconnected. All voltages are referenced to V_{SS}, unless otherwise noted. $T_A = T_J = -40°C$ to $+85°C$. Typical values are at $T_A = +25°C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Turn-On Voltage	V_{ON}	V_{IN} rising, ADJ_UVLO unconnected	MAX5992A	37	38.6	40	V
			MAX5992B	34.3	35.4	36.6	
	V_{ON_IND}	V_{IN} rising, ADJ_UVLO pulldown to V_{SS} (industrial UVLO)		20	20.8	21.5	V
V_{IN} Turn-Off Voltage	V_{OFF}	V_{IN} falling, ADJ_UVLO unconnected		30			V
V_{IN} Turn-On/Turn-Off Hysteresis	V_{HYST_UVLO}	ADJ_UVLO unconnected (Note 5)		3.2			V
V_{IN} Turn-On/Turn-Off Industrial Hysteresis	V_{HYST_IND}	V_{IN} falling, ADJ_UVLO pulldown to V_{SS}			1.8		V
V_{IN} Deglitch Time	t_{OFF_DLY}	V_{IN} falling from 40V to 20V (Note 6)		30	120		µs
Inrush to Operating Mode Delay	t_{DELAY}	Minimum time period when PG is disconnected from V_{DD} after entering power-on mode		90	100	110	ms
Current-Limit Timer	t_{LIM}	Once in power-on mode, external isolation MOSFET is turned off if current-limit condition persists for t_{LIM} (Note 7)	MAX5992A, MAX5992B	7.2	8	8.8	ms
Restart Timer	$t_{RESTART}$	After external isolation MOSFET is turned off due to a current-limit condition, the device waits $t_{RESTART}$ before reentering inrush mode			1.5		s
RTN Leakage Current	I_{RTN_LKG}	$V_{RTN} - V_{SS}$ = 10V to 60V			60	85	µA
RJ45 12V Mode (MAX5992B)							
RJ45 12V Threshold	V_{TH_RJ45}	V_{IN} rising		8.1	8.7	9.3	V
RJ45 12V Threshold Hysteresis	V_{HYST_RJ45}	V_{IN} falling			1		V
RJ45 12V Turn-On Delay	t_{RJ45}	External isolation MOSFET is turned on if $V_{IN} > V_{TH\_RJ45}$ for more than t_{RJ45}; counter is disabled when $V_{IN} > V_{UVLO}$ or when V_{IN} crosses the RJ45 12V falling threshold			1.8		s
CURRENT LIMIT							
Inrush-Current Limit	V_{INRUSH}	$V_{SENSE} - V_{SS}$, during t_{DELAY} period, $R_{SENSE} = 100m\Omega$		10	15	20	mV
Current-Limit Clamp Voltage (Power-On Mode)	V_{LIM}	After inrush completed, maximum V_{SENSE} during current-limit condition, V_{RTN} = 1V, $R_{SENSE} = 100m\Omega$	CL_SEL unconnected	72	80	88	mV
			CL_SEL pulled down to V_{SS}	170	190	210	

DC Electrical Characteristics (continued)

V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, $R_{\overline{SL}}$ = 60.4kΩ, all other pins unconnected. All voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit in Foldback Conditions	V_{TH_FLBK}	Power-on mode, (V_{RTN} - V_{SS}) > 40V		20		mV
Foldback Start Voltage	V_{FLBK_ST}	Power-on mode, (V_{RTN} - V_{SS})		11		V
SENSE Input Bias Current	I_{INPUT}	V_{SENSE} = V_{SS}	-2		+2	µA
ACTIVE BRIDGE CONTROL						
FET Turn-On Threshold	V_{BRIDGE_ON}	Power-on mode; enabled FETs turn on when V_{SENSE} > V_{BRIDGE_ON} (MAX5992A)		15		mV
External Gate Drive	V_{GS_BRIDGE}	(V_{NDR} - V_{SS}) for nFET, (V_{DD} - V_{PDR}) for pFET	8	9.5	11	V
Gate-Source Resistance	R_{GS_BRIDGE}	For both nFET and pFET		500		kΩ
Input-Voltage Threshold	V_{IN_BRIDGE}	If (V_{IN1} - V_{IN2}) > V_{IN_BRIDGE}, nFET1 and pFET2 turn on; if (V_{IN1} - V_{IN2}) < V_{IN_BRIDGE}, nFET2 and pFET1 turn on		100		mV
LOGIC						
WAD Detection Threshold	$V_{WAD-REF}$	V_{WAD} rising, V_{IN} = 14V to 60V (referenced to RTN), V_{RTN} = V_{SS} = 0V	7.2	8	8.8	V
WAD Detection Threshold Hysteresis		V_{WAD} falling, V_{RTN} = V_{SS} = 0V		0.3		V
WAD Input Current	$I_{WAD-LKG}$	V_{WAD} = 10V (referenced to RTN)			4	µA
$\overline{2EC}$ Sink Current		V_{RTN} = V_{SS} = 0V, V_{WAD} = 10V	1	1.5	2.25	mA
$\overline{2EC}$ Off-Leakage Current		V_{RTN} = V_{WAD}, $V_{\overline{2EC}}$ = 60V	-1		+1	µA
PG Output Voltage	V_{OL}	(V_{DD} - V_{PG}), I_{PG_SINK} = 2mA, V_{IN} > V_{UVLO}			500	mV
PG Off-Leakage Current		V_{PG} = V_{SS}, inrush/sleep/ultra-low-power sleep mode	-1		+1	µA
$\overline{SIG\_OK}$ Input-Voltage Threshold	V_{TH_SIG}	Referenced to V_{SS}; inrush mode is entered when $V_{\overline{SIG\_OK}}$ < V_{TH_SIG}	1.7	2.2	2.7	V
$\overline{SIG\_OK}$ Pulldown Current	$I_{\overline{SIG\_OK}}$	$\overline{SIG\_OK}$ pulldown to V_{SS}	3	5	7	µA
RDCY_SEL, WAD_SEL, CL_SEL, ADJ_UVLO Pullup Current	I_{PU}		3	5	7	µA
RDCY_SEL, WAD_SEL, CL_SEL, ADJ_UVLO Logic-Low	V_{DIG_LOW}		1.1			V
RDCY_SEL, WAD_SEL, CL_SEL, ADJ_UVLO Logic-High	V_{DIG_HIGH}				3.2	V

DC Electrical Characteristics (continued)

V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, R_{CLS} = 615Ω, $R_{\overline{SL}}$ = 60.4kΩ, all other pins unconnected. All voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SLEEP/ULTRA-LOW-POWER SLEEP MODE						
$\overline{ULP}$ Logic Threshold	$V_{TH\_\overline{ULP}}$	$V_{\overline{ULP}}$ rising and falling	2		2.6	V
$\overline{SL}$ Logic Threshold	$V_{TH\_\overline{SL}}$	$V_{\overline{SL}}$ falling	0.55	0.6	0.65	V
$\overline{SL}$ Current		$V_{\overline{SL}}$ = 0V		50		µA
LED Current Amplitude	I_{LED}	$R_{\overline{SL}}$ = 60.4kΩ, V_{DD} - V_{LED} = 4V	9.6	10.7	11.8	mA
		$R_{\overline{SL}}$ = 30.2kΩ, V_{DD} - V_{LED} = 4V	19.2	21.4	23.5	
LED Current Programmable Range			10		20	mA
LED Current with $\overline{SL}$ Connected to V_{SS}		$V_{\overline{SL}}$ = 0V	19.6	26.4	31.5	mA
LED Current Frequency	f_{ILED}	Sleep and ultra-low-power sleep modes		250		Hz
LED Current Duty Cycle	D_{ILED}	Sleep and ultra-low-power sleep modes		25		%
MPS Current Amplitude	I_{MPS}	Sleep and ultra-low-power sleep modes (MAX5992A/MAX5992B); load current less than 150mA (MAX5992A only); current pulses source out from V_{IN1} if V_{IN1} < V_{IN2}; current pulses source out from V_{IN2} if V_{IN2} < V_{IN1} (V_{DD} - V_{IN1}) or (V_{DD} - V_{IN2}) = 4V	10	12	14	mA
MPS Current Duty Cycle	D_{IMPS}	Sleep and ultra-low-power sleep modes		75		%
MPS Current Enable Time	t_{MPS}	Ultra-low-power sleep mode	76	87	98	ms
MPS Current Disable Time	t_{MPDO}	Ultra-low-power sleep mode	205	235	265	ms
$\overline{SL}$ Delay Time	$t_{\overline{SL}}$	Time period $V_{\overline{SL}}$ must remain below the $\overline{SL}$ logic threshold ($V_{TH\_\overline{SL}}$) to enter sleep and ultra-low-power sleep mode (MAX5992B only)	5.7	6.5	7.3	s
THERMAL SHUTDOWN						
Thermal Shutdown	T_{SD}	T_J rising		+150		°C
Thermal Shutdown Hysteresis		T_J falling		20		°C

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 2: The input offset current is illustrated in Figure 1.
Note 3: Effective differential input resistance is defined as the differential resistance between V_{DD} and V_{SS}. See Figure 1.
Note 4: Classification current is turned off whenever the device is in power-on mode.
Note 5: UVLO hysteresis is guaranteed by design, not production tested.
Note 6: A 20V glitch on input voltage that takes V_{DD} below V_{UVLO} shorter than or equal to t_{OFF_DLY} does not cause the devices to exit power-on mode.
Note 7: t_{LIM} is also the timer for the second inrush period when RDCY_SEL is unconnected.

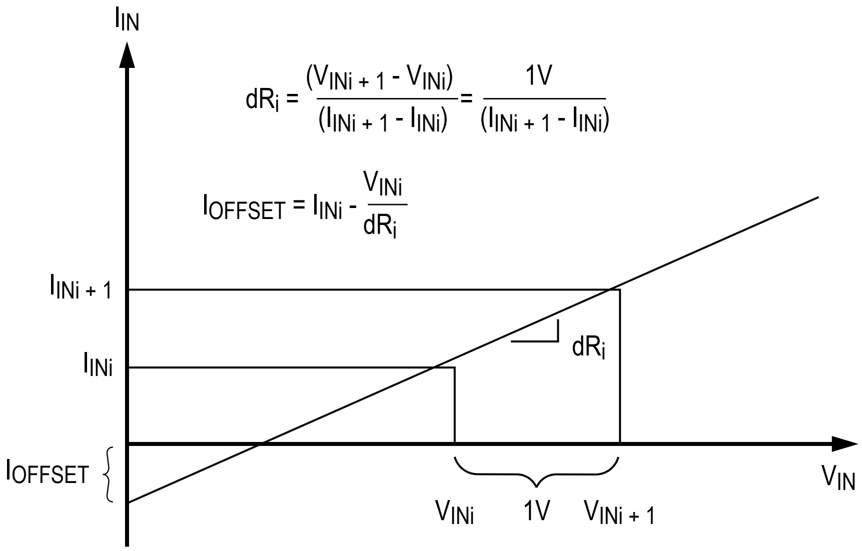
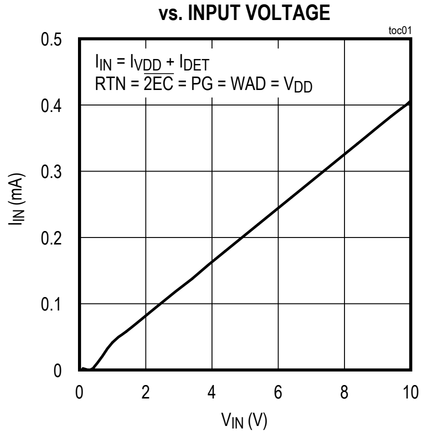


Figure 1. Effective Differential Input Resistance/Offset Current

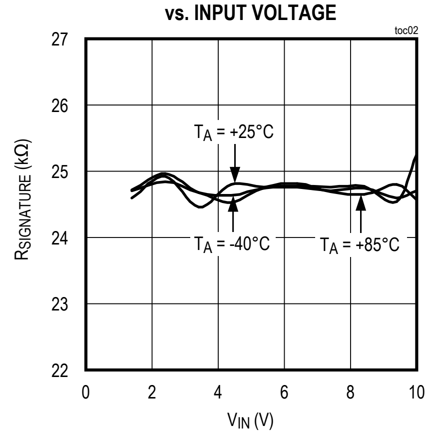
Typical Operating Characteristics

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, $R_{\overline{SL}}$ = 60.4kΩ, all other pins unconnected. All voltages are referenced to V_{SS}.)

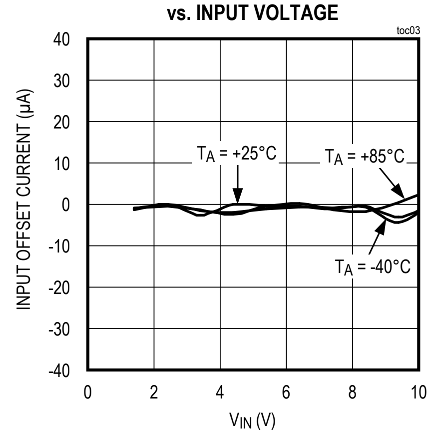
DETECTION CURRENT vs. INPUT VOLTAGE



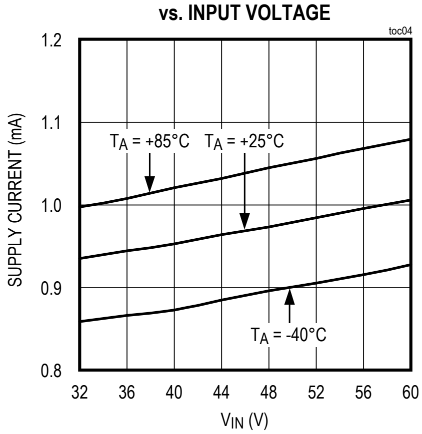
SIGNATURE RESISTANCE vs. INPUT VOLTAGE



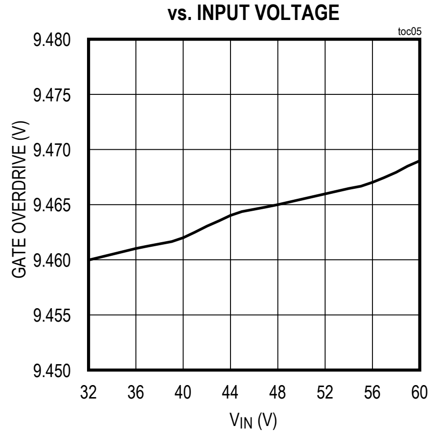
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



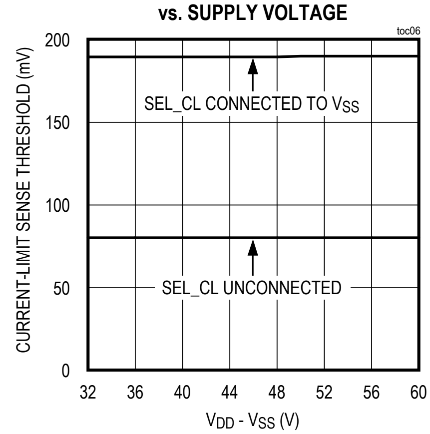
SUPPLY CURRENT vs. INPUT VOLTAGE



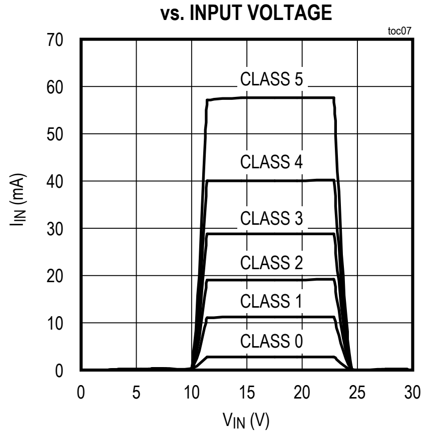
GATE OVERDRIVE VOLTAGE vs. INPUT VOLTAGE



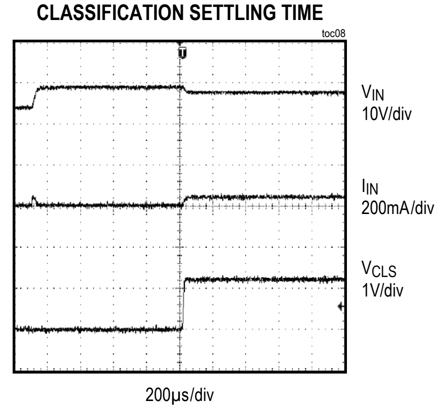
CURRENT-LIMIT SENSE THRESHOLD vs. SUPPLY VOLTAGE



CLASSIFICATION CURRENT vs. INPUT VOLTAGE



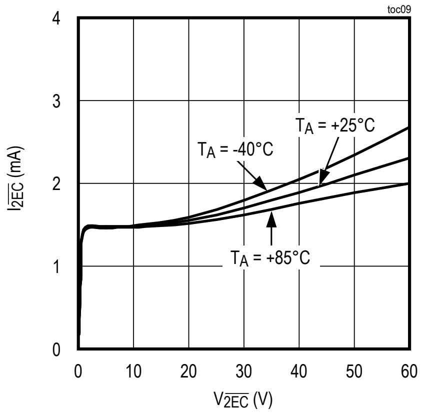
CLASSIFICATION SETTLING TIME



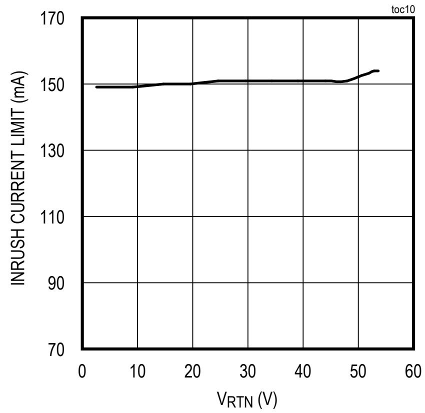
Typical Operating Characteristics (continued)

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{DET} = 24.9kΩ, $R_{\overline{SL}}$ = 60.4kΩ, all other pins unconnected. All voltages are referenced to V_{SS}.)

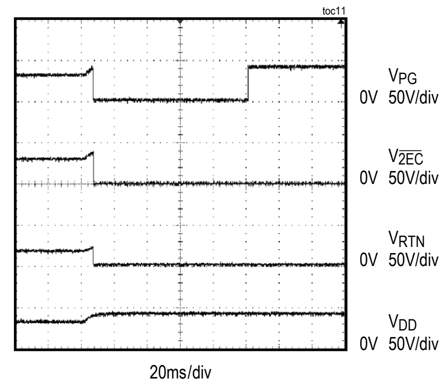
$\overline{2EC}$ SINK CURRENT vs. $\overline{2EC}$ VOLTAGE



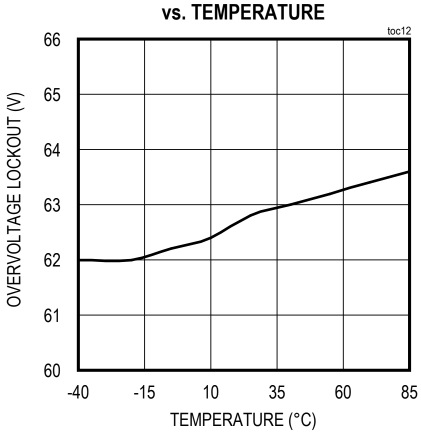
INRUSH CURRENT LIMIT vs. RTN VOLTAGE



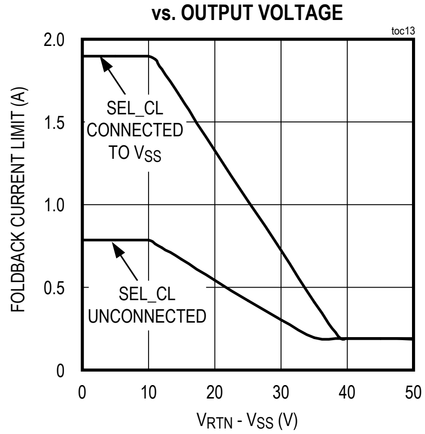
INRUSH CONTROL WAVEFORM WITH TYPE 2 CLASSIFICATION



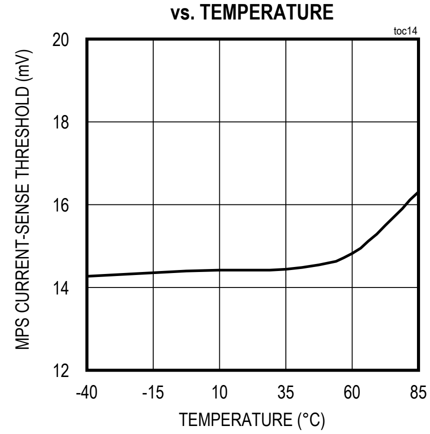
OVERVOLTAGE LOCKOUT vs. TEMPERATURE



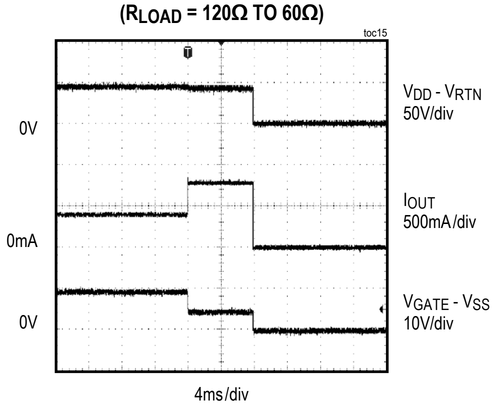
FOLDBACK CURRENT LIMIT vs. OUTPUT VOLTAGE



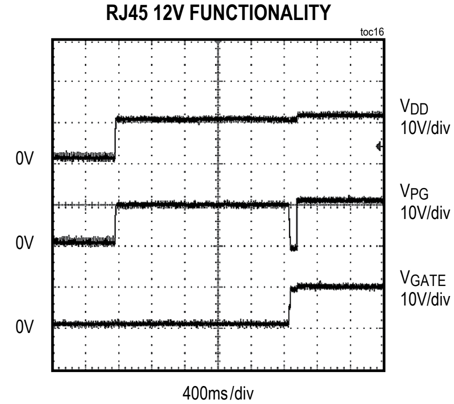
MPS CURRENT-SENSE THRESHOLD vs. TEMPERATURE



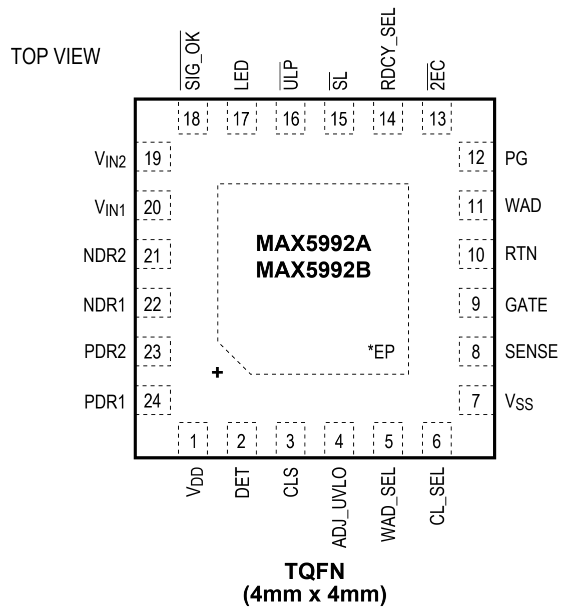
CURRENT-LIMIT TIMEOUT (R_{LOAD} = 120Ω TO 60Ω)



RJ45 12V FUNCTIONALITY



Pin Configuration



*EP = EXPOSED PAD. CONNECT EP TO V_{SS}.

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Input. Connect V_{DD} to the positive output of active FET bridge. The active FET bridge provides a rectified positive supply to V_{DD}. Connect a 68nF (min) bypass capacitor between V_{DD} and V_{SS}.
2	DET	Detection Resistor Input. Connect a detection resistor (R_{DET} = 24.9kΩ) from DET to V_{SS}.
3	CLS	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLS to V_{SS} to set the desired classification current. See the classification current specifications in the *Electrical Characteristics* table to find the resistor value for a particular PD classification.
4	ADJ_UVLO	UVLO Select Input. The state of ADJ_UVLO sets the UVLO threshold of the device. Leave ADJ_UVLO unconnected to set the PoE UVLO threshold. Connect ADJ_UVLO to V_{SS} to set the industrial UVLO threshold (see the *Electrical Characteristic* table for details).
5	WAD_SEL	WAD Behavior Select Input. When WAD_SEL is left unconnected, the device sources power from the WAD when a wall adapter is detected at the WAD input. When WAD_SEL is connected to V_{SS}, the device sources power from the WAD only when the wall adapter voltage is higher than the PoE voltage.
6	CL_SEL	Power-On Current-Limit Select Input. Leave CL_SEL unconnected to set the 800mA current limit. Connect CL_SEL to V_{SS} to set the 1.9A current limit.

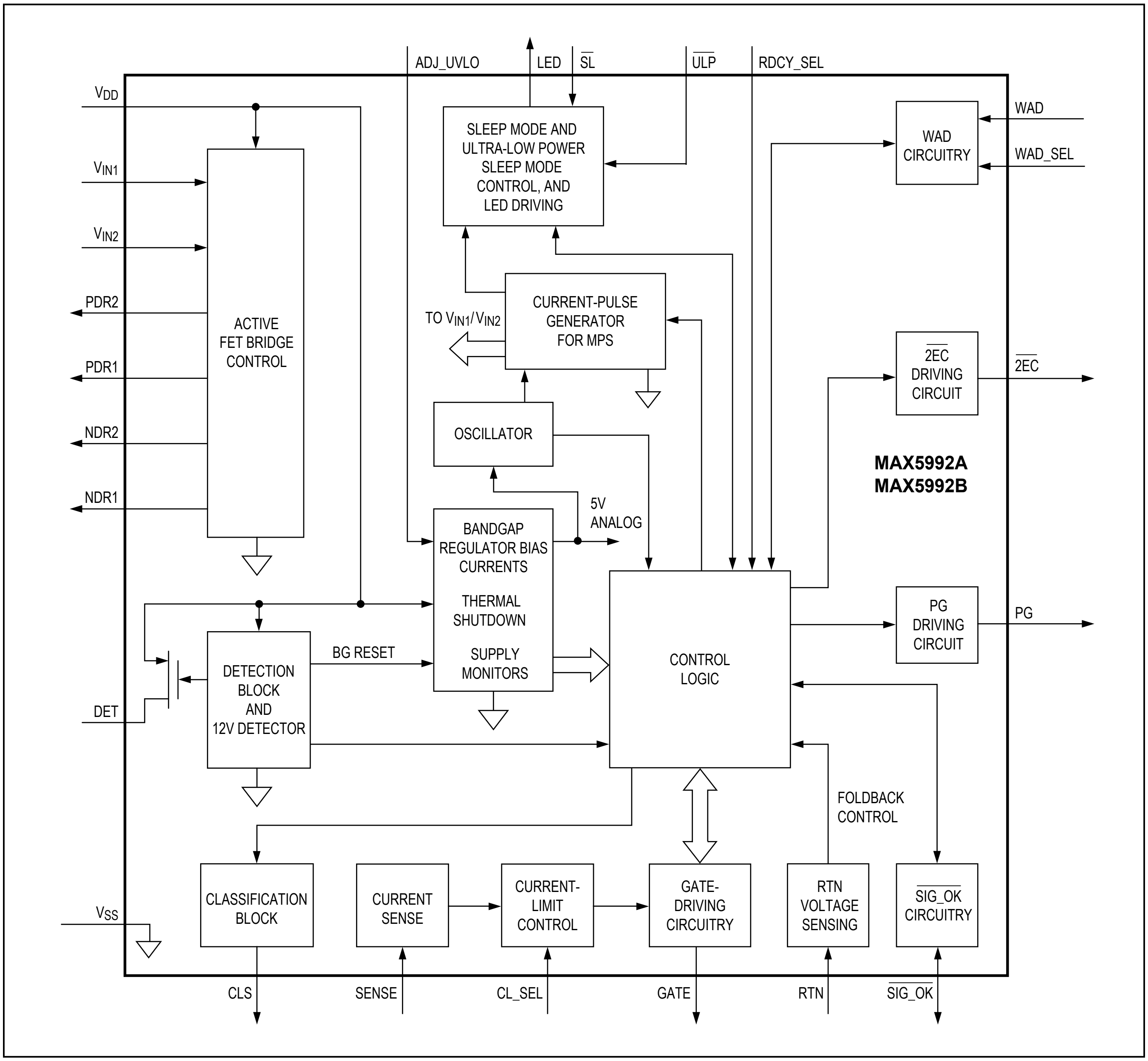
Pin Description (continued)

PIN	NAME	FUNCTION
7	V_{SS}	Negative Supply Input. Connect V_{SS} to the negative output of the active FET bridge. The active FET bridge provides a rectified negative supply to V_{SS}.
8	SENSE	Current-Sense Positive Terminal Input. Connect SENSE to the source of the external isolation MOSFET and connect a 100mΩ current-sense resistor between SENSE and V_{SS}.
9	GATE	Isolation MOSFET Gate Control Output. Connect GATE to the gate of the external isolation MOSFET.
10	RTN	Drain-Sense Input. RTN is a voltage-sensing input. Connect RTN to the drain of the external isolation MOSFET. In multi-PD redundancy/FTTH/FTTB applications, connect RTN to an isolation diode. Connect RTN to the downstream DC-DC converter ground, as shown in the *Typical Application Circuits*.
11	WAD	Wall Power Adapter Detector Input. Wall adapter detection is enabled the moment V_{DD} - V_{SS} crosses the mark event threshold. Detection occurs when the voltage from WAD to RTN is greater than 8V. When a wall power adapter is present, the isolation MOSFET turns off (unless WAD_SEL is asserted low) and $\overline{\text{2EC}}$ current sink turns on. Connect WAD directly to RTN when the wall power adapter or other auxiliary power source is not used.
12	PG	Power-Good Indicator Output. PG is referenced to V_{DD}. Use PG to drive DC-DC converter's enable pin, connect a resistor-divider from PG to RTN to obtain the required voltage. See the *Typical Application Circuits*.
13	$\overline{\text{2EC}}$	2-Event Classification Detect or Wall Adapter Detect Output. A 1.5mA current sink is enabled at $\overline{\text{2EC}}$ when a Type 2 PSE or a wall adapter is detected. When powered by a Type 2 PSE, the $\overline{\text{2EC}}$ current sink is enabled after the isolation MOSFET is fully on until V_{IN} drops below the UVLO threshold. $\overline{\text{2EC}}$ is latched when powered by a Type 2 PSE until V_{IN} drops below the reset threshold. $\overline{\text{2EC}}$ also asserts when a wall adapter supply, typically greater than 9V, is applied between WAD and RTN. The $\overline{\text{2EC}}$ current sink is turned off when the device is in sleep mode.
14	RDCY_SEL	Redundancy-Select Input. The state of the RDCY_SEL input determines the inrush-current control behavior of the device. Leave RDCY_SEL unconnected for nonredundancy applications. Connect RDCY_SEL to VSS for redundancy or FTTH/FTTB applications.
15	$\overline{\text{SL}}$	Sleep Mode Enable Input. $\overline{\text{SL}}$ referenced to V_{SS}. For the MAX5992A, a falling edge on $\overline{\text{SL}}$ ($V_{\overline{SL}}$ must drop below $V_{TH\_\overline{SL}}$) brings the device into sleep mode. For the MAX5992B holding $V_{\overline{SL}} < V_{TH\_\overline{SL}}$ for a period of 6.5s brings the device into sleep mode. $\overline{\text{SL}}$ is also used to set the LED current. An external resistor ($R_{\overline{SL}}$) connected between $\overline{\text{SL}}$ and V_{SS} sets the LED current (I_{LED}).
16	$\overline{\text{ULP}}$	Ultra-Low-Power Sleep Enable/Wake Input. $\overline{\text{ULP}}$ is referenced to V_{SS}. $\overline{\text{ULP}}$ is used in combination with $\overline{\text{SL}}$ as an ultra-low-power sleep mode input. For the MAX5992A, a falling edge on $\overline{\text{SL}}$ (while $\overline{\text{ULP}}$ is asserted low) enables ultra-low-power sleep mode. For the MAX5992B hold $\overline{\text{SL}}$ logic-low for a period of 6.5s (while $\overline{\text{ULP}}$ is asserted low) to enable ultra-low-power sleep mode. $\overline{\text{ULP}}$ also functions as a wake input. When the device is in sleep or ultra-low-power sleep mode, a falling edge on $\overline{\text{ULP}}$ brings the device back into the normal operating mode (wake mode).

Pin Description (continued)

PIN	NAME	FUNCTION
17	LED	LED Driver Output. Connect one or more LED from LED to V_{SS}. During sleep mode, ultra-low-power sleep mode and MPS enabled period, LED sources a periodic current (I_{LED}) at 250Hz frequency with 25% duty cycle. The amplitude of I_{LED} is set by $R_{\overline{SL}}$ according to the formula I_{LED} (in A) = 645.75/($R_{\overline{SL}}$ + 1200). Connect the LED pin to V_{SS} if no LED is required; do not leave the LED pin unconnected.
18	$\overline{\text{SIG\_OK}}$	Signal-OK Input/Output. $\overline{\text{SIG\_OK}}$ is internally pulled up to V_{DD}. $\overline{\text{SIG\_OK}}$ asserts when V_{IN} is rising and (V_{IN} > V_{UVLO}). When $V_{\overline{SIG\_OK}}$ drops below the V_{TH_SIG} (with reference to V_{SS}), the external isolation MOSFET is turned on and inrush mode is active. In 2x2P PD application, connect $\overline{\text{SIG\_OK}}$ to another device's $\overline{\text{SIG\_OK}}$ pin. Leave $\overline{\text{SIG\_OK}}$ unconnected in any other application.
19	V_{IN2}	Active FET Bridge Input 2. Connect a 100Ω resistor from V_{IN2} to the output of the RJ45 connector. V_{IN2} is a voltage-sensing input. Depending on the polarity of V_{IN1} and V_{IN2}, the device turns on the corresponding nFETs and pFETs of the active FET bridge. If V_{IN2} < V_{IN1}, V_{IN2} is used to provide a current pulse to the PSE when MPS is enabled.
20	V_{IN1}	Active FET Bridge Input 1. Connect a 100Ω resistor from V_{IN1} to the output of the RJ45 connector. V_{IN1} is a voltage-sensing input. Depending on the polarity of V_{IN1} and V_{IN2}, the device turns on the corresponding nFETs and pFETs of the active FET bridge. If V_{IN1} < V_{IN2}, V_{IN1} is used to provide a current pulse to the PSE when MPS is enabled.
21	NDR2	Active FET Bridge nFET2 Gate-Control Output. Connect NDR2 to the gate of the nFET2 in the active bridge.
22	NDR1	Active FET Bridge nFET1 Gate-Control Output. Connect NDR1 to the gate of the NFET1 in the active bridge.
23	PDR2	Active FET Bridge pFET2 Gate-Control Output. Connect PDR2 to the gate of the pFET2 in the active FET bridge.
24	PDR1	Active FET Bridge pFET1 Gate-Control Output. Connect PDR1 to the gate of the pFET1 in the active FET bridge.
—	EP	Exposed Pad. Do not use EP as an electrical connection to V_{SS}. EP is internally connected to V_{SS} through a resistive path and must be connected to V_{SS} externally. To optimize power dissipation, solder the exposed pad to a large copper power plane. Do not leave EP unconnected.

Simplified Block Diagram



Detailed Description

PD Operating Modes

Depending on the input voltage ($V_{IN} = V_{DD} - V_{SS}$), the MAX5992A/MAX5992B devices operate in three different modes: PD detection, PD classification, and PD power-on. The devices enter PD detection mode when the input voltage is between 1.4V and 10.1V. The devices enter PD classification mode when the input voltage is between 12.6V and 20.5V. The devices enter PD power-on mode once the input voltage exceeds V_{UVLO}.

Detection Mode (1.4V ≤ V_{IN} ≤ 10.1V)

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the 1.4V to 10.1V range (1V step minimum) and then records the current measurements at the two points. The PSE then computes ΔV/ΔI to ensure the presence of the 24.9kΩ signature resistor. Connect the signature resistor (R_{DET}) from DET to V_{SS} for proper signature detection. The devices pull DET to V_{DD} in detection mode and pull down to V_{SS} when the input voltage exceeds 12.5V. In detection mode, most of the devices' internal circuitry is off and the offset current is less than 10μA.

If the voltage applied to the PD is reversed, install protection diodes at the input terminal to prevent internal damage to the devices (see the *Typical Application Circuits*). Since the PSE uses a slope technique (ΔV/ΔI) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode (12.5V ≤ V_{IN} ≤ 20.5V)

In the classification mode, the PSE classifies the PD based on the power consumption required by the PD. This allows the PSE to efficiently manage power distribution.

Class 0 to Class 5 is defined as shown in Table 1. (The IEEE 802.3af/at standard defines only Class 0–Class 4. Class 5 is for any special requirement.) An external resistor (R_{CLS}) connected from CLS to V_{SS} sets the classification current.

The PSE determines the class of a PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.5V and 20.5V, the devices exhibit a current characteristic with a value shown in Table 1. The PSE uses the classification current information to classify the power requirement of the PD. The classification current includes the current drawn by R_{CLS} and the supply current of the devices so the total current drawn by the PD is within the IEEE 802.3af/at standard figures. The classification current is turned off whenever the devices are in power-on mode.

2-Event Classification and Detection

During 2-Event classification, a Type 2 PSE probes the PD for classification twice. In the first classification event, the PSE presents an input voltage between 12.5V and 20.5V and the devices present the programmed load I_{CLASS}. The PSE then drops the probing voltage below the mark event threshold of 10.8V and the devices present the mark current (I_{MARK}). This sequence is repeated one more time.

Table 1. Setting Classification Current

CLASS	MAXIMUM POWER USED BY PD (W)	R_{CLS} (Ω)	V_{IN}* (V)	CLASS CURRENT SEEN AT V_{IN} (mA)		IEEE 802.3at PD CLASSIFICATION CURRENT SPECIFICATION (mA)	
				MIN	MAX	MIN	MAX
0	0.44 to 12.95	615	12.5 to 20.5	0	3.96	0	5
1	0.44 to 3.84	118	12.5 to 20.5	9.12	11.88	8	13
2	3.84 to 6.49	69.8	12.5 to 20.5	17.2	19.8	16	21
3	6.49 to 12.95	45.3	12.5 to 20.5	26.3	29.7	25	31
4	12.95 to 25.5	30.9	12.5 to 20.5	36.4	43.6	35	45
5	> 25.5	21.5	12.5 to 20.5	52.7	63.3	51	68

**V_{IN} is measured across the devices' input V_{DD} to V_{SS}.*

When the devices are powered by a Type 2 PSE, the 2-Event identification output $\overline{\text{2EC}}$ asserts low after the external isolation n-channel MOSFET is fully turned on. $\overline{\text{2EC}}$ current sink is turned off when V_{IN} goes below the UVLO threshold (V_{OFF}) and turns on when V_{IN} goes above the UVLO threshold (V_{ON}), unless V_{IN} goes below V_{THR} to reset the latched output of the Type 2 PSE detection flag.

Alternatively, the $\overline{\text{2EC}}$ output also serves as a wall adapter detection output when the devices are powered by an external wall power adapter. See the *Wall Power Adapter Detection and Operation* section for more information.

Power-On Mode (Wake Mode)

The devices enter power-on mode when V_{IN} rises above the undervoltage-lockout threshold (V_{ON}). When V_{IN} rises above V_{ON}, the devices turn on the external isolation MOSFET to connect V_{SS} to RTN with inrush current limit. The isolation MOSFET is fully turned on when the voltage at RTN is near V_{SS} and the inrush current is reduced below the inrush limit. Once the isolation MOSFET is fully turned on and enters the power-on state, the devices change the current limit to power-on current limit. When the RDCY_SEL is pulled down to V_{SS}, a 2-level inrush-current limit kicks in if current limit persists after the 100ms inrush-current limit times out.

Undervoltage Lockout

The devices operate from a 12V to 60V supply voltage with a different UVLO threshold. When the input voltage is above the threshold, $\overline{\text{SIG\_OK}}$ is asserted, the devices power up, and the external isolation MOSFET is turned on.

A UVLO select input (ADJ_UVLO) is used to set the turn-on voltage. Leave ADJ_UVLO unconnected to select the PoE turn-on voltage. The MAX5992A has a 38.6V turn-on voltage, while the MAX5992B has a 35.4V turn-on voltage. When the input voltage goes below V_{OFF} for more than t_{OFF_DLY}, the external isolation MOSFET turns off. Connect ADJ_UVLO to V_{SS} to select the 20.8V industrial turn-on voltage.

Power-On Current Limit

The devices have a selectable power-on current limit with foldback control. The power-on current limit is selected by the CL_SEL input. Leave CL_SEL unconnected to select the 0.8A current limit. Connect CL_SEL to V_{SS} to select the 1.9A current limit. If a current-limit condition persists for more than t_{LIM} (8ms), the devices turn off the isolation MOSFET. The devices reenter power-on mode with inrush current-limit control after 1.5s.

Foldback Current

During startup and normal operation, an internal circuit senses the voltage at V_{SENSE}. When necessary, the devices reduce the current-limit clamp voltage (V_{LIM}) to help reduce the power dissipation through the external isolation MOSFET. Foldback begins when (V_{RTN} - V_{SS}) > 11V. The V_{LIM} eventually reduces down to the minimum current-limit threshold (V_{TH_FLBK} = 20mV) when V_{RTN} - V_{SS} > 40V (Figure 2). Foldback current is disabled during the inrush period.

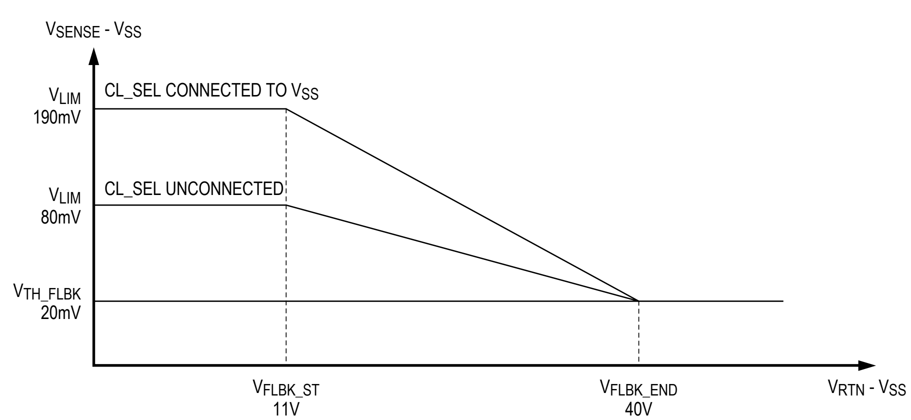


Figure 2. Foldback Current Characteristics

Sleep Mode and Ultra-Low-Power Sleep Mode

The devices feature a sleep mode that reduces the power consumption while maintaining the power signature of the standard. The devices release the pullup switch from PG to V_{DD} while keeping the external n-channel isolation MOSFET turned on. The active FET bridge is turned off (except for the MAX5992B). The PG output disables downstream DC-DC converters, reducing the power consumption of the overall PD system. The LED driver output (LED) sources periodic current pulses. The LED current I_{LED} is set by an external resistor $R_{\overline{SL}}$ (see the *LED Driver* section). To enable sleep mode, apply a falling edge to $\overline{SL}$ (MAX5992A) or hold $\overline{SL}$ low for a minimum of 6.5s after a falling edge (MAX5992B). Apply a falling edge to $\overline{ULP}$ and the devices exit sleep mode.

The ultra-low-power sleep mode allows the devices to further reduce power consumption while still maintaining the power signature of the standard. The ultra-low-power sleep input ($\overline{ULP}$) is internally held high with a 50kΩ pullup resistor to the internal 5V bias of the devices. Set $\overline{ULP}$ to logic-low and apply a falling edge to $\overline{SL}$ to enable ultra-low-power sleep mode. Apply a falling edge to $\overline{ULP}$, so the devices exit ultra-low-power sleep mode and resume normal operation.

Maintain Power Signature (MPS) (MAX5992A)

The MAX5992A provides a MPS to sink current from upstream PSE to maintain power on. The MPS current is generated to comply with the IEEE 802.3af/3at standard for PSE to stay on. When MPS is enabled, the devices turn off the active FET bridge, pulse LED current, and keep the external isolation MOSFET on. PG is pulled up to V_{DD} when MPS is enabled in power-on mode.

150mA Load Current Check (MAX5992A)

The MAX5992A features a 150mA load current check function. In power-on mode, when the load current drops below 150mA, the devices turn off the active FET bridge and enable MPS. This is to prevent the PoE from being back-powered by higher voltage adaptor and consequently being damaged in PoE.

Active FET Bridge Controller

The devices contain two pairs of nFET/pFET drivers to control an external active FET bridge. The active FET bridge provides input polarity protection for V_{DD} and V_{SS} before the PD is powered on. The devices turn on the active FET bridge in the power-on mode (after inrush current). The MAX5992B turns on the active FET bridge to reduce the power loss once the PD is powered on. The MAX5992A do not turn on the active FET bridge until the PD port current exceeds the 150mA threshold.

Depending on the polarity of V_{IN1} and V_{IN2}, the active FET bridge drivers turn on the corresponding path to provide the correct polarity for the devices. If (V_{IN1} - V_{IN2}) > V_{IN_BRIDGE}, then pFET1 and nFET 2 are turned on. If (V_{IN2} - V_{IN1}) > V_{IN_BRIDGE}, then pFET2 and nFET1 are turned on (Figure 3).

The MAX5992A turns off the active FET bridge in sleep mode and ultra-low-power sleep mode. The MAX5992A also turns off the active FET bridge when MPS is enabled due to load-current drops below 150mA.

Isolation MOSFET GATE Driver

Connect the gate of the external n-channel MOSFET to GATE. An internal 50µA current source pulls GATE to (V_{SS} + 10V) to turn on the MOSFET. An internal 40µA current source pulls down GATE to V_{SS} to turn off the MOSFET.

The pullup and pulldown current controls the maximum slew rate at the output during turn-on or turn-off. Use the following equation to set the maximum slew rate:

$$\frac{\Delta V_{RTN}}{\Delta t} = \frac{I_{GATE}}{C_{GD}}$$

where C_{GD} is the total capacitance between the gate and the drain of the external MOSFET.

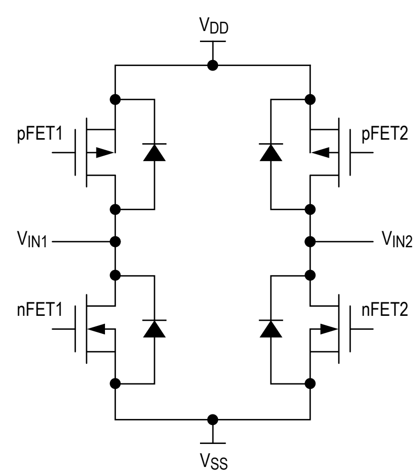


Figure 3. Active FET Bridge

The current limit and capacitive load at the drain control the slew rate during startup. During current-limit regulation, the device manipulates the GATE voltage to control the voltage at SENSE (V_{SENSE}). A fast pulldown activates if V_{SENSE} overshoots the limit threshold (V_{LIM}). The fast pulldown current increases with the amount of overshoot, and the maximum fast pulldown current is 44mA.

During turn-off, when the GATE voltage reaches a value lower than 1.2V, a strong pulldown switch is activated to keep the MOSFET securely off.

Nonredundancy/Redundancy Inrush-Current Control

The devices contain a redundancy-select input (RDCY_SEL) to control the inrush-current behavior. For redundancy applications, connect RDCY_SEL to V_{SS}. For nonredundancy applications, leave RDCY_SEL unconnected.

In nonredundancy mode, the devices turn on the external isolation MOSFET to connect RTN to V_{SS} with inrush-current limit (internally set to 150mA) for 100ms. In redundancy applications, the devices extend a second 100ms with a 2-level inrush current-limit scheme to ensure the load is powered in the absence of the supplying power source (while the PD is taking over to supply the power).

RDCY_SEL Unconnected (Nonredundancy)

The devices provide a 150mA inrush-current limit with a 100ms timeout during startup. If the inrush current-limit condition is removed within the 100ms period, the devices switch to the power-on current-limit control.

If inrush-current limit times out and inrush-current limit persists, then the devices enable a second 150mA inrush current-limit period. The MAX5992A/MAX5992B have a 8ms second inrush period. At the end of the second inrush period, if the inrush current-limit condition persists, then the devices turn off the isolation MOSFET. The devices reenter inrush current-limit control after 1.5s.

RDCY_SEL Connected to V_{SS} (Redundancy)

The MAX5992A turns on the external isolation MOSFET to connect V_{SS} to RTN with the inrush-current limit (internally set to 150mA) for a 100ms period. If the inrush current-limit condition is removed within the 100ms period, then the devices switch to the power-on current-limit control.

If the inrush-current limit times out and the inrush-current limit persists, then the devices enable a second 100ms inrush current-limit period with a 2-level current limit (0.8A or 1.9A, determined by the state of CL_SEL). Within the second 100ms period, if the inrush current-limit condition is removed, then the devices switch to the power-on current-limit control. At the end of the second 100ms period, if the inrush current-limit condition persists, then the devices turn off the isolation MOSFET. The devices reenter inrush current-limit control after 1.5s.

LED Driver

The devices drive an LED connected from the output LED to V_{SS}. During sleep mode/ultra-low-power sleep mode, the LED is driven by current pulses with the amplitude set by the resistor connected from $\overline{SL}$ to V_{SS}. The MAX5992A also turns on the LED when the port current is less than 150mA. Connect the LED pin to V_{SS} if no LED is required; do not leave the LED pin unconnected.

The LED driver current amplitude is programmable from 10mA to 20mA using $R_{\overline{SL}}$ according to the following formula:

$$I_{LED} = 645.75/(R(_{SL}) + 1200) \text{ (in amperes)}$$

Power-Good Output (PG)

PG is an active-high logic output. PG is disconnected from V_{DD} for a period of t_{DELAY} and until the external isolation MOSFET is fully turned on. Connect PG to RTN with a resistor-divider to obtain a turn-on threshold to enable/disable the downstream DC-DC converter. For 2x2PD or multi-PD redundancy applications, connect the two PGs together.

Thermal-Shutdown Protection

The devices include thermal protection from excessive heating. If the junction temperature exceeds the thermal-shutdown threshold of +150°C, the devices turn off the external power MOSFET, LED driver, and $\overline{2EC}$ current sink. When the junction temperature falls below +130°C, the devices enter inrush mode and then return to the power-on mode.

Wall Power Adapter Detection and Operation

For applications where an auxiliary power source such as a wall power adapter is used to power the PD, the devices feature wall power adapter detection. The devices have two selectable wall power adapter behaviors for different applications. A WAD behavior select input (WAD_SEL) is used to select between the two wall power adapter behaviors.

Once the wall power adapter voltage (V_{WAD} - V_{RTN}) exceeds the WAD detection threshold, the devices respond to the WAD_SEL configuration. The devices support adapter voltage from 9V to 57V.

WAD_SEL Unconnected

The devices give highest priority to the wall adapter to power the load in seamless power transition. The external isolation MOSFET turns off, $\overline{2EC}$ current sink turns on, and the classification current is disabled if V_{IN} is in the classification range.

WAD_SEL Connected to V_{SS}

While the PSE is supplying the power to the PD, the wall adaptor is plugged in. The devices allow the highest voltage source to deliver power to the load. When wall adapter voltage is higher than PoE voltage, the devices smoothly switch the power from PoE to wall adapter. The devices turn off active FET bridge and enable MPS current to keep PSE power on. The isolation external MOSFET remains on. After the wall adapter is unplugged, the PoE continues supplying power to the load in seamless power transition.

Overvoltage Protection

The devices contain an overvoltage-protection feature. An internal overvoltage circuit turns off the external isolation MOSFET when V_{DD} - V_{SS} exceeds 66V.

$\overline{SIG\_OK}$

The devices contain a signal-OK input/output ($\overline{SIG\_OK}$) for communication between two devices in 2x2P applications. In 2x2P applications, connect the $\overline{SIG\_OK}$ pin of the two devices together. After both devices are powered up, the $\overline{SIG\_OK}$ asserts low and the external isolation MOSFET turns on. Leave $\overline{SIG\_OK}$ unconnected in all other applications (Figure 5).

Applications Information

2x2 PD Operation

The devices are able to operate in a 2x2P configuration through a single 8-wire Ethernet cable, where two PDs provide power to the DC-DC converter. The two PDs pass detection and classification separately and provide power when both are ready. After the first PD passes the detection and classification, it enables MPS to upstream PSE while waiting for the second PD to pass the detection and classification. The two PDs start to turn on its own external isolation MOSFET once the two $\overline{SIG\_OK}$ pins are pulled down to V_{SS}. After both of the external isolation MOSFETs are fully enhanced, PG is asserted to enable the DC-DC converter.

Multi-PD Redundancy/FTTH/FTTB

The MAX5992A can be used in multi-PD redundancy applications where more than one PoE sets (PSE and PD) are available and ORing together to provide uninterrupted power for mission-critical equipment. Only the PoE set with the higher port voltage provides power to the load. The other PoE set is in standby and takes over to supply power only when the supplying PoE is absent (Figure 6).

The MAX5992A features a redundancy inrush control scheme to avoid output power collapses during the power-supply transition from one PoE set to another PoE set (see the *Nonredundancy/Redundancy Inrush-Current Control* section).

PCB Layout Considerations

Careful PCB layout is critical to achieve high efficiency and low EMI. Follow these layout guidelines for optimal performance:

1) Place the high-frequency input bypass capacitor (68nF ceramic capacitor from V_{DD} to V_{SS} as close as possible to the device.
2) Use large SMT component pads for power-dissipating devices such as the MAX5992A/MAX5992B and the external MOSFETs and sense resistors in the high-power path.
3) Use short, wide traces whenever possible for high-power paths.
4) Use the MAX5992 evaluation kit as a design and layout reference.
5) The exposed pad (EP) must be soldered evenly to the PCB ground plane (V_{SS}) for proper operation and power dissipation. Use multiple vias beneath the exposed pad for maximum heat dissipation. A 1.0mm to 1.2mm pitch is the recommended spacing for these vias and should be plated (1oz copper) with a small barrel diameter (0.30mm to 0.33mm).
6) For the best accuracy current sensing, use Kelvin-sense techniques for the SENSE and V_{SS} inputs in the PCB layout. The high-side sensing should be done from the end of the high-side sense resistor pad, and the V_{SS} should be routed from the end of the low-side sense resistor pad. To minimize the impact from additional series resistance, the two end points should be as close as possible, and sense trace length should be minimized (refer to the MAX5994 evaluation kit for a design example).

Typical Application Circuits

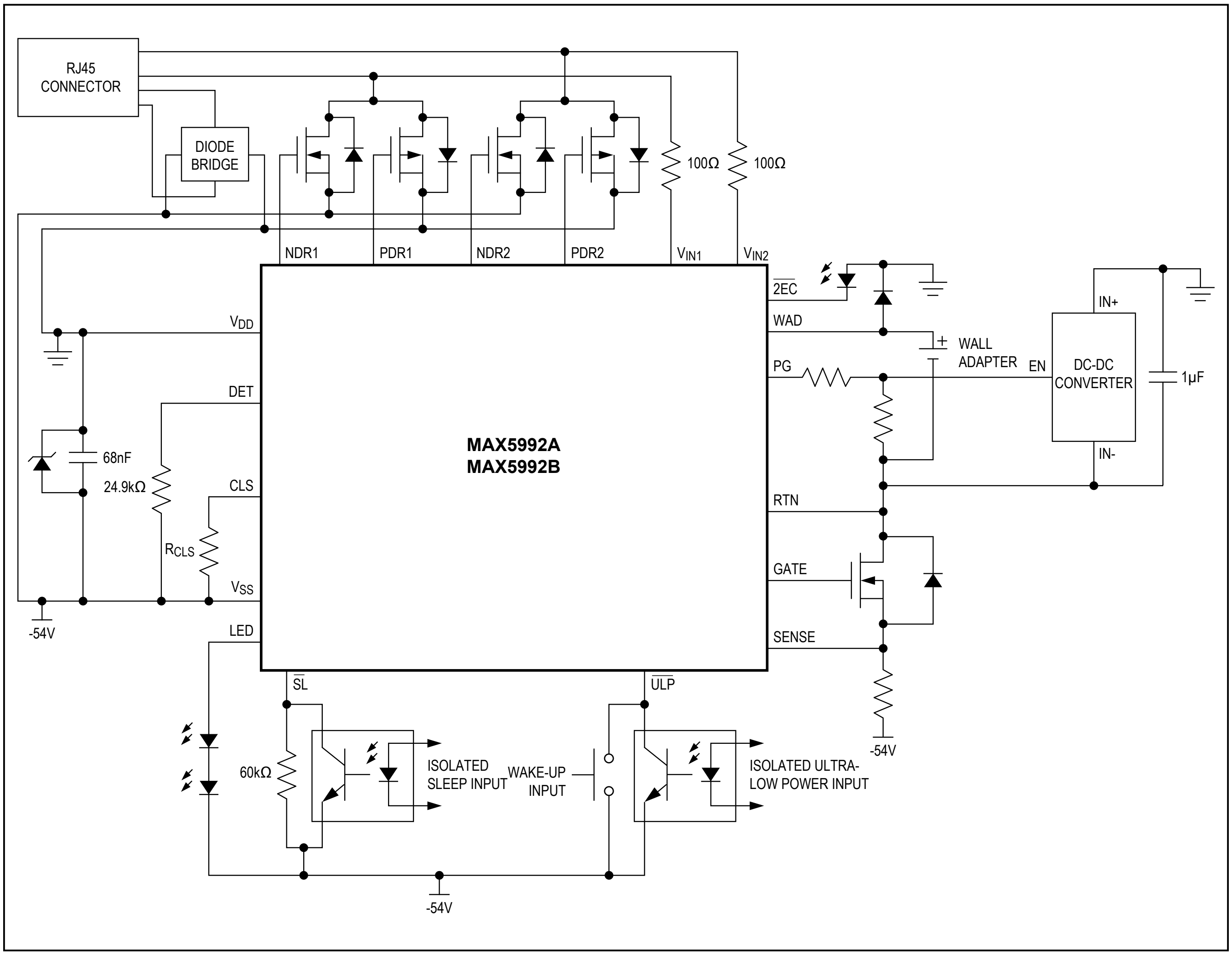


Figure 4. Single PD Application

Typical Application Circuits (continued)

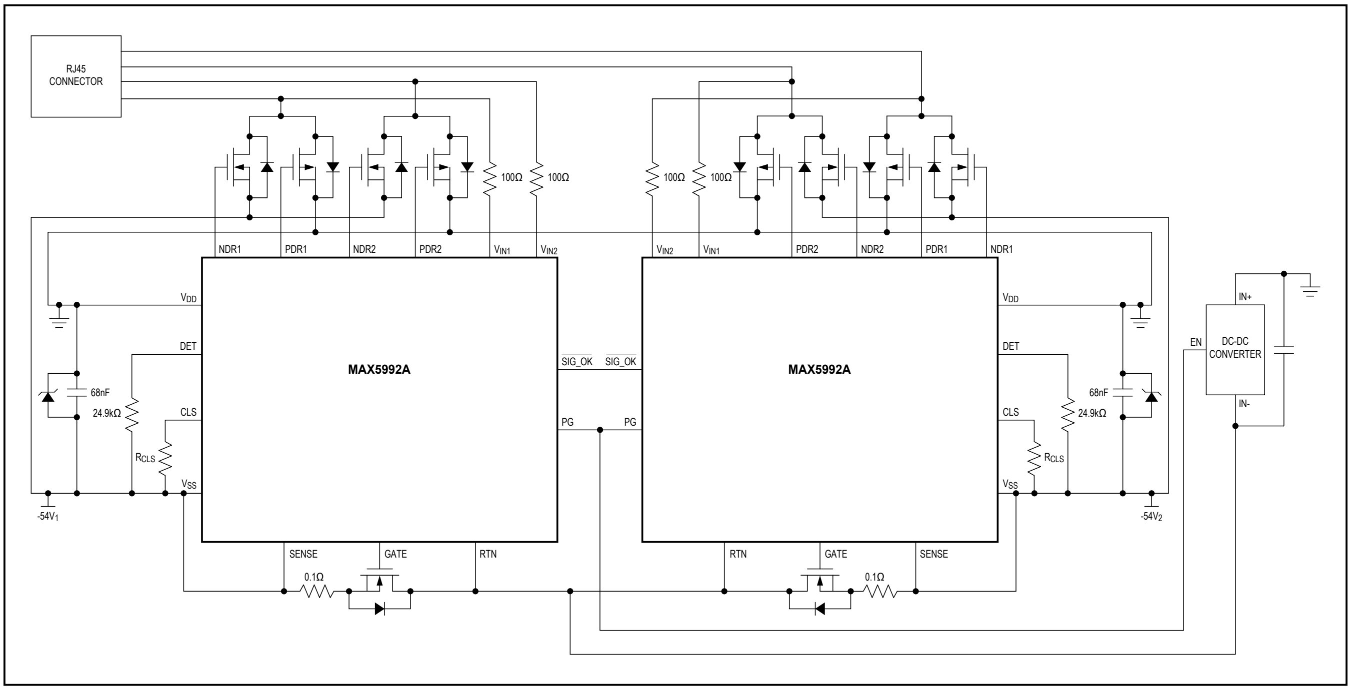


Figure 5. 2x2P PD Application

Typical Application Circuits (continued)

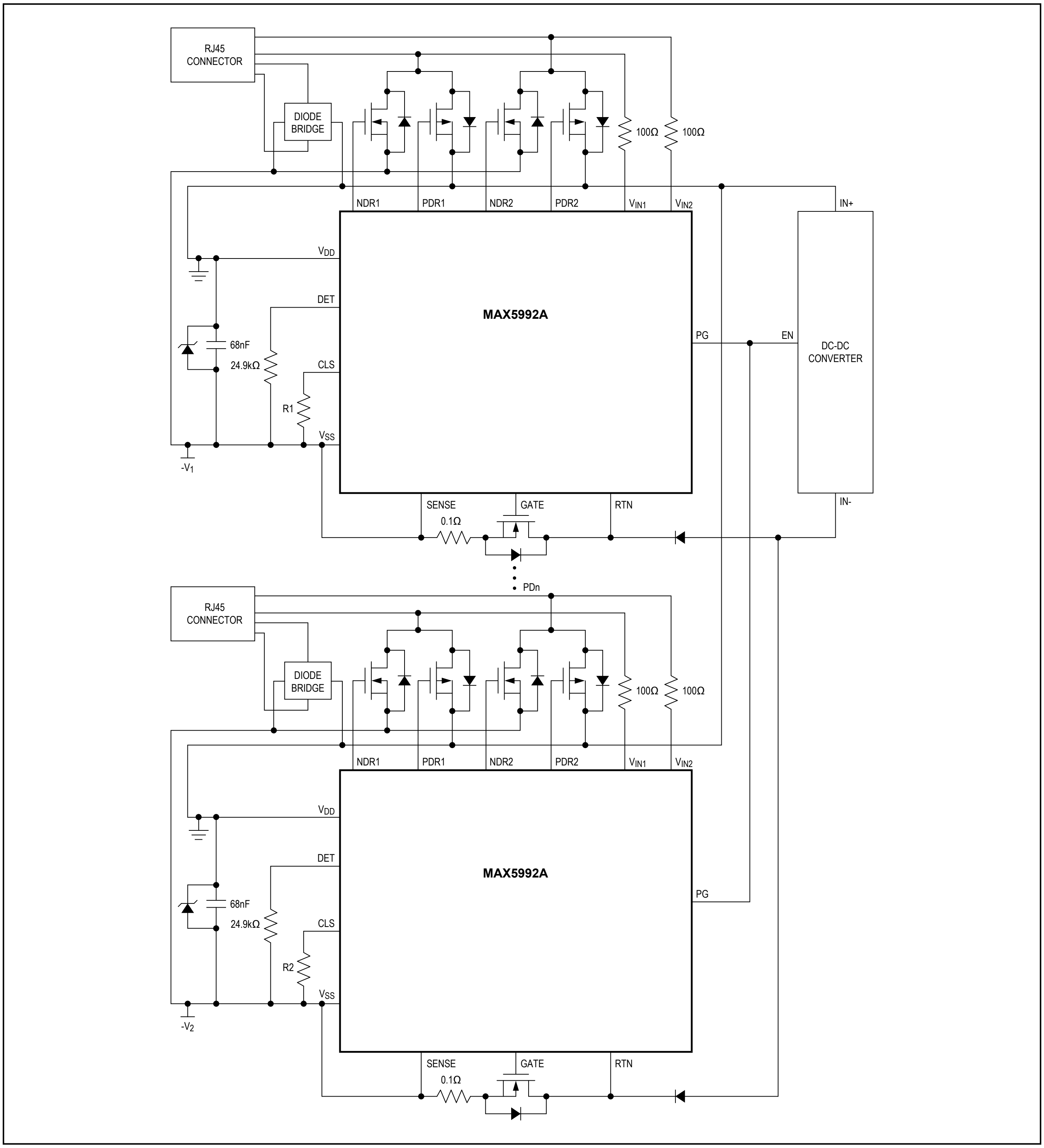


Figure 6. Multi-PD Redundancy Application

Ordering Information/Selector Guide

PART	PIN-PACKAGE	APPLICATION	PoE UVLO (V)	6.5s $\overline{SL}$ DELAY	150mA CHECK	CURRENT LIMIT TIMER	RJ45 12V APPLICATION
MAX5992AETG+	24 TQFN-EP*	High Power	38.6	No	Enable	8ms	Disable
MAX5992BETG+	24 TQFN-EP*	Standard Power	35.4	Yes	Disable	8ms	Disable

Note: *All devices operate over the -40°C to +85°C temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T2444+4	**21-0139**	**90-0028**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/13	Initial release	—
1	2/17	Updated *General Description* and *Absolute Maximum Ratings* sections, and *Electrical Characteristics* table	1–2, 3–5
2	3/18	Updated *Package Information* and *DC Electrical Characteristics* table	2–3
3	5/19	Removed MAX5992C from data sheet	1–24

