Document Number: SC900844
Rev. 2.0, 5/2011

RoHS

Integrated Power Management IC for Ultra-mobile and Embedded Applications

900844

POWER MANAGEMENT

98ASA10841D
11 mm x 11 mm
338-MAPBGA

The 900844 is a high efficiency Power Management Integrated Circuit (PMIC) capable of providing operating voltages for Ultra-mobile platforms for Netbook, Tablets, and embedded devices through its 20 voltage rails. It has 5 switching power supplies running at frequencies from 1.0 to 4.0 MHz,14 highly efficient LDOs, and one 3.3 V power switch. It incorporates a 10-bit ADC, Real Time Clock, 8 GPIOs and 8 GPOs.

The 900844 is fully configurable and controllable through its SPI interface. It provides an optimized power management solution for ultra-mobile platforms used on netbooks, tablets, and slates.

Optimum partitioning, high feature integration, and state-of-the-art technology, allow Freescale to effectively serve this growing market segment.

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
SC900844JVK	-40 °C to 85 °C	338-MAPBGA

Features

- Main system power management integrated in a single chip
- Fully programmable DC/DC switching, low drop-out regulators, and load switches
- SPI interface (up to 25 MHz operation)
- 10-bit ADC for internal and external sensing with touch screen interface
- Real time clock (RTC)
- 8 Interrupt capable GPIOs and 8 GPOs
- I/O interrupt and reset controller

Applications

- Netbooks
- Tablet PC
- Slates
- Embedded Devices

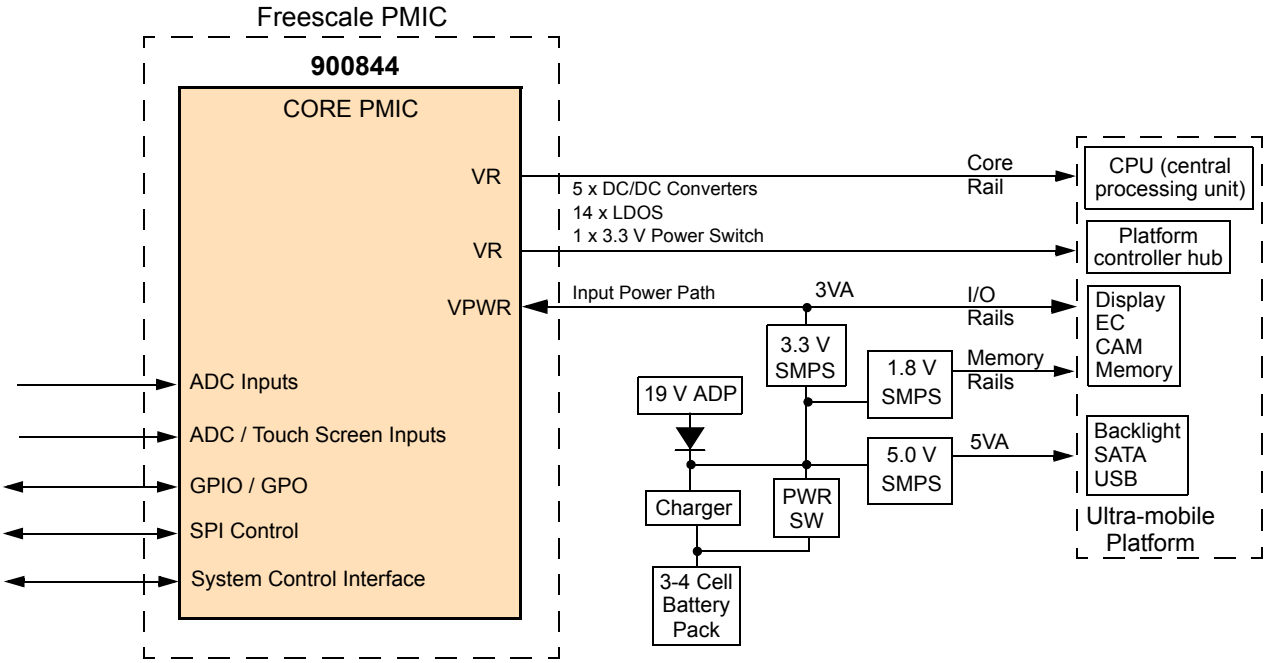


Figure 1. 900844 Simplified Application Diagram

freescale semiconductor

INTERNAL BLOCK DIAGRAM

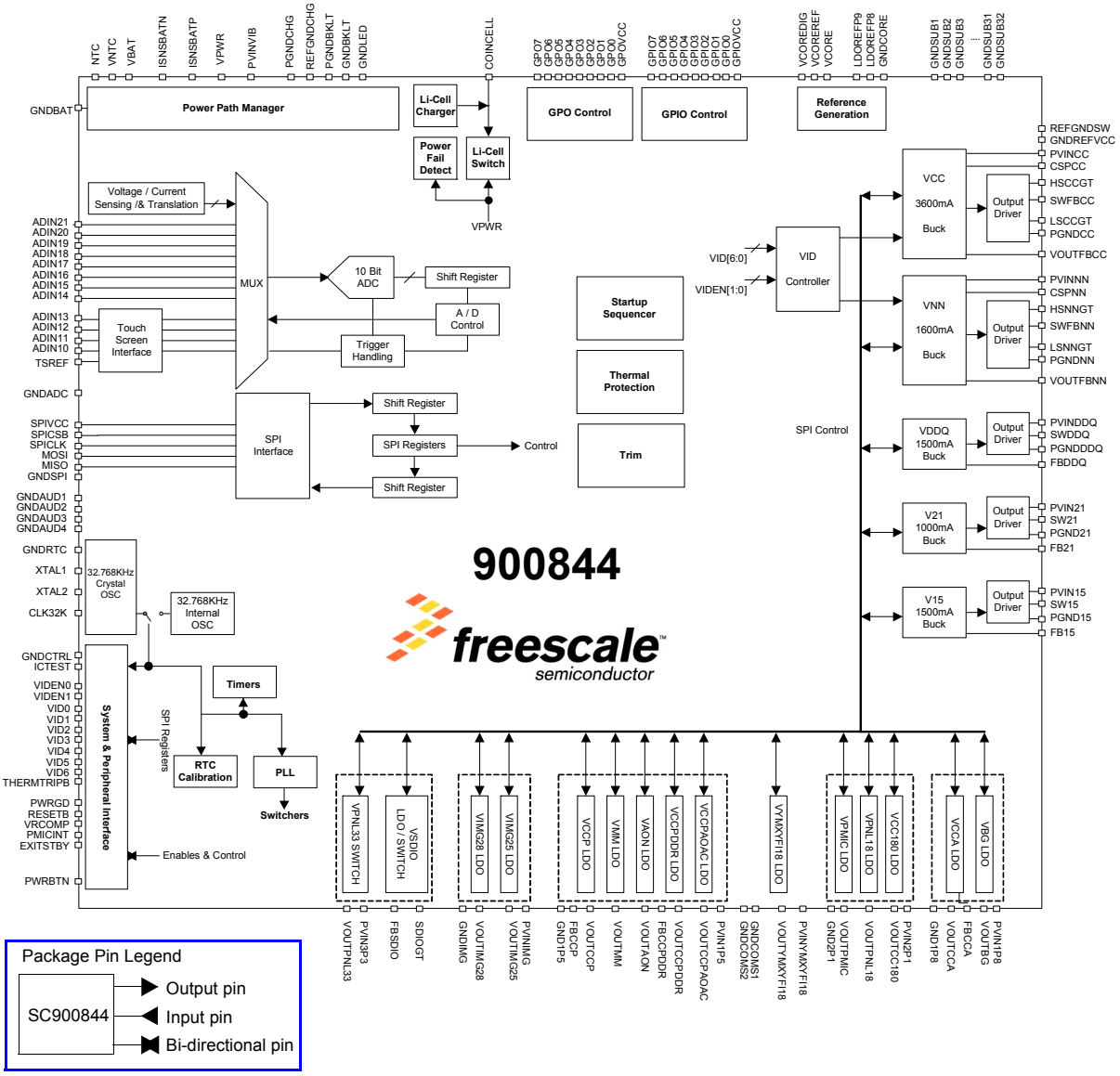


Figure 2. 900844 Internal Block Diagram

PIN OUT DESCRIPTION AND BALL MAP

Refer to Pin Description for a detailed list of pins and ball assignments. The ball map of the package is given in Figure 3 as a top view. The BGA footprint on the application PCB will have the same mapping as given in Figure 3.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	NC1		NC1		PVIN1P5		FBCCP		NC		PVIN2P1		VOUTPNL18		SPICLK		NC		GNDLSPR		GNDLSPL		NC		NC		NC2		NC2
B		NC1		VOUTCCPAOAC		LDOREFP8		CS		VOUTPMIC		VOUTCC180		VCORE		PMICINT		VINLSPR		NC		NC		NC		NC		NC2	
C	NC1		VOUTCCA		PVIN1P5		VOUTAON		VOUTCCP		PVIN2P1		VCOREREF		RESETB		NC		VYMXPAEN		VINLSPL		NC						NC2
D		VOUTBG		VIDEN0		PVIN1P8								SPICSB				NC		NC								NC	
E	VID2		VID0		VIDEN1		FBCCA																		NC		GNDCP		NC
F		VID6		VID4																								NC	
G	CSPCC		SWFBCC				FBCCPDDR		VOUTCCPDDR		PWRBTN		LDOREFP9		MOSI		THERMTRIPB		NC		GNDAUD4		GNDAUD1				NC		GNDAUDXTAL
H		LSCCGT		LSCCGT				VID1		GND1P5		SCK		GNDCORE		VRCOMP		GNDSUB		NC		GNDSUB				NC		RX2	
J	PGNDCC		PGNDCC				VID5		VID3		VOUTMM		VCOREDIG		MISO		EXITSTBY		GNDSUB		GNDSUB		GNDSUB				FS2		BCL2
K		HSCCGT		HSCCGT				VOUTFBCC														NC				NC		BCL1	
L	HSNNGT		PVINNN		PVINCC		PVINCC		PGNDNN		GNDREFVCC		GNDSPI		SPIVCC		GNDSUB		GNDSUB		GNDAUD2		RX1		I2SVCC		FS1		NC
M		LSNNGT		VOUTFBNN		PGNDDDQ		PGNDDDQ				GND2P1		GNDSUB		PWRGD		GNDSUB				NC						GNDSP	
N	SWDDQ		SWDDQ		PGNDDDQ		PGNDDDQ		SWFBNN		CSPNN		GND1P8		GNDSUB		GNDSUB		GNDSUB		NC		NC				NC		NC
P		SWDDQ		SWDDQ		PVINDDQ		PVINDDQ				GNDSUB		GNDSUB		GNDSUB		GNDSUB				NC				NC		NC	
R	PGNDYMX3G		PGNDYMX3G		PVINDDQ		PVINDDQ		FBDDQ		GNDSUB		GNDSUB		GNDSUB		GNDSUB		GNDAUD3		NC		ICTEST				NC		GNDLED
T		NC		NC		NC		NC				GNDSUB		GNDSUB		GNDSUB		GNDSUB				GNDSUB			NC		NC		
U	PGND21		PGND21		PGND21		REFGNDSW		NC		GNDSUB		GNDSUB		GNDSUB		GNDSUB		GNDSUB		NC		NC		NC		NC		NC
V		SW21		SW21		SW21		FB21				GNDSUB		GNDIMG		GNDADC		GNDSUB				NC		NC		PGNDOTG		PGNDOTG	
W	PVIN21		PVIN21		PVIN21		FB15				GNDCOMS2		NC		ADIN20		TSREF		NC		NC		NC		NC		NC		NC
Y		PGND15		PGND15		PGND15		GPO4														NC				PGNDBKLT		PGNDBKLT	
AA	SW15		SW15		SW15		GNDCOMS1		NC		GPIO3		NC		NC		ADIN13		NC		GNDBAT		NC		NC		NC		NC
AB		PVIN15		PVIN15		PVIN15		GPO7		GPIO1		SDIOGT		GNDCTRL		ADIN11		GPIO6		NC		NC				VPWR		GNDBKLT	
AC	NC		NC				GPO1		NC		GPIOVCC		FBSDIO		ADIN21		ADIN15		GPIO4		REFGNDCHG		NTC		CHGBYPGT		VBAT		COINCELL
AD		PVINYMXYFI18		GPO2								PGNDYMXPA										NC				ISNSBATP		NC	
AE	VOUTYMXYFI18		NC		GPOVCC						NC						ADIN14				NC		NC		NC		CHGGT		VNTC
AF		NC		GPO0		NC						PGNDYMXPA						XTAL2		GPIO5		NC		NC		PGNDCHG		ISNSBATN	
AG	NC3		GPO3		GPO6		GPIO0		VOUTPNL33		NC		PVINVIB		VOUTIMG28		ADIN16		XTAL1		GPIO7		RAWCHG		NC		NC		NC4
AH		NC3		GPO5		NC		NC		NC		PGNDYMXPA		VOUTIMG25		ADIN19		ADIN17		ADIN10		CLK32K		NC		PGNDCHG		NC4	
AJ	NC3		NC3		NC		GPIO2		PVIN3P3		NC		NC		PVINIMG		ADIN18		ADIN12		GNDRTC		NC		NC		NC4		NC4

Figure 3. 900844 Package Ball Map

PIN DESCRIPTION

The Type Column indicates the maximum average current through each ball assigned to the different nodes, 500 mA maximum for HIPWR, 300 mA maximum for MDPWR, and 100 mA maximum for LOPWR

Table 1. 900844 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
VCC - (0.65 V-1.2 V) / 3.5 A VID CPU BUCK with External FETs						
PVINCC	HIPWR	-	4.8 V	2	L5, L7	Gate drivers power supply input
HSCCGT	HIPWR	-	4.8 V	2	K2, K4	High side FET gate drive
LSCCGT	HIPWR	-	4.8 V	2	H2, H4	Low side FET gate drive
PGNDCC	HIPWRGND	-	-	2	J1, J3	Local ground for internal circuitry
VOUTFBCC	SGNL	I	4.8 V	1	K8	Output voltage sensing input and negative current sense terminal
SWFBCC	SGNL	I	3.6 V	1	G3	Switch node feedback
CSPCC	SGNL	I	3.6 V	1	G1	Positive current sense terminal
VNN - (0.65 V-1.2 V) / 1.6 A VID CPU BUCK with External FETs						
PVINNN	HIPWR	-	4.8 V	1	L3	Gate drivers power supply input
HSNNGT	HIPWR	-	4.8 V	1	L1	High side FET gate drive
LSNNGT	HIPWR	-	4.8 V	1	M2	Low side FET gate drive
PGNDNN	HIPWRGND	-	-	1	L9	Local ground for internal circuitry
VOUTFBNN	SGNL	I	4.8 V	1	M4	Output voltage sensing input and negative current sense terminal
SWFBNN	SGNL	I	3.6 V	1	N9	Switch node feedback
CSPNN	SGNL	I	3.6 V	1	N11	Positive current sense terminal
VDDQ - 1.8 V / 1.3 A BUCK						
PVINDDQ	HIPWR	-	4.8 V	4	P6, P8, R5, R7	Power supply input
SWDDQ	HIPWR	-	4.8 V	4	N1, N3, P2, P4	Switch node
PGNDDDQ	HIPWRGND	-	-	4	M6, M8, N5, N7	Power ground
FBDDQ	SGNL	I	3.6 V	1	R9	Output voltage feedback input
V21 - 2.1 V / 1.0 A BUCK						
PVIN21	HIPWR	-	4.8 V	3	W1, W3, W5	Power supply input
SW21	HIPWR	-	4.8 V	3	V2, V4, V6	Switch node
PGND21	HIPWRGND	-	-	3	U1, U3, U5	Power ground
FB21	SGNL	I	3.6 V	1	V8	Output voltage feedback input
V15 - 1.5 V (or 1.6 V) / 1.5 A BUCK						
PVIN15	HIPWR	-	4.8 V	3	AB2, AB4, AB6	Power supply input
SW15	HIPWR	-	4.8 V	3	AA1, AA3, AA5	Switch node
PGND15	HIPWRGND	-	-	3	Y2, Y4, Y6	Power ground
FB15	SGNL	I	3.6 V	1	W7	Output voltage feedback input

Table 1. 900844 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
VBG - 1.25 V/2 mA LDO VCCA - 1.5 V/150 mA LDO						
PVIN1P8	LOPWR	-	3.6 V	1	D6	Power supply input, shared by VBG and VCCA
GND1P8	GND	-	-	1	N13	Ground reference
VOUTBG	LOPWR	-	2.5 V	1	D2	VBG output voltage node
VOUTCCA	LOPWR	-	2.5 V	1	C3	VCCA output voltage node
FBCCA	SGNL	I	2.5 V	1	E7	VCCA output voltage feedback input
VCC180- 1.8 V/390 mA LDO VPNL18- 1.8 V/225 mA LDO VPMIC - 1.8 V/50 mA LDO						
PVIN2P1	HIPWR	-	3.6 V	2	A11, C11	Power supply input, shared by VCC180, VPNL18, and VPMIC
GND2P1	GND	-	-	1	M12	Ground reference
VOUTCC180	HIPWR	-	2.5 V	1	B12	VCC180 output voltage node
VOUTPNL18	MDPWR	-	2.5 V	1	A13	VPNL18 output voltage node
VOUTPMIC	LOPWR	-	2.5 V	1	B10	VPMIC output voltage node
VYMXYFI18 - (YMX:1.8 V/200 mA - YFI:1.8 V/200 mA) LDO						
PVINYMXYFI18	MDPWR	-	4.8 V	1	AD2	Power supply input for VYMXYFI18
VOUTYMXYFI18	MDPWR	-	3.6 V	1	AE1	VYMXYFI18 output voltage node
GNDCOMS1	GND	-	-	1	AA7	Ground reference
GNDCOMS2	GND	-	-	1	W11	Ground reference
VCCPAOAC- 1.05 V/155 mA LDO VCCPDDR - 1.05 V/60 mA LDO VAON - 1.2 V/250 mA LDO VMM- 1.2 V/5 mA LDO VCCP - 1.05 V/445 mA LDO						
PVIN1P5	HIPWR	-	3.6 V	2	A5, C5	Power supply input, shared by VCCPAOAC, VCCPDDR, VAON, VMM, and VCCP
GND1P5	GND	-	-	1	H10	Ground reference
VOUTCCPAOAC	LOPWR	-	2.5 V	1	B4	VCCPAOAC output voltage node
VOUTCCPDDR	LOPWR	-	2.5 V	1	G9	VCCPDDR output voltage node
FBCCPDDR	SGNL	I	2.5 V	1	G7	VCCPDDR output voltage feedback input
VOUTAON	MDPWR	-	2.5 V	1	C7	VAON output voltage node
VOUTMM	LOPWR	-	2.5 V	1	J11	VMM output voltage node
VOUTCCP	HIPWR	-	2.5 V	1	C9	VCCP output voltage node
FBCCP	SGNL	I	2.5 V	1	A7	VCCP output voltage feedback input
VIMG25- 2.5 V/80 mA LDO VIMG28- 2.8 V/225 mA LDO						
PVINIMG	MDPWR	-	4.8 V	1	AJ15	Power supply input, shared by VIMG25 and VIMG28
GNDIMG	GND	-	-	1	V14	Ground reference
VOUTIMG25	LOPWR	-	3.6 V	1	AH14	VIMG25 output voltage node

Table 1. 900844 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
VOUTIMG28	MDPWR	-	3.6 V	1	AG15	VIMG28 output voltage node
VPNL33 - 3.3 V/100 mA Switch						
PVIN3P3	MDPWR	-	3.6 V	1	AJ9	Power supply input, shared by VPNL33 and VSDIO
VOUTPNL33	LOPWR	-	3.6 V	1	AG9	VPNL33 output voltage node
VSDIO - 3.3 V/215 mA Switch OR 1.8 V/215 mA LDO						
SDIOGT	LOPWR	-	3.6 V	1	AB12	Gate driver output for VSDIO pass FET
FBSDIO	SGNL	-	3.6 V	1	AC13	Feedback node when VSDIO is in Switch mode; Output voltage node when VSDIO is in LDO mode.
Internal Supplies						
VCORE	LOPWR	-	3.6 V	1	B14	Internal supply output voltage node
VCOREDIG	LOPWR	-	1.5 V	1	J13	Internal supply output voltage node
VCOREREF	LOPWR	-	3.6 V	1	C13	Internal band gap supply output voltage node
LDOREFP8	LOPWR	-	3.6 V	1	B6	Internal divided down band gap supply output voltage node dedicated for LDOs
LDOREFP9	LOPWR	-	3.6 V	1	G13	Internal divided down band gap supply output voltage node dedicated for LDOs
GNDCORE	LOPWRGND	-	-	1	H14	Ground for internal supplies
Input Power Path						
VPWR	MDPWR	-	4.8 V	1	AB26	Input power node for PMIC
VBAT	LOPWR	-	4.8 V	1	AC27	Battery voltage sensing input
GNDBAT	LOPWRGND	-	-	1	AA21	Input supply ground
VNTC	LOPWR	-	3.6 V	1	AE29	Bias voltage for NTC resistor stack
NTC	SGNL	I	3.6 V	1	AC23	NTC connection node
ISNSBATP	SGNL	I	4.8 V	1	AD26	Connect to VBAT
ISNSBATN	SGNL	I	4.8 V	1	AF28	Connect to VBAT
PVINVIB	MDPWR	-	4.8 V	1	AG13	Always connect to VPWR
Coin Cell Charger						
COINCELL	LOPWR	-	3.6 V	1	AC29	Coin cell supply input, coin cell charger output
ADC + TS I/F						
ADIN10	SGNL	I	4.8 V	1	AH20	ADC generic input 1, used as touchscreen input X1, TSX1
ADIN11	SGNL	I	4.8 V	1	AB16	ADC generic input 2, used as touchscreen input X2, TSX2
ADIN12	SGNL	I	4.8 V	1	AJ19	ADC generic input 3, used as touchscreen input Y1, TSY1
ADIN13	SGNL	I	4.8 V	1	AA17	ADC generic input 4, used as touchscreen input Y2, TSY2
ADIN14	SGNL	I	4.8 V	1	AE17	ADC generic input 5
ADIN15	SGNL	I	4.8 V	1	AC17	ADC generic input 6
ADIN16	SGNL	I	4.8 V	1	AG17	ADC generic input 7
ADIN17	SGNL	I	4.8 V	1	AH18	ADC generic input 8

Table 1. 900844 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
ADIN18	SGNL	I	4.8 V	1	AJ17	ADC generic input 9
ADIN19	SGNL	I	4.8 V	1	AH16	ADC generic input 10
ADIN20	SGNL	I	4.8 V	1	W15	ADC generic input 11
ADIN21	SGNL	I	4.8 V	1	AC15	ADC generic input 12
TSREF	LOPWR	-	3.6 V	1	W17	Reference for touchscreen interface
GNDADC	LOPWRGND	-	-	1	V16	Ground reference for ADC
Oscillator and Real Time Clock - RTC						
XTAL1	SGNL	I	2.5 V	1	AG19	32.768 kHz oscillator crystal connection 1
XTAL2	SGNL	O	2.5 V	1	AF18	32.768 kHz oscillator crystal connection 2
CLK32K	SGNL	O	3.6 V	1	AH22	32 kHz clock output
GNDRTC	GND	-	-	1	AJ21	Ground for the RTC block
Platform Architecture Sideband Signals						
PMICINT	SGNL	O	2.5 V	1	B16	PMIC Interrupt. Asserted by PMIC to wake platform controller hub and begin communications. Level-sensitive, read to clear.
VRCOMP	SGNL	O	2.5 V	1	H16	Voltage regulator complete. Asserted high by the PMIC when a SPI voltage regulation request has been decoded. The signal is de-asserted on completion of the request (i.e. the rail is in regulation).
RESETB	SGNL	O	2.5 V	1	C15	Active low hard reset for platform controller hub. When asserted, the platform controller hub should return to its initial default state.
PWRGD	SGNL	O	2.5 V	1	M16	POWER GOOD: The 900844 asserts this signal to indicate that all power rails to the platform controller hub are good. Assertion of PWRGD also means that VCCA_OSC has been valid for at least 30 microseconds. The Platform Controller Hub will remain “off” until this signal is asserted.
EXITSTBY	SGNL	I	2.5 V	1	J17	EXIT Standby. When asserted, the 900844 exits the AOAC standby settings for regulating the platform supplies. When asserted, the 900844 switches VRs on which are defined in registers 0x09 through 0x0D. This is a low latency VR context switch.
THERMTRIPB	SGNL	I	1.5 V	1	G17	Thermal trip. Asserted by the CPU to indicate a catastrophic thermal event.
VIDEN0	SGNL	I	1.5 V	1	D4	Driven by the CPU to indicate which VR the VID bus is addressed to (VCC or VNN). Debounced inside the 900844 for 150 ns. The CPU will hold the value for at least 300 ns.
VIDEN1	SGNL	I	1.5 V	1	E5	
VID0	SGNL	I	1.5 V	1	E3	Driven by the CPU to indicate the output voltage setting for the VCC and VNN rails. Debounced inside the 900844 for 150 ns. The CPU will hold the value for at least 300 ns.
VID1	SGNL	I	1.5 V	1	H8	
VID2	SGNL	I	1.5 V	1	E1	
VID3	SGNL	I	1.5 V	1	J9	
VID4	SGNL	I	1.5 V	1	F4	
VID5	SGNL	I	1.5 V	1	J7	
VID6	SGNL	I	1.5 V	1	F2	
GNDCTRL	GND	-	-	1	AB14	Logic Control Ground

Table 1. 900844 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
SPI Interface						
SPIVCC	LOPWR	-	3.6 V	1	L15	Supply for SPI Bus
SPICLK	SGNL	I	3.6 V	1	A15	SPI Clock Input
MOSI	SGNL	I	3.6 V	1	G15	SPI write input
MISO	SGNL	O	3.6 V	1	J15	SPI read output
SPICSB	SGNL	I	3.6 V	1	D14	SPI chip select input
GNDSPI	GND	-	-	1	L13	Ground for SPI interface
GPIOs & GPOs & Power Button						
GPIOVCC	LOPWR	-	3.6 V	1	AC11	GPIO power
GPIO0	SGNL	I/O	3.6 V	1	AG7	Fully configurable GPIO inputs/outputs for general purpose sensing and platform control
GPIO1	SGNL	I/O	3.6 V	1	AB10	
GPIO2	SGNL	I/O	3.6 V	1	AJ7	
GPIO3	SGNL	I/O	3.6 V	1	AA11	
GPIO4	SGNL	I/O	3.6 V	1	AC19	
GPIO5	SGNL	I/O	3.6 V	1	AF20	
GPIO6	SGNL	I/O	3.6 V	1	AB18	
GPIO7	SGNL	I/O	3.6 V	1	AG21	
GPOVCC	LOPWR	-	3.6 V	1	AE5	GPO power
GPO0	SGNL	O	3.6 V	1	AF4	General purpose outputs
GPO1	SGNL	O	3.6 V	1	AC7	
GPO2	SGNL	O	3.6 V	1	AD4	
GPO3	SGNL	O	3.6 V	1	AG3	
GPO4	SGNL	O	3.6 V	1	Y8	
GPO5	SGNL	O	3.6 V	1	AH4	
GPO6	SGNL	O	3.6 V	1	AG5	
GPO7	SGNL	O	3.6 V	1	AB8	
PWRBTN	SGNL	I	1.5 V	1	G11	PMIC hardware on/off button
Test Pins						
ICTEST	SGNL	I	7.5 V	1	R23	Always connect to GND
Reference Supplies						
VINLSPR	MDPWR	-	5.5V	1	B18	Always connect to VPWR
VINLSPL	MDPWR	-	5.5V	1	C21	Always connect to VPWR
I2SVCC	LOPWR	-	3.6 V	1	L25	Always connect to VPMIC

Table 1. 900844 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
Ground References						
PGNDCHG	HIPWRGND	-	-	2	AF26, AH26	Power GND
BCL1	SGNL	I/O	3.6 V	1	K28	Always connect to GND
FS1	SGNL	I/O	3.6 V	1	L27	Always connect to GND
RX1	SGNL	I	3.6 V	1	L23	Always connect to GND
BCL2	SGNL	I/O	3.6 V	1	J29	Always connect to GND
FS2	SGNL	I/O	3.6 V	1	J27	Always connect to GND
RX2	SGNL	I	3.6 V	1	H28	Always connect to GND
SCK	SGNL	I	3.6 V	1	H12	Always connect to GND
GNDSP	LOPWRGND	-	-	1	M28	Analog GND
GNDLSPR	MDPWRGND	-	-	1	A19	Analog GND
GNDLSPL	MDPWRGND	-	-	1	A21	Analog GND
GNDCP	LOPWRGND	-	-	1	E27	Analog GND
PGNDYMXPA	HIPWRGND	-	-	3	AD12, AF12, AH12	Power GND
PGNDYMX3G	HIPWRGND	-	-	2	R1, R3	Power GND
PGNDOTG	HIPWRGND	-	-	2	V26, V28	Power GND
PGNDBKLT	HIPWRGND	-	-	2	Y26, Y28	Power GND
GNDAUDXTAL	GND	-	-	1	G29	Analog GND
GNDAUD1	GND	-	-	1	G23	Analog GND
GNDAUD2	GND	-	-	1	L21	Analog GND
GNDAUD3	GND	-	-	1	R19	Analog GND
GNDAUD4	GND	-	-	1	G21	Analog GND
GNDBKLT	GND	-	-	1	AB28	Analog GND
GNDLED	GND	-	-	1	R29	Analog GND
REFGNDCHG	GND	-	-	1	AC21	Dedicated reference ground for the input power path
REFGNDSW	GND	-	-	1	U7	Dedicated reference ground for the switching regulators
GNDREFVCC	GND	-	-	1	L11	Dedicated reference ground for VCC regulator
GNDSUB	GND	-	-	32	H18, H22, J19, J21, J23, L17, L19, M14, M18, N15, N17, N19, P12, P14, P16, P18, R11, R13, R15, R17, T12, T14, T16, T18, T22, U11, U13, U15, U17, U19, V12, V18	Substrate GND

Table 1. 900844 Pin Description

Node Name	Type	I/O	Rating	# of Balls	BGA Location	Pin Description
Reserved						
RAWCHG	MDPWR	-	20 V	1	AG23	Reserved - Do not connect
CHGBYPGT	MDPWR	-	4.8 V	1	AC25	Reserved - Do not connect
CHGGT	MDPWR	-	4.8 V	1	AE27	Reserved - Do not connect
VYMXPAEN	SGNL	I	2.5 V	1	C19	Reserved - Do not connect
CS	SGNL	I	3.6 V	1	B8	Reserved - Do not connect

Notes

1. The Type Column indicates the maximum average current through each ball assigned to the different nodes. 500 mA maximum for HIPWR, 300 mA maximum for MDPWR, and 100 mA maximum for LOPWR

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Input Voltage	-	-0.3 to +4.4	V
Coin Cell Voltage	-	-0.3 to +3.6	V
ESD Rating, All Pins, Human Body Model (HBM)(4)	V_{ESDHBM}	±2000	V
ESD Rating, All Pins, Charge Device Model (CDM) (4), (5)	V_{ESDCDM}	±450	V
THERMAL RATINGS			
Ambient Operating Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-30 to +125	°C
Storage Temperature Range	T_{ST}	-65 to +150	°C
Peak Package Reflow Temperature (2), (3)	T_{PPRT}	260	°C
POWER RATINGS			
Hard Mechanical Off There is no Valid VBAT voltage connected to the 900844, BATDET = 0		0	mW
Soft Mechanical Off The 900844 has input power from 3.3 V Supply into VBAT. All VRs are programmed “OFF”, BATDET = 1		5.0	mW
Power On The 900844 has input power from 3.3 V supply into VBAT. The cold-boot rails are “ON”. V21 = 2.1 V, V15 = 1.5 V, VAON = 1.2 V, VCCPAOAC = 1.05 V, VPMIC = 1.8 V, All VR outputs are set in PFM or APS mode driving purely capacitive loads. BATDET = 1		100	mW

Notes

2. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
3. Freescale's Package Reflow capability meets the Pb-free requirements for JEDEC standard J-STD-020C, for Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL)
4. ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).
5. All pins meet 500 V CDM except VCOREREF.

POWER DISSIPATION

During operation, the temperature of the die must not exceed the maximum junction temperature. Depending on the operating ambient temperature and the total internal dissipation this limit can be exceeded.

To optimize the thermal management scheme and avoid overheating, the 900844 provides a thermal management system that protects against overheating. This protection should be considered as a fail-safe mechanism, and the application design should initiate thermal shutdown under normal conditions. Reference Thermal Management for more details.

POWER CONSUMPTION

Table 2 defines the maximum power consumption specifications in the various system and device states. For each entry in the table, the component is assumed to be configured for driving purely capacitive loads, and the voltages listed in each entry are nominal output voltages.

Note that the “Soft Mechanical Off” state is a transitional state. The device will spend less than 150 µs in this state before V15 starts to turn on, upon detection of a valid input voltage.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM CONTROL INTERFACE					
Input Low Voltage EXITSTBY, VID[6:0] THRMTRIPB, VIDEN[1:0]	V_{IL}	 0 0	 - -	 $0.3*V_{CCP}$ $0.3*V_{CCPA OAC}$	V
Input High Voltage EXITSTBY, VID[6:0] THRMTRIPB, VIDEN[1:0]	V_{IH}	 $0.7*V_{CCP}$ $0.7*V_{CCPA OAC}$	 - -	 V_{CCP} $V_{CCPAOAC}$	V
Output Low Voltage PMICINT, VRCOMP, RESETB, PWRGD.	V_{OL}	 0	 -	 0.1	V
Output High Voltage PMICINT, VRCOMP, RESETB, PWRGD.	V_{OH}	 V_{PMIC} - 0.1	 -	 V_{PMIC}	V
SPI INTERFACE LOGIC IO					
Operating Voltage Range (SPIVCC Pin)	V_{SPIVCC}	1.74	1.8	3.1	V
Input High SPICSB, MOSI, SPICLK	-	0.7* V_{SPIVCC}	-	V_{SPIVCC} +0.3	V
Input Low SPICSB, MOSI, SPICLK	-	0	-	0.3* V_{SPIVCC}	V
Output Low MISO (Output sink 100 µA)	-	0	-	0.1	V
Output High MISO (Output source 100 µA)	-	V_{SPIVCC} -0.1	-	V_{SPIVCC}	V
OSCILLATOR AND CLOCK OUTPUTS MAIN CHARACTERISTICS					
Operating Voltage	-	1.2	-	1.5	V
RTC OSC Consumption Current (RTC Mode: All blocks disabled, no main battery attached, coin cell is attached to COINCELL)	-	-	1.0	2.0	µA
Output Low CLK32K (Output sink 100 µA)	-	0	-	0.1	V
Output High CLK32K (Output source 100 µA)	-	V_{SPIVCC} - 0.1	-	V_{SPIVCC}	V
CLK32K Output Duty Cycle	-	40	50	60	%
RTC					
Input Voltage Range	-	1.2	-	1.5	V
Consumption Current	-	-	15	25	µA
Crystal OSC Frequency Tolerance	-	-30	-	+30	ppm
Crystal OSC Peak Temperature Frequency (Turn Over Temperature)	-	20	25	30	°C
Crystal OSC Maximum Series Resistance	-	-	80	-	KΩ
Crystal OSC Maximum Drive Level	-	-	0.5	-	µW

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal OSC Operating Drive Level	-	0.25	-	0.5	µW
Crystal OSC Nominal Lead Capacitance	-	-	9.0	-	pF
Crystal OSC Aging	-	-	-	3.0	ppm/year
COIN CELL CHARGER					
Coin cell Charge Voltage (Selectable through VCOIN[2:0] bits)	$V_{COINCELL}$	2.5	-	3.3	V
Coin cell Charge Voltage Accuracy	-	-100	-	100	mV
Coin cell Charge Current	I_{COIN}	-	60	-	µA
Coin cell Charge Current Accuracy	-	-15	-	15	%
POWER STATES DETECTION THRESHOLDS					
Battery Cutoff Threshold (Depending on Battery Model)	V_{BATOFF}	2.2	-	2.4	V
Coin Cell Disconnect Threshold	$V_{COINOFF}$	1.8	-	2.0	V
Low Battery Threshold	V_{LOWBAT}	3.2	-	-	V
Valid Battery Threshold	V_{TRKL}	-	3.0	-	V
VPWR Rising Under-voltage Threshold	V_{PWRUVR}	-	3.1	-	V
VPWR Falling Under-voltage Threshold	V_{PWRUVF}	-	2.55	-	V
VCC ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Programmability Range Low Power Mode Active Mode	V_{CC}	 0.3 0.65	 - -	 0.7 1.2	V
Output Voltage Programmability Step Size	-	-	12.5	-	mV
Output Voltage Accuracy 0.6 V < V_{CC} < 12 V, 1.5 A < I_{CC} < 3.5 A 0.6 V < V_{CC} < 12 V, I_{CC} < 1.5 A 0.3 V < V_{CC} < 0.6 V	-	 -5.0 -4.0 -7.0	 - - -	 5.0 4.0 7.0	%
Output Voltage Overshoot Maximum overshoot voltage above VID setting voltage. Maximum overshoot time is 10-30 s, output voltage = 0.9 V at 50 mA	V_{OS}	-	-	50	mV
Continuous Output Load Current Low Power mode Active Mode	I_{CC}	 - 0.2	 - -	 0.2 3.5	A
Peak Current Limit	I_{LIMCC}	-	5.0	-	A
Output Current Limit Accuracy	-		±15	-	%
Transient Load Change Low Power Mode Active Mode	ΔI_{CC}	 - -	 - -	 0.2 1.2	A

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VNN ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Programmability Range (Set by VID Control Signals)	V_{NN}	0.65	-	1.2	V
Output Voltage Programmability Step Size	-	-	12.5	-	mV
Output Voltage Accuracy	-	-5.0	-	5.0	%
Output Voltage Overshoot Maximum overshoot voltage above VID setting voltage. Maximum overshoot time is 10 s, output voltage = 0.9 V at 50 mA	V_{OS}	-	-	50	mV
Continuous Output Load Current Low Power Mode Active Mode	I_{NN}	 - 0.2	 - -	 0.2 1.6	A
Peak Current Limit	I_{LIMNN}	-	2.5	-	A
Output Current Limit Accuracy	-	-	±20	-	%
Transient Load Change	ΔI_{NN}	-	-	0.5	A
VDDQ ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Setting	V_{DDQ}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Continuous Output Load Current	I_{DDQ}	-	-	1.3	A
Peak Current Limit	I_{LIMDDQ}	-	1.78	-	A
Output Current Limit Accuracy 0.5 A < I_{DDQ} < 1.3 A I_{DDQ} < 0.5 A	-	 -15 -20	 - -	 +15 +20	%
Transient Load Change	I_{DDQ}	-	-	0.5	A
Effective Quiescent Current Consumption (PWM, No Load)	I_{QDDQ}	-	30	-	µA
V21 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Setting	V_{21}	-	2.1	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Continuous Output Load Current	I_{21}	-	-	1.0	A
Peak Current Limit	I_{LIM21}	-	1.42	-	A
Output Current Limit Accuracy	-	-20	-	+20	%
Transient Load Change	I_{21}	-	-	0.5	A
Effective Quiescent Current Consumption (PWM, No Load)	I_{Q21}	-	30	-	µA

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
V15 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Extended Input Voltage Range	V_{PWR}	2.8	3.6	4.7	V
Output Voltage Setting (Also programmable to 1.6 V, typical)	V_{15}	-	1.5	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Continuous Output Load Current	I_{15}	0	0.75	1.5	A
Peak Current Limit	I_{LIM15}	-	1.6	-	A
Output Current Limit Accuracy	-	-20	-	+20	%
Transient Load Change	I_{15}	-	-	0.5	A
Effective Quiescent Current Consumption (PWM, No Load)	I_{Q15}	-	30	-	µA
VBG ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{DDQ} V_{21}	1.71 1.995	1.80 2.100	1.89 2.205	V
Output Voltage Setting	V_{BG}	-	1.25	-	V
Output Voltage Accuracy	-	-2.0	-	2.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{BGUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{BGUVH}	-	1.0	-	%
Continuous Output Load Current Active Mode Low Power Mode	I_{BG}	 - -	 - -	 2.0 40	 mA µA
Current Limit	I_{LIMBG}	-	94	-	mA
Transient Load Change	ΔI_{BG}	-	-	1.0	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{BG} = 1.5 mA, V_{DDQ} = 1.8 V)	$PSRR_{BG}$	50	60	-	dB
Effective Quiescent Current Consumption Active Mode Low Power Mode	I_{QBG}	 - -	 - -	 18 10	µA
VCCA ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{DDQ} V_{21}	1.71 1.995	1.80 2.100	1.89 2.205	V
Output Voltage Setting	V_{CCA}	-	1.5	-	V
Output Voltage Accuracy	-	-2.0	-	2.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{CCAUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{CCAUVH}	-	1.0	-	%
Continuous Output Load Current Active Mode Low Power Mode	I_{CCA}	 - -	 - -	 150 3.0	 mA mA

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Current Limit	I_{LIMCCA}	-	225	-	mA
Transient Load Change	ΔI_{CCA}	-	-	50	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CCA} = 112.5 mA, V_{DDQ} = 1.8 V)	$PSRR_{CCA}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QCCA}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VCC180 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{21}	1.995	2.1	2.205	V
Output Voltage Setting	V_{CC180}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{CC180UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{CC180UVH}$	-	1.0	-	%
Continuous Output Load Current	I_{CC180}				
Active Mode		-	-	390	mA
Low Power Mode		-	-	7.8	mA
Current Limit	$I_{LIMCC180}$	-	585	-	mA
Transient Load Change	ΔI_{CC180}	-	-	350	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CC180} = 292.5 mA, V_{21} = 2.1 V)	$PSRR_{CC180}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QCC180}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VPNL18 ELECTRICAL CHARACTERISTICS SPECIFICATION					
Input Voltage Range	V_{21}	1.995	2.1	2.205	V
Output Voltage Setting	V_{PNL18}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{PNL18UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{PNL18UVH}$	-	1.0	-	%
Continuous Output Load Current					mA
Active Mode	I_{PNL18}	-	-	210	
Low Power Mode		-	-	4.2	
Current Limit	$I_{LIMPNL18}$	-	315	-	mA
Transient Load Change	ΔI_{PNL18}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{PNL18} = 157.5 mA, V_{21} = 2.1 V)	$PSRR_{PNL18}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QPNL18}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VPMIC ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{21}	1.995	2.1	2.205	V
Output Voltage Setting	V_{PMIC}	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{PMICUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{PMICUVH}$	-	1.0	-	%
Continuous Output Load Current Active Mode Low Power Mode	I_{PMIC}	 - -	 - -	 100 2.0	mA
Current Limit	$I_{LIMPMIC}$	-	150	-	mA
Transient Load Change	ΔI_{PMIC}	-	-	20	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{PMIC} = 75 mA, V_{21} = 2.1 V)	$PSRR_{PMIC}$	50	60	-	dB
Effective Quiescent Current Consumption Active Mode Low Power Mode	I_{QPMIC}	 - -	 - -	 18 10	µA
VYMXYFI18 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{21}	1.995	2.1	2.205	V
Output Voltage Setting	$V_{YMXYFI18}$	-	1.8	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{YMXYFI18UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{YMXYFI18UVH}$	-	1.0	-	%
Continuous Output Load Current Active Mode Low Power Mode	$I_{YMXYFI18}$	 - -	 - -	 200 4.0	mA
Current Limit	$I_{LIMYMXYFI18}$	-	300	-	mA
Transient Load Change	$\Delta I_{YMXYFI18}$	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, $I_{YMXYFI18}$ = 150 mA), (V_{21} = 2.1 V or V_{PWR} = 3.6 V)	$PSRR_{YMXYFI18}$	40	-	-	dB
Output Noise (10 Hz to 100 kHz, $I_{YMXYFI18}$ = 200 mA), (V_{21} = 2.1 V or V_{PWR} = 3.6 V)	$V_{NOISEYMXYFI18}$	-	-	40	μV_{RMS}
Effective Quiescent Current Consumption Active Mode Low Power Mode	$I_{QYMXYFI18}$	 - -	 - -	 18 10	µA

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VCCPAOAC ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	$V_{CCPAOAC}$	-	1.05	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{CCPAOACUV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{CCPAOACUVH}$	-	1.0	-	%
Continuous Output Load Current	$I_{CCPAOAC}$				mA
Active Mode		-	-	155	
Low Power Mode		-	-	3.1	
Current Limit	$I_{LIMCCPAOAC}$	-	232.5	-	mA
Transient Load Change	$\Delta I_{CCPAOAC}$	-	-	50	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, $I_{CCPAOAC}$ = 116 mA, V_{15} = 1.5 V)	$PSRR_{CCPAOAC}$	50	60	-	dB
Effective Quiescent Current Consumption	$I_{QCCPAOAC}$				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VCCPDDR ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{CCPDDR}	-	1.05	-	V
Output Voltage Accuracy	-	-2.0	-	2.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{CCPDDRUV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{CCPDDRUVH}$	-	1.0	-	%
Continuous Output Load Current	I_{CCPDDR}				mA
Active Mode		-	-	60	
Low Power Mode		-	-	1.2	
Current Limit	$I_{LIMCCPDDR}$	-	90	-	mA
Transient Load Change	ΔI_{CCPDDR}	-	-	10	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CCPDDR} = 45 mA, V_{15} = 1.5 V)	$PSRR_{CCPDDR}$	50	60	-	dB
Effective Quiescent Current Consumption	$I_{QCCPDDR}$				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VAON ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{AON}	-	1.2	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{AONUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{AONUVH}	-	1.0	-	%

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Continuous Output Load Current	I_{AON}				mA
Active Mode		-	-	250	
Low Power Mode		-	-	5.0	
Current Limit	I_{LIMAON}	-	375	-	mA
Transient Load Change	ΔI_{AON}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{AON} = 187.5 mA, V_{15} = 1.5 V)	$PSRR_{AON}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QAON}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VMM ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{MM}	-	1.2	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{MMUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{MMUVH}	-	1.0	-	%
Continuous Output Load Current	I_{MM}				mA
Active Mode		-	-	5.0	
Low Power Mode		-	-	0.1	
Current Limit	I_{LIMMM}	-	25	-	mA
Transient Load Change	ΔI_{MM}	-	-	3.0	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{MM} = 4.0 mA, V_{15} = 1.5 V)	$PSRR_{MM}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QMM}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VCCP ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{15}	1.425	1.5	1.680	V
Output Voltage Setting	V_{CCP}	-	1.05	-	V
Output Voltage Accuracy	-	-5	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{CCPUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	V_{CCPUVH}	-	1.0	-	%
Continuous Output Load Current	I_{CCP}				mA
Active Mode		-	-	445	
Low Power Mode		-	-	8.9	
Current Limit	I_{LIMCCP}	-	667.5	-	mA
Transient Load Change	ΔI_{CCP}	-	-	100	mA

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{CCP} = 334 mA, V_{15} = 1.5 V)	$PSRR_{CCP}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QCCP}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VIMG25 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Output Voltage Setting	V_{IMG25}	-	2.5	-	V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{IMG25UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{IMG25UVH}$	-	1.0	-	%
Continuous Output Load Current	I_{IMG25}				mA
Active Mode		-	-	80	
Low Power Mode		-	-	1.6	
Current Limit	$I_{LIMIMG25}$	-	120	-	mA
Transient Load Change	ΔI_{IMG25}	-	-	10	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{IMG25} = 60 mA, V_{PWR} = 3.3 V)	$PSRR_{IMG25}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QIMG25}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VIMG28 ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.0	3.6	4.4	V
Output Voltage Setting	V_{IMG28}	(Selectable, see Table 43)			V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	$V_{IMG28UV}$	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{IMG28UVH}$	-	1.0	-	%
Continuous Output Load Current	I_{IMG28}				mA
Active Mode		-	-	225	
Low Power Mode		-	-	4.5	
Current Limit	$I_{LIMIMG28}$	-	337.5	-	mA
Transient Load Change	ΔI_{IMG28}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{IMG28} = 169 mA, V_{PWR} = 3.3 V)	$PSRR_{IMG28}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QIMG28}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VSDIO ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.135	3.3	3.465	V
Output Voltage Setting	V_{SDIO}	(Selectable, see Table 44)			V
Output Voltage Accuracy	-	-5.0	-	5.0	%
Under-voltage Detection Threshold (With respect to the output voltage)	V_{SDIOUV}	-	-12	-	%
Under-voltage Detection Threshold Hysteresis	$V_{SDIOUVH}$	-	1.0	-	%
Continuous Output Load Current	I_{SDIO}				mA
Active Mode		-	-	215	
Low Power Mode		-	-	4.3	
Current Limit	$I_{LIMSDIO}$	-	322.5	-	mA
Transient Load Change	ΔI_{SDIO}	-	-	100	mA
Power Supply Rejection Ratio (PSRR) (20 to 100 kHz, I_{SDIO} = 161 mA, V_{PWR} = 3.3 V)	$PSRR_{SDIO}$	50	60	-	dB
Effective Quiescent Current Consumption	I_{QSDIO}				µA
Active Mode		-	-	18	
Low Power Mode		-	-	10	
VPNL33 POWER SWITCH ELECTRICAL CHARACTERISTICS					
Input Voltage Range	V_{PWR}	3.135	3.3	3.465	V
Drop Across Switch with reference to V_{PWR}	-	-	-	3.0	%
Continuous Output Load Current	I_{PNL33}	-	-	100	mA
ADC ELECTRICAL CHARACTERISTICS					
Conversion Current	-	-	-	1.2	mA
OFF Supply Current	-	-	-	1.0	µA
Converter Reference Voltage	-	-	2.4	-	V
Integral Nonlinearity (Rs = 5.0 kΩ maximum) (6)	-	-	-	±3.0	LSB
Differential Nonlinearity (Rs = 5.0 kΩ maximum) (6)	-	-	-	±1.0	LSB
Zero Scale Error (Offset) (Rs = 5.0 kΩ maximum) (6)	-	-	-	10	LSB
Full Scale Error (Gain) (Rs = 5.0 kΩ maximum) (6), (7)	-	-	-	11	LSB
Drift Over Temperature				±2.0	LSB
Source Impedance					
No Bypass Capacitor at Input	-	-	-	5.0	kΩ
Bypass Capacitor at Input of (10 nF)	-	-	-	30	kΩ
Input Buffer Input Range(8)	-	0.02	-	2.4	V

Notes
6. Rs represents a possible external series resistor between the voltage source and the ADIN input.
7. At room temperature.
8. Refer to Table 57 for analog valid input range and input buffer range characteristics for each ADC Channel

Table 3. Static Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
GPIOS ELECTRICAL CHARACTERISTICS					
GPIO Voltage Level (This is wired externally though GPIOVCC pin)	$V_{GPIOVCC}$	-	1.8 V, 2.5 V, 3.3 V	-	V
GPO Voltage Level (This is wired externally though GPOVCC pin)	V_{GPOVCC}	-	1.8 V, 2.5 V, 3.3 V	-	V
Accuracy for GPIOVCC, GPOVCC	-	-5.0	-	5.0	%
GPIO Output Drive Capability	-	-	20	-	Ω
Input Low Voltage	V_{IL}	0	-	0.3*V_{CC}	V
Input High Voltage	V_{IH}	0.7*V_{CC}	-	V_{CC}	V
Output Low Voltage (V_{CC} = V_{CC_MIN}, I_{OL} = 4.0 mA)	V_{OL}	-	-	0.1	V
Output High Voltage (V_{CC} = V_{CC_MIN}, I_{OH} = -4.0 mA)	V_{OL}	V_{CC}-0.1	-	-	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE TIMING AND LOGIC IO					
Time SPICSB has to be low before the first rising edge of SPICLK	t_{SELSU}	20	-	-	ns
Time SPICSB has to remain low after the last falling edge of SPICLK	t_{SELHLD}	20	-	-	ns
Time SPICSB has to remain high between two transfers	$t_{SELHIGH}$	20	-	-	ns
Clock period of SPICLK (Equivalent to a maximum clock frequency of 25 MHz)	t_{CLKPER}	40	-	-	ns
Part of the clock period where SPICLK has to remain high	$t_{CLKHIGH}$	18	-	-	ns
Part of the clock period where SPICLK has to remain low	t_{CLKLOW}	18	-	-	ns
Time MOSI has to be stable before the next falling edge of SPICLK	t_{WRTSU}	5.0	-	-	ns
Time MOSI has to remain stable after the falling edge of SPICLK	t_{WRTHLD}	5.0	-	-	ns
Time MISO will be stable before the next falling edge of SPICLK	t_{RDSU}	5.0	-	-	ns
Time MISO will remain stable after the falling edge of SPICLK	t_{RDHLD}	5.0	-	-	ns
Time MISO needs to become active after the falling edge of SPICSB	t_{RDEN}	Refer to Figure 6 for more details			
Time MISO needs to become inactive after the rising edge of SPICSB	t_{RDDIS}	5.0	-	-	ns
VIDEN/VID TIMING SPECIFICATION					
VIDEN/VID Debounce time	t_{DB}	100	-	400	ns
VIDEN Invalid State Hold Time	t_{HOLD}	1.0	-	-	µs
OSCILLATOR AND CLOCK OUTPUTS MAIN CHARACTERISTICS					
RTC OSC Startup Time (Upon Application of Power)	-	-	-	500	ms
RTC					
RTC Clock Frequency, Crystal OSC Nominal Frequency	-	-	32.768	-	KHz
VCC ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CC}/t	-	-	1.0	A/ns
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V (25 mV/s))	t_{SSCC}	-	-	0.06	ms
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{CCOFF}	-	-	1.0	ms
DAC Slew Rate	-	-	25	-	mV/µs
Switching Frequency	f_{SW}	-	1.0	-	MHz
VNN ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{NN}/t	-	-	1.0	A/ns
Soft Start Time (Enable to output voltage ramp up from 0 V to 1.0 V (25 mV/s))	t_{SSNN}	-	-	0.06	ms
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{NNOFF}	-	-	1.0	ms
DAC Slew Rate	-	-	25	-	mV/µs
Switching Frequency	f_{SW}	-	1.0	-	MHz

Table 4. Dynamic Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VDDQ ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{DDQ}/t	-	-	1.0	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	t_{SSDDQ}	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{DDQOFF}	-	-	1.0	ms
Switching Frequency	f_{SW}	-	4.0	-	MHz
V21 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{21}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 V to 2.1 V)	t_{SS21}	-	-	84	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{21OFF}	-	-	1.0	ms
Switching Frequency	f_{SW}	-	4.0	-	MHz
V15 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{15}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.1 V)	t_{SS15}	-	-	100	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{15OFF}	-	-	1.0	ms
Switching Frequency	f_{SW}	-	4.0	-	MHz
VBG ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{BG}/t	-	-	0.001	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	t_{SSBG}	-	-	20	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{BGOFF}	-	-	5.0	ms
VCCA ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CCA}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.5 V)	t_{SSCCA}	-	-	30	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{CCAOFF}	-	-	5.0	ms
VCC180 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CC180}/t	-	-	1.0	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	$t_{SSCC180}$	-	-	30	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{CC180OFF}$	-	-	5.0	ms
VPNL18 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{PNL18}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	$t_{SSPNL18}$	-	-	140	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{PNL18OFF}$	-	-	5.0	ms
VPMIC ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{PMIC}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	t_{SSPMIC}	-	-	700	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{PMICOFF}$	-	-	5.0	ms

Table 4. Dynamic Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VYMXYFI18 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	$I_{YMXYFI18}/t$	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	$t_{SSYMXYFI18}$	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{YMXYFI18OFF}$	-	-	5.0	ms
VCCPAOAC ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	$I_{CCPAOAC}/t$	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	$t_{SSCCPAOAC}$	-	-	30	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{CCPAOACOFF}$	-	-	5.0	ms
VCCPDDR ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CCPDDR}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	$t_{SSCCPDDR}$	-	-	35	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{CCPDDROFF}$	-	-	5.0	ms
VAON ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{AON}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	t_{SSAON}	-	-	25	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{AONOFF}	-	-	5.0	ms
VMM ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{MM}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.2 V)	t_{SSMM}	-	-	125	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{MMOFF}	-	-	5.0	ms
VCCP ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{CCP}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.0 V)	t_{SSCCP}	-	-	26	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	t_{CCPOFF}	-	-	5.0	ms
VIMG25 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{IMG25}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.5 V)	$t_{SSIMG25}$	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{IMG25OFF}$	-	-	5.0	ms
VIMG28 ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{IMG28}/t	-	-	0.1	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 2.9 V)	$t_{SSIMG28}$	-	-	200	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{IMG28OFF}$	-	-	5.0	ms

Table 4. Dynamic Electrical Characteristics

T_A = -40 to 85 °C, V_{PWR} = 3.0 to 4.4 V, in gathering these parametrics, Freescale used the external components described in the Hardware Design Considerations section of this document, over the full load current range, unless otherwise noted. Typical values are characterized at V_{PWR} = 3.6 V and 25 °C.

Characteristic	Symbol	Min	Typ	Max	Unit
VSDIO ELECTRICAL CHARACTERISTICS					
Transient Load Speed of Change	I_{SDIO}/t	-	-	0.01	A/µs
Soft Start Time (Enable to output voltage ramp up from 0 to 1.8 V)	t_{SSSDIO}	-	-	100	µs
Turn Off Time (OFF to output voltage ramp down to 0 V)	$t_{SDIOOFF}$	-	-	5.0	ms
POWER SWITCHES ELECTRICAL CHARACTERISTICS					
Ramp Up Time		-	-	50	µs
ADC ELECTRICAL CHARACTERISTICS					
Conversion Time Per Channel		-	-	10	µs
Turn on/off Time		-	-	31	µs

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

The 900844 is a high efficiency Power Management Integrated Circuit (PMIC). It is optimized for Ultra-mobile platforms for Netbook, Tablets, Slates, embedded devices, and other applications requiring “multi-cell” battery voltage.

The 900844 PMIC, is designed to provide CPU power requirements and control as an integral part of Freescale's power management solution to meet the needs of Ultra-mobile platforms.

Optimum partitioning, high feature integration, and state of the art technology, enable Freescale to support Ultra-mobile platforms that are cost effective, by reducing component count and board area. The Freescale solution also allows ease of system design, resulting in a faster time to market development cycle.

It accepts input from a supply in the range of 3.0 to 4.4 V (for example, from a multi-cell battery scaled down to 3.3 V) to deliver regulated power to various components (CPU, chip sets, wireless, memory, storage, display, sensors, and others) on Ultra-mobile platforms.

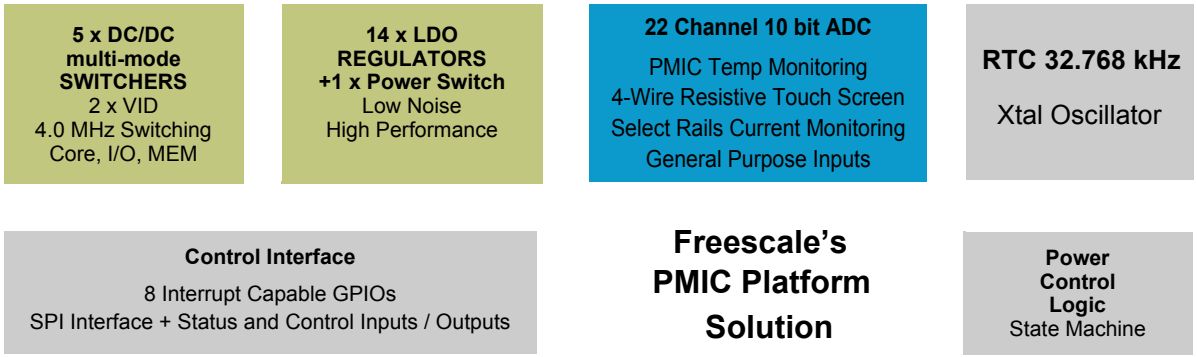


Figure 4. Power Management Solution - High Level Block Diagram

FEATURE LIST

- Netbook, Tablets, and embedded devices, Ultra-mobile platform Architecture Support
- Fully Programmable DC/DC Switching, Low Drop-Out Regulators, and Load Switches
  - Delivers regulated reliable power to various system components
  - High efficiency multi mode power conversion ensuring extended battery life
  - Fully programmable with extensive protection features and complete fault reporting for best in class overall system reliability
  - Internal Compensation
  - 5 Buck DC/DC Regulators
    - 2x VID Controlled with 1.0 MHz switching and external switches for CPU and Graphics core support
    - 3x with 4.0 MHz switching and integrated MOSFET for platform support and LDO supply for optimized thermal performance and power efficiency.
  - 14 Low Dropout (LDO) regulators.
  - One configurable LDO/Switch regulator for SDIO card support
  - A 3.3 V load switch for platform support
- Coin Cell Backup battery charger
- SPI communication interface (up to 25 MHz operation)
- 22 channel (32 capable) 10-bit ADC for internal and external sensing with touch screen interface
- Low power 32.786 kHz XTAL oscillator.
- Real Time Clock (RTC) to provide time reference and alarm functions with wake up control.
- Eight Interrupt capable GPIOs and 8 GPOs
- Various control and status reporting I/Os
- Interrupt and Reset controller. All interrupt signals can be masked.
- Overall solution size target of < 400 mm^2 (including clearance and routing)
- Operating temperature of -40 to +85 °C

FUNCTIONAL BLOCK DIAGRAM

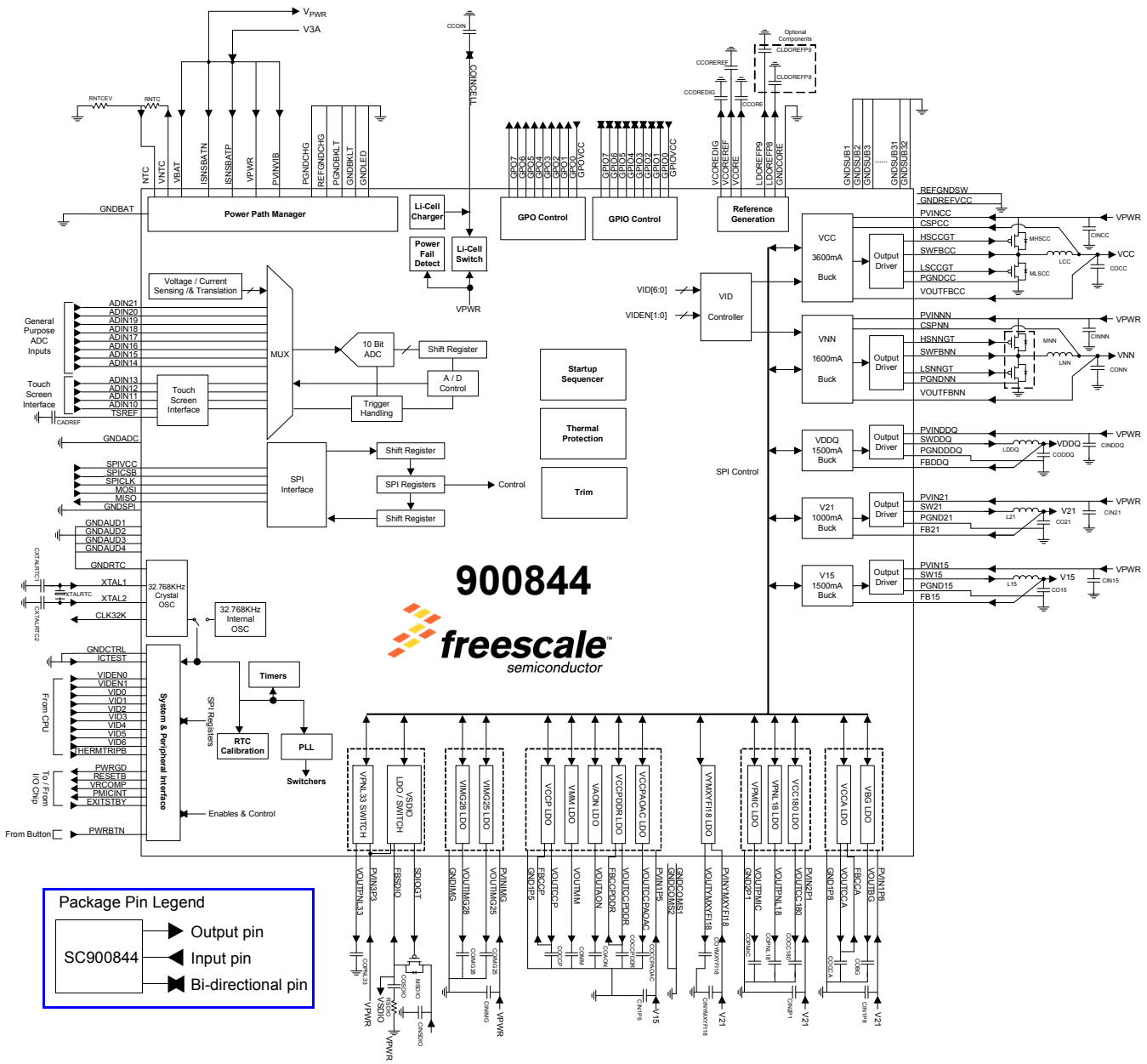


Figure 5. 900844 Functional Block Diagram

The component list for those items listed in this schematic can be found in the External Components BOM [(23)].

FUNCTIONAL DEVICE OPERATION

SYSTEM CONTROL INTERFACE

OVERVIEW

This section addresses the various interfaces and I/Os between the PMIC solution and the rest of the system.

The system control interface includes the following:

- SPI interface.
- Interrupt controller
- Platform sideband signals
- Special registers

SPI INTERFACE

The 900844 contains a SPI interface port which allows a host controller to access the register set. Using these registers, 900844 resources can be controlled. The registers also provide information on the PMIC status, as well as information on external signals.

The addressable register map spans 1024 registers of 8 data bits each. The map is not fully populated. A detailed structure of the register set along with bit names, positions, and basic descriptions, are given in Table 74. Expanded bit descriptions are included in the individual functional sections for application guidance.

Note that not all bits are truly writable. Refer to the individual sub-circuit descriptions and Table 74 to determine the read/write capability of each bit.

Table 5. SPI Interface Pin Functionality

Pin Name	SPI Functionality
SPICLK	SPI Clock Input (up to 25 MHz)
MOSI	Master Out / Slave In (Serial Data In)
MISO	Master In / Slave Out (Serial Data Out)
SPICSB	Chip Select (Active Low)
SPIVCC	SPI Bus Supply - 1.8 V typical

The System Controller Unit (SCU) within the Platform Controller Hub (PCH) is the master, while the PMIC is the slave. The SPI interface operates at a typical frequency of 12.5 MHz, and at a maximum frequency of 25 MHz, with lower speeds supported.

The SPI interface is configured in mode 1: clock polarity is active high (CPOL = 0), and data is latched on the falling edge of the clock (CPHA = 1). The chip select signal, SPICSB, is active low. The SPICSB line must remain active during the entire SPI transfer. The MISO line will be tri-stated while SPICSB is high.

The SPI frame consists of 24 bits: a Read/Write bit, a 10-bit address code (MSB first), 5 "dead" bits and 8 data bits (also MSB first). The Read/Write bit selects whether the SPI transaction is a read or a write: for a write operation, the R/W bit must be a one; for a read operation, it must be a zero.

For a read transaction, any data on the MOSI pin after the address bits is ignored. The MISO pin will output the data field pointed to by the 10-bit address loaded at the beginning of the SPI sequence. SPI read backs of the address field and unused bits are returned as zero. For read operations, the PMIC supports address auto-increment.

For a write operation, once all the data bits are written, the data is transferred into the registers on the falling edge of the 24th clock cycle. All unused SPI bits in each register must be written to a zero.

To start a new SPI transfer, the SPICSB line must go inactive and then active. After the LSB of data is sent, if the SPICSB line is held low, up to seven additional address/data packets may be sent as writes to the PMIC. Refer to the VRCOMP Pin section.

The following diagrams illustrate the SPI Write Protocol, SPI Read Protocol, and SPI Timing.

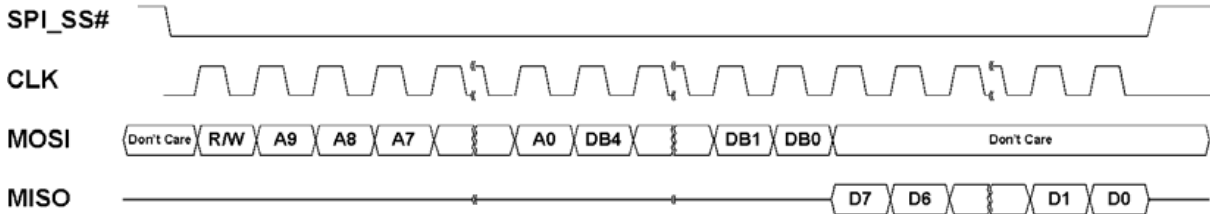


Figure 6. SPI Read from PMIC Diagram (One Address/Data Packet shown)

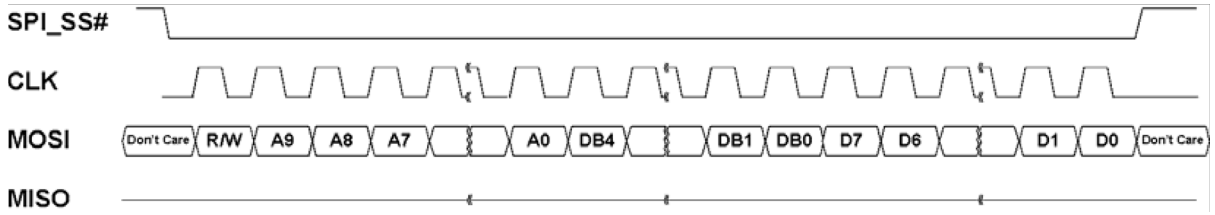


Figure 7. SPI Write to PMIC Diagram (One address/Data Packet Shown)

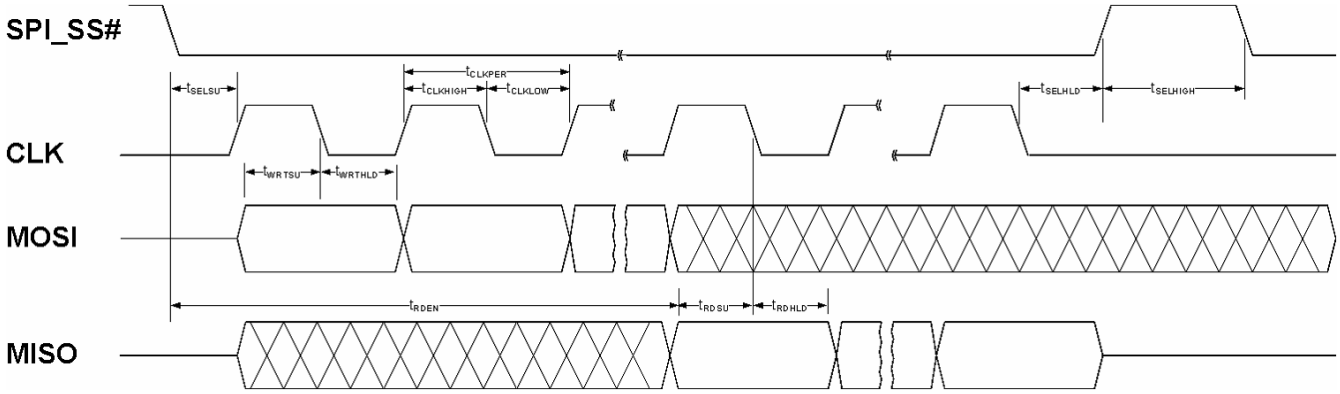


Figure 8. SPI Interface Timing Diagram (Processor Input capacitance is 3.0 pF)

INTERRUPT CONTROLLER

Control

The PMIC informs the system of important events using interrupts. Unmasked interrupt events are signaled to the host by driving the PMICINT pin high.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. If a new interrupt occurs while the controller clears an existing interrupt bit, the interrupt line will remain high.

Each interrupt can be masked by setting the corresponding mask bit to a ‘1’. As a result, when a masked interrupt bit goes high, the interrupt line will not go high. A masked interrupt can still be read from the register. If a masked interrupt bit was already high, the interrupt line will go high after unmasking.

The following is the interrupt handling mechanism which has inherent latency that the clients must expect:

1. PMIC interrupts SCU, if both the 1st and 2nd level bits are not masked.
2. SCU reads PMIC master, 1st level, interrupt event register.
3. SCU then traverses all the branches of the interrupt tree where events are indicated.
4. SCU will service events in leaf node registers.

When an unmasked interrupt event happens:

- The 2nd level bit is set.
- The 1st level bit is set by a rising edge sent from the 2nd level register, and the PMICINT signal goes from low to high
- When the system controller, the SCU, reads the 1st level register the 2nd level registers that were set, remain set. Any unset registers are free to accept an interrupt event.
- When the 1st level register is read, any 1st level register bits that were set at the point the SPI read strobe shifts the register value into the SPI transmit shift register, that bit will be cleared by the SPI self clear signal immediately following the read strobe. This allows new interrupts to be recorded without being lost. If all unmasked 1st level bits get cleared by the read, the PIMCINT pin will de-assert. If a new unmasked 1st level interrupt event happens, just after the read of the 1st level register, the PIMCINT pin interrupt pin will remain asserted. The SCU reads each 2nd level register and these are cleared on read.
- When the 2nd level register is read, any 2nd level register bits that were set at the point the SPI read strobe sweeps, the register value into the SPI transmit shift register, that bit will be cleared by the SPI self clear signal immediately following the read strobe. This allows new interrupts to be recorded without being lost. If a new unmasked 2nd level interrupt event happens just after the read of the 2nd level register, the PMICINT pin will assert if the 1st level bit is not masked.

Table 6. Interrupt Registers Summary

Block	ADDR	Register Name	RW	D7	D6	D5	D4	D3	D2	D1	D0	Initial
IRQ	0x04	INTERRUPT	R	EXT	AUX	VRFAULT	GPIO	RTC	CHR	ADC	PWRBTN	0x00
IRQ	0x05	INTMASK	R/W	MEXT	MAUX	MVRFAULT	MGPIO	MRTC	MCHR	MADC	MPWRBTN	0xFA
RTC	0x1C	RTCC	R	IRQF	PF (=0)	AF	UF	RSVD	RSVD	RSVD	RSVD	0x00
POWER	0x30	VRFAULTINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	VRFAIL	BATOCP	THRM	0x00
POWER	0x31	MVRFAULTINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MVRFAIL	MBATOCP	MTHRM	0x03
ADC	0x5F	ADCINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	OVERFLOW	PENDET	RND	0x00
ADC	0x60	MADCINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MOVERFLOW	MPENDET	MRND	0x00
GPIO	0xE8	GPIOINT	R	GPIINT7	GPIINT6	GPIINT5	GPIINT4	GPIINT3	GPIINT2	GPIINT1	GPIINT0	0x00

Notes

9. Because of the design of the clear on read logic, any interrupt event is allowed to happen at any time. If the interrupt event happens close to when a read of the interrupt register happens, if the SPI read captures that interrupt bit as being set, then that bit will get cleared. If the read does not capture the bit as being set, it will not be cleared. In this way no interrupt events are lost.
10. The 2nd level interrupts that get "Ored" together to set the 1st level interrupt bits can block other 2nd level interrupts from setting the 1st level interrupt register. This is because if any of the 2nd level interrupts is high, the output of the OR will remain high, blocking the other 2nd level interrupt's rising edge. This should not be a problem. because when the 2nd level register is read, the SCU will see all the bits that are active when it is read. The software will decide which one to service first, just as it needs to do when more than one 1st level interrupt bits are set when that register is read.
11. Masking has no affect on interrupt bits being set or cleared. Masking just prevents the interrupt event from asserting the interrupt pin. If an interrupt bit is set, but is masked, the interrupt pin does not assert. If the mask bit is cleared while the bit is still set, the interrupt pin will assert. Most interrupt registers have 1st and 2nd level mask bits. Both mask bits must be in the unmasked state to generate an interrupt to the SCU.
12. Some 2nd level interrupt registers are level sensitive. If the level that sets these interrupts registers is active when the register is read, it will clear during the active time of the clear on read signal and then reassert. This will reassert the 1st level interrupt bit.
13. The GPIO interrupts do not have interrupt masking bits, they have interrupt prevention bits. This is controlled by bits 5:4 of the GPIO control register. See GPIOs for more details on using the GPIO as interrupt inputs.
14. Interrupts generated by external events are de-bounced. Therefore, the event needs to be stable throughout the de-bounce period before an interrupt is generated. Nominal de-bounce periods for each event are documented in Table 7. Due to the asynchronous nature of the de-bounce timer, the effective de-bounce time can vary slightly.

Interrupt Bit Summary

Table 7 summarizes all 1st and 2nd level interrupt bits associated with the Interrupt Controller. For more detailed behavioral descriptions, refer to the related sections.

Table 7. Interrupt Bit Summary

1st Level		2nd Level		Interrupt Event Condition	Detect	Debounce time
Name	**Bit**	**Name**	**Bit**			
PWRBTN	D0	-	-	PWRBTN falling edge detection	Falling	10 ms
ADC	D1	RND	D0	ADC Round Robin Cycle Complete	Hi Level	-
		PENDET	D1	Touch Screen Wake-up	Rising	-
		RSVD	D7:D2	-	-	-
CHR	D2	RSVD	D0	-	-	-
		BATOVP	D1	Battery Over-voltage	Rising/Falling	(16)
		TEMP	D2	Battery Temperature Outside Valid Window	Hi Level	1.0 ms
		RSVD	D3	-	-	-
		RSVD	D4	-	-	-
		BATDET	D5	Battery Connect/Disconnect	Hi Level	0.5 sec
		RSVD	D6	-	-	-
		USBOVP	D7	Input Over-voltage Reached	Hi level	10 ms
RTC	D3	RSVD	D3:D0	-	-	-
		UF	D4	Update Cycle	Hi Level	-
		AF	D5	Current Time = Alarm Time	Hi Level	-
		RSVD	D6	-	-	-
		IRQF	D7	IRQF=UIE*UF + AIE*AF	Hi Level	-
GPIO	D4	GPINT0	D0	Edge Detect	Rising/Falling/Both	GPIDBNC0
		GPINT1	D1	Edge Detect	Rising/Falling/Both	GPIDBNC1
		GPINT2	D2	Edge Detect	Rising/Falling/Both	GPIDBNC2
		GPINT3	D3	Edge Detect	Rising/Falling/Both	GPIDBNC3
		GPINT4	D4	Edge Detect	Rising/Falling/Both	GPIDBNC4
		GPINT5	D5	Edge Detect	Rising/Falling/Both	GPIDBNC5
		GPINT6	D6	Edge Detect	Rising/Falling/Both	GPIDBNC6
		GPINT7	D7	Edge Detect	Rising/Falling/Both	GPIDBNC7
VRFAULT	D5	THRM	D0	Junction Temperature > Thermal Warning Threshold	Hi Level	10 ms
		RSVD	D1	-	-	-
		VRFAIL	D2	Regulator Fault Present	Hi Level	(15)
		RSVD	D7:D3	-	-	-
AUX	D6	RSVD	D0	-	-	-
		RSVD	D1	-	-	-
		RSVD	D0	-	-	-
		RSVD	D1	-	-	-
		RSVD	D7:D4	-	-	-
EXT	D7	Not supported				

Notes

15. Varies by regulator. Normally it is 1.5 times the regulator turn on time.
16. 32 ms rising and 120 μs falling

SIDEBAND SIGNALS

The following pins are included as part of the Sideband signals:

Table 8. Sidebands Pin Functionality

Pin Name	I/O	Pin Functionality
PMICINT	O	Active high PMIC Interrupt Output pin
VRCOMP	O	Active high Voltage Regulator Complete signal
RESETB	O	Active low hard reset for Platform controller hub
PWRGD	O	Active high Power Good Output signal
EXITSTBY	I	Active high Exit Standby signal
THRMTRIPB	I	Active low Thermal Trip Assertion Input signal
VIDEN[1:0]	I	Active high Input signals driven by the CPU, to indicate if the VID bus is addressing VCC or VNN.
VID[6:0]	I	Active high input signals driven by the CPU, to indicate the output voltage setting for the VCC and VNN rails.

PMCINT Pin

The PMICINT pin interrupts the platform controller hub by rising from low to high when an unmasked interrupt event occurs. It is a level sensitive pin and it is cleared when the platform controller hub reads the Interrupt registers. Reference Interrupt Controller for a more detailed explanation of the Interrupt mechanism.

The PMICINT pin follows the DC Signaling specifications in Table 3 with a reference of 1.8 V (VPMIC).

VRCOMP Pin

This is an active high voltage regulator complete signal. It is asserted low by the PMIC when a SPI voltage regulation request, or other write request has been decoded. The signal is de-asserted on completion of the request (i.e. the rail is in regulation). This signal is relevant to the SPI initiated writes and EXITSTBY assertion.

The VRCOMP pin follows the DC Signaling specifications in Table 3 with a reference of 1.8 V (VPMIC).

Figure 9 illustrates the Voltage Regulators register write cycles and VRCOMP functionality. The rising edge on the SPICSB pin indicates the end of the block of Voltage Regulators configurations, at which point the VRCOMP pin is driven low. As an address/data block is written, the PMIC can start to ramp those rails (DC-DC, LDO, or switch). Once all of the rails are in regulation, the PMIC drives the VRCOMP pin high, indicating to the platform controller hub that the voltage regulator configuration request is completed, and the PMIC is ready for subsequent transactions. The maximum number of voltage regulator change packets (address/data combinations) is 8. The voltage regulators should ramp at the rate defined in the regulators tables. Due to the relatively long turn-off time of the voltage regulators, the VRCOMP signal is to be gated-off after a 500 ns minimum (30 ms max.) low time.

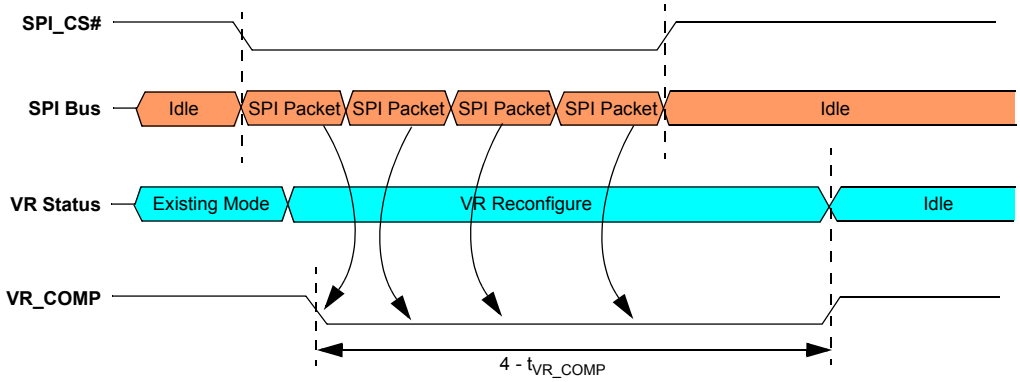


Figure 9. VRCOMP Functionality in a SPI Voltage Regulators Configuration

$\overline{\text{RESET}}$ Pin

This is an active low, hard reset for the platform controller hub. When this pin is asserted, the platform controller hub returns to its initial default state. This signal can be asserted when a cold or warm reset is initiated, depending on the settings in the CHIPCNTL register.

The $\overline{\text{RESET}}$ pin follows the DC Signaling specifications in Table 3 with a VCC of 1.8 V (VPMIC)

PWRGD Pin

This is a Power Good output signal from the 900844 to the Platform controller hub. Assertion of PWRGD means that the VCCPAOAC, VAON, and VPMIC rails have been valid for at least 100 microseconds. The Platform Controller Hub will remain off until this signal is asserted. This signal is only de-asserted if VCCPAOAC, VAON, or VPMIC is out of regulation, or a cold reset is initiated by the firmware.

The PWRGD pin follows the DC signaling specifications in Table 3 with a reference of 1.8 V (VPMIC)

WARM and COLD RESET

The $\overline{\text{RESET}}$ and PWRGD signals have two functions which are initiated through the register file. Together they define a warm reset or cold reset to the platform controller hub. The sequencing shown in Figure 10 and is controlled from the register CHIPCNTRL through bits WARMRST and COLDRST. The pulse will be held low for 5.0 μs < t < 31 μs.

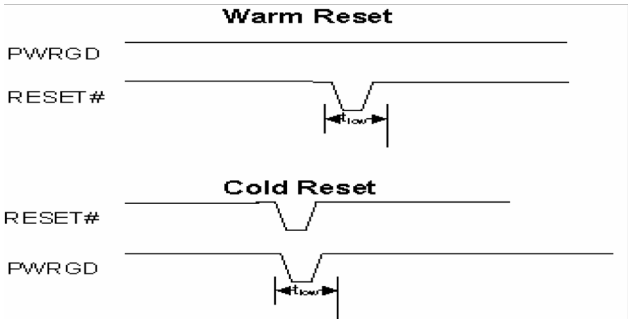


Figure 10. Warm/Cold Reset Functionality

Table 9. CHIPCNTL Register Structure and Bit Description

Name	Bits	Description
CHIPCNTL (ADDR 0x 06 - R/W - Default Value: 0x00)		
COLDRST	0	Cold Reset Function Enable x0 = No Change x1 = Pulse $\overline{\text{RESET}}$ and PWRGD Low
WARMRST	1	Warm Reset Function Enable x0 = No Change x1 = Pulse $\overline{\text{RESET}}$ Low
Reserved	7:2	Reserved

EXITSTBY Pin

When the EXITSTBY pin is asserted high, the 900844 exits the AOAC standby settings for regulating the platform supplies. When asserted, the PMIC switches the voltage regulators, as defined in the voltage regulator registers from the CTL bits to the AOACTL bits. This is a low latency voltage regulators context switch.

EXITSTBY pin follows the DC signaling specifications in Table 3 with a reference of 1.05 V (V_{CCP})

AOAC Exit Standby

When the EXITSTBY signal is asserted high from the Platform controller hub, the VRCOMP signal will be driven low. The AOACTL bits will be copied to the CTL bits in the different voltage regulator control registers on the rising edge of the EXITSTBY signal, unless Bit 5 is '0'. If Bit 5 is '0', then the CTL bits are not modified. The VRCOMP signal is de-asserted at this point. The rails defined in the new CTL registers will be ramped up together or remain in the same state, as if the AOACTL settings were the same as the previous CTL setting. Once all of the rails are in regulation, the VRCOMP signal will be driven high.

Figure 11 shows the timing diagram of the EXITSTBY signal. There is a special case (optimized case) when the EXITSTBY signal is asserted with the VCCP, VCCPDDR, VCCA, and VCC180 rails. If some combination of these four rails turn on with the assertion of the EXITSTBY signal, the entire time for the re-configuration should take no longer than 30 ms. See Figure 12.

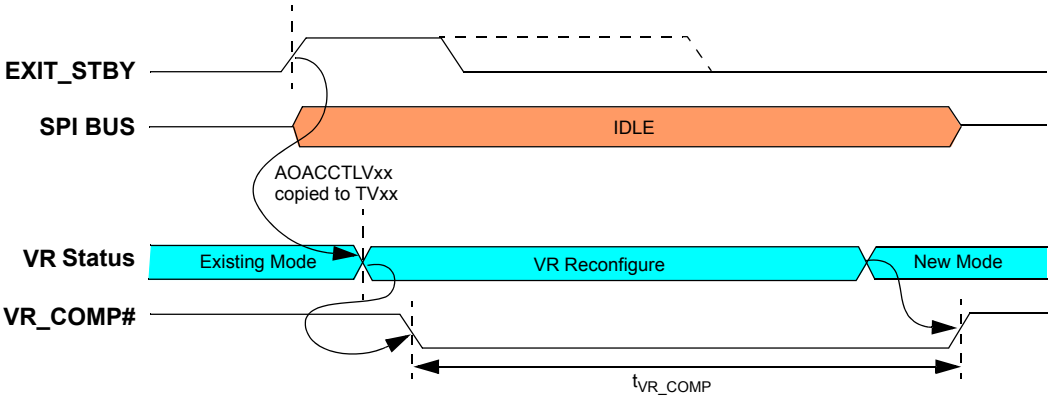


Figure 11. General Exit Standby Diagram

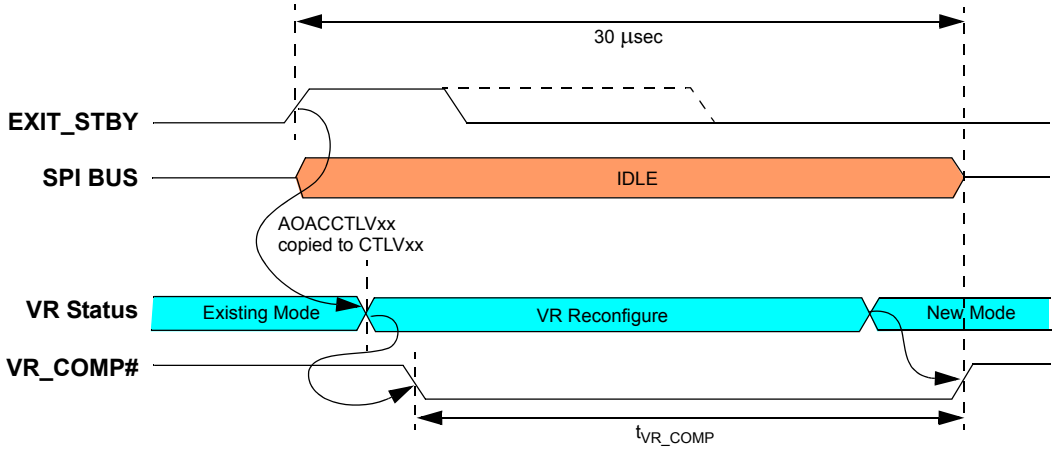


Figure 12. Optimized Exit Standby Diagram

The power-on default AOACCTLVxx register setting for the VCCP, VCCPDDR, VCCA, and VCC180 rails, are to be turned on by the assertion of the EXITSTBY signal. However, every regulator has an AOACCTLVxx register setting, and can be configured to turn on, turn off, or have no change. The power-on default AOACCTLVxx register setting for all other regulators is set to no change. Note that the V_{DDQ} regulator has to be enabled in order for the V_{CCA} regulator to turn on.

THERMTRIPB Pin

THERMTRIPB is an active low Thermal Trip input signal. It is asserted by the CPU to indicate a catastrophic thermal event. On the falling edge of THERMTRIPB, the PMIC has 500 ms to sequence off all rails from the highest to lowest. The PMIC will turn on automatically upon detecting a turn on event, at which point the cold boot flow should be followed as shown in Turn on Events.

The PMIC provides a weak (50 -100 kΩ) pull-up to VCCPAOAC. The PMIC only responds to a THERMTRIPB signal if the V_{CCP} regulator is on. The platform controller hub output driver is a nominal 55 Ω.

The THERMTRIPB pin follows the DC Signaling specifications in Table 3 with a reference of 1.05 V (VCCPAOAC).

VIDEN[1:0] & VID[6:0] Pins

Both VCC and VNN regulators are variable in the CPU and supply two different sub-systems. The CPU implements a VID mechanism that minimizes the number of required pins. The VID for VNN and VCC are multiplexed on to the same set of pins, and a separate 2-bit enable/ID is defined to specify to which sub-system the driven VID corresponds. One of the combinations notifies that the VID is invalid. This is used when the CPU is in C6/Standby, to tri-state the VID pins to save power.

Table 10. VIDEN Selections

VIDEN[1:0] Bits		Selection
0	0	Invalid
0	1	VCC
1	0	VNN
1	1	Unused

Both VCC and VNN have initial boot voltage (VCC V_{BOOT} = 1.1 V; VNN V_{BOOT} = 0.9 V) settings that the platform controller hub sets to the VNN and VCC regulators by a SPI write to the VNNLATCH and VCCLATCH registers. Once all of the platform voltage rails are up, the CPU will drive the VID and VIDEN signals to set the VNN and VCC output voltage to the appropriate level. The VID and VIDEN signals will go through the sequence INVALID >> VNN >> INVALID >> VCC.

VID[6:0] and VIDEN[1:0] will transition together and the PMIC must de-bounce the VID[6:0] and VIDEN[1:0] for 100 to 400 ns. The CPU will hold these signals valid for at least 500 ns. VID signals are disabled from controlling VCC/VNN unless the V_{CCP} regulator is enabled

Both regulators support dynamic VID transitioning during normal runtime operation. Dynamic VIDs require the CPU to change the VIDEN signals for the VNN regulator to INVALID each time, to change the VNN output voltage. The VCC regulator is different in that it does not require the VIDEN signals to change to change the VCC output voltage. If the VIDEN signals are set for VCC (01), the VID signals can change and the VCC regulator will respond by changing the output voltage accordingly.

Figure 13 shows how the VCC output voltage can change during normal runtime operation when the VIDEN signals are set to VCC (01). If the VIDEN signals are set to VCC (01), the VCC regulator must monitor the VID signals, latch any changes, and change the output voltage setting accordingly. When the CPU is dynamically changing the VID setting for the VCC regulator during normal operation, it will only change the VID combination by 1 step, which corresponds to a voltage step of ±12.5 mV. During these changes, the VCC regulator must follow the 25 mV/ms slew rate specification.

The VNN regulator differs from the VCC regulator, in that dynamic changes to the VNN regulator output voltage require the VIDEN signals to change to INVALID each time. Figure 14 shows how the VNN output voltage can change during normal runtime operation.

The VIDEN[1:0] pins are active high signals driven by the CPU to indicate if the VID bus is addressing VCC or VNN. They follow the DC Signaling specifications in Table 3 with a reference of 1.05 V ($V_{CCPAOAC}$)

The VID[6:0] pins are active high signals driven by the CPU to indicate the output voltage setting for the VCC and VNN rails. They follow the DC Signaling specifications in Table 3 with a reference of 1.05 V (V_{CCP})

The VID output buffer driver is of the CMOS type. The platform controller hub output driver Impedance is a pull-up (55 Ω +20%/-55%) and pull-down (55 Ω +20%/-55%). Motherboard Impedance is 55 Ω ±15%. Under extreme conditions, there could be ringing that cross the 70/30% threshold, hence the de-bounce requirements. Maximum leakage current on the VID pins is 100 mA.

VID[6:0] for each of the VCC and VNN rails will be latched in an internal register that will be updated with every VID[6:0] pin signaling.

Table 11. VCC and VNN Latch Register Structure and Bit Description

Name	Bits	Description
FSLVCCLATCH (ADDR 0x1C9 - R - Default Value: 0x7F)		
VCCVID	6:0	This register latches an Image of the last VID[6:0] signals for VCC
Reserved	7	Reserved
FSLVNNLATCH (ADDR 0x1CA - R - Default Value: 0x7F)		
VNNVID	6:0	This register latches an Image of the last VID[6:0] signals for VNN
Reserved	7	Reserved

Note that the term Reserved or RSVD is used throughout this document. This nomenclature refers to Reserved Registers that are not for designed customer use. For question regarding these registers, contact Freescale Semiconductor Technical Support.

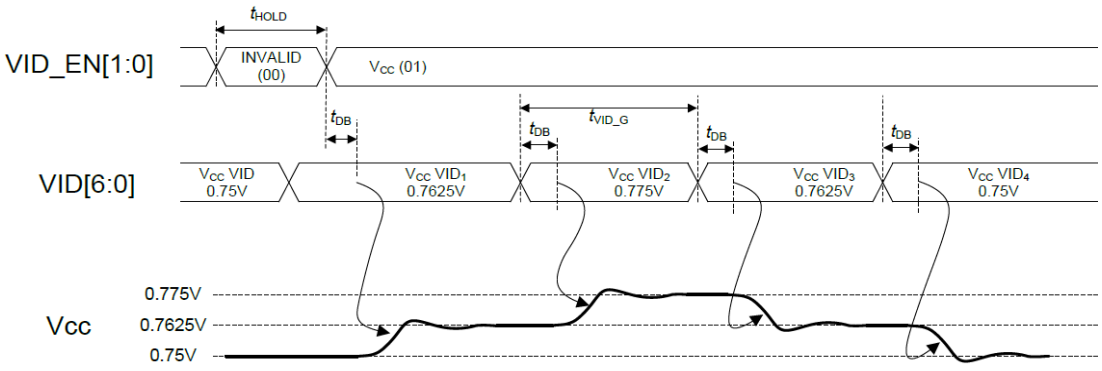


Figure 13. Dynamic VCC Timing Diagram

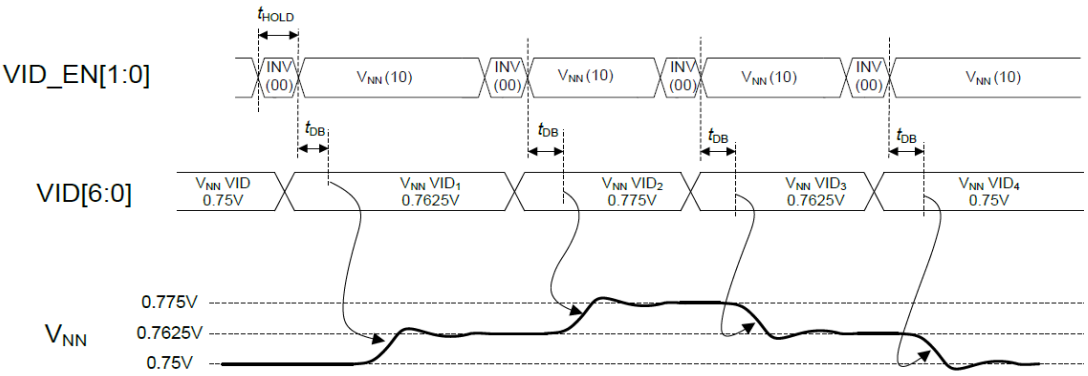


Figure 14. Dynamic VNN Timing Diagram

Figure 15 shows the 7-bit VID codes vs. the output voltage of VCC and VNN.

VID							VID (V)	VID							VID (V)	VID							VID (V)	VID							VID (V)
6	5	4	3	2	1	0		6	5	4	3	2	1	0		6	5	4	3	2	1	0		6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1.2000	0	1	0	0	0	0	0	1.1000	1	0	0	0	0	0	0	0.7000	1	1	0	0	0	0	0	0.3000
0	0	0	0	0	0	1	1.2000	0	1	0	0	0	0	1	1.0875	1	0	0	0	0	0	1	0.6875	1	1	0	0	0	0	1	OFF
0	0	0	0	0	1	0	1.2000	0	1	0	0	0	1	0	1.0750	1	0	0	0	0	1	0	0.6750	1	1	0	0	0	1	0	OFF
0	0	0	0	0	1	1	1.2000	0	1	0	0	0	1	1	1.0625	1	0	0	0	0	1	1	0.6625	1	1	0	0	0	1	1	OFF
0	0	0	0	1	0	0	1.2000	0	1	0	0	1	0	0	1.0500	1	0	0	0	1	0	0	0.6500	1	1	0	0	1	0	0	OFF
0	0	0	0	1	0	1	1.2000	0	1	0	0	1	0	1	1.0375	1	0	0	0	1	0	1	0.6375	1	1	0	0	1	0	1	OFF
0	0	0	0	1	1	0	1.2000	0	1	0	0	1	1	0	1.0250	1	0	0	0	1	1	0	0.6250	1	1	0	0	1	1	0	OFF
0	0	0	0	1	1	1	1.2000	0	1	0	0	1	1	1	1.0125	1	0	0	0	1	1	1	0.6125	1	1	0	0	1	1	1	OFF
0	0	0	1	0	0	0	1.2000	0	1	0	1	0	0	0	1.0000	1	0	0	1	0	0	0	0.6000	1	1	0	1	0	0	0	OFF
0	0	0	1	0	0	1	1.2000	0	1	0	1	0	0	1	0.9875	1	0	0	1	0	0	1	0.5875	1	1	0	1	0	0	1	OFF
0	0	0	1	0	1	0	1.2000	0	1	0	1	0	1	0	0.9750	1	0	0	1	0	1	0	0.5750	1	1	0	1	0	1	0	OFF
0	0	0	1	0	1	1	1.2000	0	1	0	1	0	1	1	0.9625	1	0	0	1	0	1	1	0.5625	1	1	0	1	0	1	1	OFF
0	0	0	1	1	0	0	1.2000	0	1	0	1	1	0	0	0.9500	1	0	0	1	1	0	0	0.5500	1	1	0	1	1	0	0	OFF
0	0	0	1	1	0	1	1.2000	0	1	0	1	1	0	1	0.9375	1	0	0	1	1	0	1	0.5375	1	1	0	1	1	0	1	OFF
0	0	0	1	1	1	0	1.2000	0	1	0	1	1	1	0	0.9250	1	0	0	1	1	1	0	0.5250	1	1	0	1	1	1	0	OFF
0	0	0	1	1	1	1	1.2000	0	1	0	1	1	1	1	0.9125	1	0	0	1	1	1	1	0.5125	1	1	0	1	1	1	1	OFF
0	0	1	0	0	0	0	1.2000	0	1	1	0	0	0	0	0.9000	1	0	1	0	0	0	0	0.5000	1	1	1	0	0	0	0	OFF
0	0	1	0	0	0	1	1.2000	0	1	1	0	0	0	1	0.8875	1	0	1	0	0	0	1	0.4875	1	1	1	0	0	0	1	OFF
0	0	1	0	0	1	0	1.2000	0	1	1	0	0	1	0	0.8750	1	0	1	0	0	1	0	0.4750	1	1	1	0	0	1	0	OFF
0	0	1	0	0	1	1	1.2000	0	1	1	0	0	1	1	0.8625	1	0	1	0	0	1	1	0.4625	1	1	1	0	0	1	1	OFF
0	0	1	0	1	0	0	1.2000	0	1	1	0	1	0	0	0.8500	1	0	1	0	1	0	0	0.4500	1	1	1	0	1	0	0	OFF
0	0	1	0	1	0	1	1.2000	0	1	1	0	1	0	1	0.8375	1	0	1	0	1	0	1	0.4375	1	1	1	0	1	0	1	OFF
0	0	1	0	1	1	0	1.2000	0	1	1	0	1	1	0	0.8250	1	0	1	0	1	1	0	0.4250	1	1	1	0	1	1	0	OFF
0	0	1	0	1	1	1	1.2000	0	1	1	0	1	1	1	0.8125	1	0	1	0	1	1	1	0.4125	1	1	1	0	1	1	1	OFF
0	0	1	1	0	0	0	1.2000	0	1	1	1	0	0	0	0.8000	1	0	1	1	0	0	0	0.4000	1	1	1	1	0	0	0	OFF
0	0	1	1	0	0	1	1.1875	0	1	1	1	0	0	1	0.7875	1	0	1	1	0	0	1	0.3875	1	1	1	1	0	0	1	OFF
0	0	1	1	0	1	0	1.1750	0	1	1	1	0	1	0	0.7750	1	0	1	1	0	1	0	0.3750	1	1	1	1	0	1	0	OFF
0	0	1	1	0	1	1	1.1625	0	1	1	1	0	1	1	0.7625	1	0	1	1	0	1	1	0.3625	1	1	1	1	0	1	1	OFF
0	0	1	1	1	0	0	1.1500	0	1	1	1	1	0	0	0.7500	1	0	1	1	1	0	0	0.3500	1	1	1	1	1	0	0	OFF
0	0	1	1	1	0	1	1.1375	0	1	1	1	1	0	1	0.7375	1	0	1	1	1	0	1	0.3375	1	1	1	1	1	0	1	OFF
0	0	1	1	1	1	0	1.1250	0	1	1	1	1	1	0	0.7250	1	0	1	1	1	1	0	0.3250	1	1	1	1	1	1	0	OFF
0	0	1	1	1	1	1	1.1125	0	1	1	1	1	1	1	0.7125	1	0	1	1	1	1	1	0.3125	1	1	1	1	1	1	1	OFF

Figure 15. 7-Bit VID Code vs. VCC/VNN Output Voltage

As explained previously, the output voltage setting for the VCC and VNN regulators can be set via the VID/VIDEN pins from the CPU, or by programming the VNNLATCH and VCCLATCH registers through the SPI interface via the platform controller hub. Figure 16 shows the relationship between the VID/VIDEN signals, the DVPxVRD bit in the Latch registers, and the VRCOMP output signal. The figure shows V_{CC} as an example, but is also applicable to V_{NN}

The DVPxVRD bit in the VNNLATCH and VCCLATCH registers controls the select input to the multiplexer. If the DVPxVRD bit is set to a '0', the regulator uses the VID/VIDEN pins from the CPU, and if the DVPxVRD bit is set to a '1', the regulator uses the VNNLATCH and VCCLATCH registers to set the output voltage.

When the DVPxVRD bit is set to a '0', any changes to the VNNLATCH and VCCLATCH registers should be ignored. When the DVPxVRD bit is set to a '1', any changes on the VID/VIDEN pins from the CPU should be ignored.

As soon as the DVPxVRD bit is set to a '1', the regulator switches from using the VID/VIDEN pins to using the VCCLATCH register, and the output voltage of the regulator changes to what the VCCLATCH register is set.

Figure 16 shows how the PMIC controls the VRCOMP signal. The PMIC toggles the VRCOMP signal any time the DVPxVRD bit is set to a '1' and the output voltage of the V_{NN} or the V_{CC} regulator changes. If the output voltage of the V_{CC}/V_{NN} regulator changes and the DVPxVRD bit is set to a '0', the VRCOMP signal should not toggle. VRCOMP only toggles for changes to V_{CC} and V_{NN} through the SPI registers.

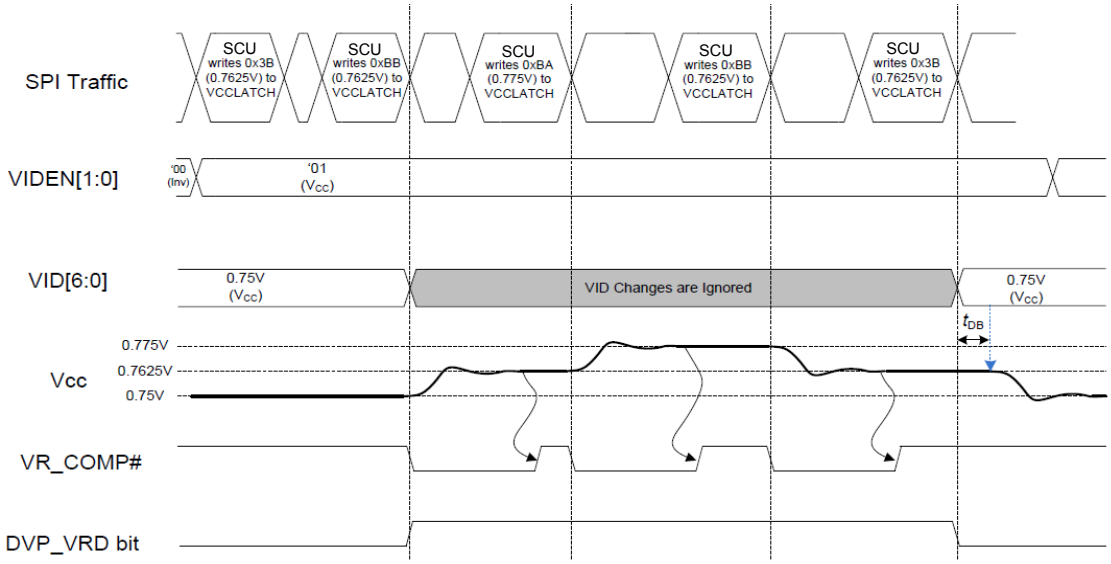


Figure 16. Relationship Between the VID/VIDEN Pins, the DPV1VRD Bit, and VRCOMP Signal

SPECIAL REGISTERS

Vendor ID and Version ID

The Vendor ID and other version details can be read via the Identification bits. These are hard-wired on the chip.

Table 12. Vendor ID Registers Structure and Bits Description

Name	Bits	Description
ID1 (ADDR 0x00 - R - Default Value: 0x28)		
VENDID1	2:0	Chip1 Vendor ID
REV1	5:3	Chip1 Revision ID
Reserved	7:6	Reserved
ID2 (ADDR 0x01 - R - Default Value: 0x00)		
VENDID2	2:0	Chip2 Vendor ID
REV2	5:3	Chip2 Revision ID
Reserved	7:6	Reserved
ID3 (ADDR 0x02 - R - Default Value: 0x00)		
Reserved	7:0	Reserved
ID4 (ADDR 0x03 - R - Default Value: 0x00)		
Reserved	7:0	Reserved

Embedded Memory

There are 24 memory registers of general purpose embedded memory, which are accessible by the processor to store critical data during power down. These registers consist of 8 in the general purpose registers area, and 16 more in the Freescale dedicated register area. General memory registers are called MEMx [MEM1, MEM2… MEM8]. The Freescale dedicated registers are called FSLMEMx [FSLMEM1, FSLMEM2… FSLMEM16]. The data written to these registers is maintained by the coin cell, when the main battery is deeply discharged or removed, and is part of the RTC block. The content of the embedded memory is reset by RTCPORB. The banks can be used for any system need, for bit retention with coin cell backup.

X is from 1 to 8 in Table 13.

Table 13. General Purpose Memory MEMx Register Structure and Bits Description

Register	Name	Bits	Description
MEMx	-	7:0	General Purpose Memory Register x

The rest of the 24 registers reside in the Freescale dedicated register space. X is from 1 to 16 in Table 14.

Table 14. General Purpose Memory FSLMEMx Register Structure and Bits Description

Register	Name	Bits	Description
FSLMEMx	-	7:0	General Purpose Memory Register x

Output Driver Control

Select output pins output drive capability can be programmed for 4 different settings as shows in the following tables. All of the following outputs follow the settings as shown.

Table 15. Output Driver Control Selection

Slope Select		Rise Time (ns)	Fall Time (ns)
0	0	8.4	7.0
0	1	6.2	6.2
1	0	Hi-Z	Hi-Z
1	1	22.3	21.3

Table 16. Output Driver Register Structure and Bit Description

Name	Bits	Description
FSLOUTDRVCNTL1 (ADDR 0x1BF - R/W - Default Value: 0x00)		
PWRGDDRV	1:0	PWRGD Output Pin Driver Capability
VRCOMPBDRV	3:2	VRCOMP Output Pin Driver Capability
PMICINTDRV	5:4	PMICINT Output Pin Driver Capability
RESETBDRV	7:6	RESETB Output Pin Driver Capability
FSLOUTDRVCNTL3 (ADDR 0x1C1 - R/W - Default Value: 0x01)		
SPISDODRV	1:0	MISO Output Pin Driver Capability
RSVD	7:2	Reserved

PLL Control

The following register controls the PLL and the different divider values for different output frequencies.

Table 17. PLL Control Register Structure and Bit Description

Name	Bits	Description
FSLPLLCNTL (ADDR 0x1E4 - R/W - Default Value: 0x1B)		
PLLDIVIDE	2:0	PLL Divide Ratio and Effective VCO Frequency Settings x0 = 112, 3.670 MHz x1 = 116, 3.801 MHz x2 = 120, 3.932 MHz x3 = 124, 4.063 MHz x4 = 128, 4.194 MHz x5 = 132, 4.325 MHz x6 = 136, 4.456 MHz x7 = 140, 4.588 MHz
PLL16MEN	3	16 MHz frequency enable x0 = 16 MHz clock disabled x1 = 16 MHz clock enabled and PLL enabled
PLLEN	4	PLL Enable, even if there is no block requesting a clock x0 = PLL enabled based on device enables only x1 = PLL enabled
Reserved	7:5	Reserved

TEST MODES

Test Mode Configuration

During evaluation and testing, the IC can be configured for normal operation or test mode via the ICTEST pin and other register configurations. Details of Test mode programmability are not documented herein, but should be referenced from other Design for Test documentation.

Test modes are for Freescale use only, and must not be accessed in applications. In test modes, signals are multiplexed on existing functional pins. The ICTEST pin must therefore be tied to ground (for normal operation) at the board level, in product applications

Test mode also disables the thermal protection for high temperature op life testing. A proprietary protocol is included for scan chain test configurations, which reuses the SPI pins.

In-package Trimming

During IC final test, several parameters are trimmed in the package, such as the main bandgap, and other precision analog functions. Trim registers are for Freescale use only and must not be accessed in product applications. Fuse programming circuitry will be blocked during normal and test mode operation.

CLOCK GENERATION AND REAL TIME CLOCK (RTC)

CLOCK GENERATION

A system clock is generated for internal digital circuitry, as well as for external applications utilizing the clock output pins. A crystal oscillator is used for the 32.768 kHz time base and generation of related derivative clocks. If the crystal oscillator is not running (for example, if the crystal is not present), an internal 32 kHz oscillator will be used instead.

Clocking Scheme

The internal 32 kHz oscillator is an integrated backup for the crystal oscillator and provides a 32.768 kHz nominal frequency at 50% accuracy, if running. The internal oscillator only runs if a valid supply is available at the battery or coin cell, and would not be used as long as the crystal oscillator is active. The crystal oscillator continues running, supplied from one of the sources as described previously, until all power is depleted or removed. All control functions will run off the crystal derived frequency, occasionally referred to as the "32 kHz".

At system startup, the 32 kHz clock is driven to the CLK32K output pin, which is SPIVCC referenced. CLK32K is provided as a peripheral clock reference. The driver is enabled by the startup sequencer. Additionally, a SPI bit M32KCLK bit is provided for direct SPI control. The M32KCLK bit defaults to 0 to enable the driver and resets on the RTCPORB to ensure the buffer is activated at the first power up and configured as desired, for subsequent power ups.

The drive strength of the output drivers is programmable with CLK32KDRV[1:0] (master control bits that affect the drive strength of CLK32K), see FSLOUTDRVCNTL2 Register in Table 16.

If a switch over occurs between the two clock sources (such as when the crystal oscillator is starting up), it will occur during the active low phase of both clocks, to avoid clocking glitches. A status bit, OSCSTP, is available to indicate to the processor which clock is currently selected: OSCSTP=1 when the internal RC is used, and OSCSTP=0 if the XTAL source is used.

Oscillator Specifications

The 32 kHz crystal oscillator has been optimized for use in conjunction with the Abracon™ ABS07-32.768KHZ-T, or equivalent.

The electrical characteristics of the 32 kHz Crystal oscillators are given in the Oscillator section on Table 3 and Table 4, taking into account the crystal characteristics noted previously. The oscillator accuracy depends largely on the temperature characteristics of the used crystal. Application circuits can be optimized for required accuracy by adapting the external crystal oscillator network (via component accuracy and/or tuning). Additionally, a clock calibration system is provided to adjust the 32.768 cycle counter that generates the 1.0 Hz timer and RTC registers; see Real Time Clock (RTC) for more detail.

REAL TIME CLOCK (RTC)

The RTC block provides a real-time clock with time-of-day, year, month, and date, as well as daily alarm capabilities. The real-time clock will use the 32.768 kHz oscillator as its input clock. The real-time clock will be powered by the coin cell backup battery as a last resort, if no other power source is available (Battery or USB/Wall plug). The register set is compatible with the Motorola™ MC146818 RTC device.

Overview

The RTC module uses a 15-bit counter to generate a 1.0 Hz clock for timekeeping. The seven time and calendar registers keep track of seconds, minutes, hours, day-of-week, day-of-month, month, and year. The three seconds, minutes, and hours alarm registers can be used to generate time-of-day alarm interrupts.

The RTC time, alarm, and calendar values can be represented in 8-bit binary or BCD format. The hours and hours alarm values can be represented in 24 hour or 12 hour format, with AM/PM in the 12 hour mode. RTC control register B allows for software configurable clock formatting and interrupt masking. Control registers A, C, and D, report software testable RTC status, including interrupt flags, update-in-progress, and valid-RAM-time.

The RTC resets when the RTCPORB signal is driven low. The clock and calendar registers will be initialized to 00:00:00, Sunday, January 1, 2000.

Features

The RTC module includes the following features:

- Counts seconds, minutes, and hours of the day
- Counts days of the week, date, month, and year
- Binary or BCD representation of time, calendar, and alarm
- 12 or 24 hour clock with AM and PM in 12 hour mode
- Automatic leap year compensation
- Automatic end of month recognition
- 15 bytes of clock, calendar, RTC control, and coin cell registers
- Two interrupts are separately software maskable and testable
- Time-of-day Alarm
- End-of-clock update cycle interrupt
- 15-bit counter to generate 1.0 Hz RTC clock
- Software testable Valid-ram-and-time status bit indicates data integrity

MODES OF OPERATION

Normal mode

In Normal mode, the RTC module updates time and calendar registers using the internal 1.0 Hz RTC clock. Once per second, the alarm registers are compared to the current time, and if enabled, an alarm interrupt will occur when the alarm time matches the current time. During normal operation, all 14 bytes of RTC and coin cell battery registers can be read through the SPI interface. Control register B may be updated to enable End-of-clock Update interrupts, alarm interrupts, or to put the RTC in Set mode.

The coin cell charger register is available for R/W in normal mode.

Coin Cell mode

When the application is powered down, the RTC will continue to keep track of time using power provided by the coin cell battery. Since the system SPI will be powered down during this time, there is no read or write access to the RTC registers in Coin Cell mode.

Set mode

In Set mode, the clock and calendar updates are suspended, and the software may update the time, calendar, and alarm registers. The time and calendar formats must match the formats specified by the DM and 12/24 format bits in RTC register B. When the format bits are modified, all 14 time, calendar, and alarm registers must be updated in the specified format.

Scan/Test mode

Internal Test mode not available for the end application.

Setting the Time, Calendar, and Alarm

Before initializing the internal registers, the Set bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. Select the RTC data format by writing the appropriate values to the DM and 24/12 bits in Register B. This can all be done simultaneously with one SPI write to register B.

Next, the program should initialize all 10 time, calendar, and alarm locations, in the format specified by Register B (binary or BCD, 12 or 24 hour). All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. Both the alarm hours, and the hours bytes must use the same hours format, either 12 or 24.

The Set bit may now be cleared to allow updates. Once initialized, the real-time clock makes all updates in the selected data mode. The data mode (DM) cannot be changed without re-initializing the 10 data bytes.

The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. When the 12 hour format is selected the high order bit of the hour bytes represents PM when it is a "1". The 24/12 bit cannot be changed without re-initializing the hour and alarm-hour locations.

Table 18 shows the binary and BCD formats of the 10 time, calendar, and alarm locations.

Table 18. Time, Calendar, and Alarm Data Modes

Address location	Function	Decimal Range	Range		Example [17]	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0x10	Seconds	0-59	$00-$3B	$00-$59	15	21
0x11	Seconds Alarm	0-59	$00-$3B	$00-$59	15	21
0x12	Minutes	0-59	$00-$3B	$00-$59	3A	58
0x13	Minutes Alarm	0-59	$00-$3B	$00-$59	3A	58
0x14	Hours (12 Hour Mode) (24 Hour Mode)	 1-12 0-23	 $01-$0C(AM) / $81-$92(PM) $00-$17	 $01-$12(AM) / $81-$92(PM) $00-$23	0B	11
0x15	Hours Alarm (12 Hour Mode) (24 Hour Mode)	 1-12 0-23	 $01-$0C(AM) / $81-$92(PM) $00-$17	 $01-$12(AM) / $81-$92(PM) $00-$23	0B	11
0x16	Day of the Week Sunday=1	1-7	$01-$07	$01-$07	05	05
0x17	Date of the Month	1-31	$01-$1F	$01-$31	0F	15
0x18	Month	1-12	$01-$0C	$01-$12	02	02
0x19	Year	0-99	$00-$63	$00-$99	08	08

Notes

17. Example: 11:58:21 Thursday 15 February 2008 (time is AM)

Reading the Time, Calendar, and Alarm

Under normal operation, the current time and date may be read by accessing the RTC registers through the system SPI. Since the alarm is only updated by a SPI write instruction, the three alarm registers may be read at any time and will always be defined.

The 900844 SPI will run at a minimum of 12.5 MHz. Each individual SPI read transaction requires 25 cycles (less for burst-read). The RTC contains seven timekeeping registers to keep track of seconds, minutes, hours, day-of-week, day-of-month, month, and year. If the SPI is clocked at the slowest frequency, and the RTC is read using individual (not burst) SPI read commands, the following equation gives the maximum amount of time it takes the processor to read a complete date and time (assuming the reads are done sequentially, and uninterrupted): (25 * 7) / (12.5 MHz) = 14 μs.

This equation shows that a program which randomly accesses the time and date information will find the data in transition statistically 14 times per million attempts. If a clock update occurs during the time it takes to read all seven timekeeping registers, the values read may be inconsistent. In other words, if the program starts to read the seven date/time registers and an RTC update occurs, the data collected may be in transition. In this event, it is possible to read transition data in one of the registers, resulting in undefined output. It is more likely that the registers read after the update would be incremented (by one second), and the registers read before the update would not.

The time, calendar, and alarm bytes are always accessible by the processor program. Once per second, the seven bytes are advanced by one second and checked for an alarm condition. If any of the seven bytes are read at this time, the data outputs should be considered undefined. Similarly, all seven bytes should be read between updates to get a consistent time and date. Reading some of the bytes before an update and some after, may result in an erroneous output. The Update Cycle section explains how to accommodate the update cycle in the processor program.

Update Cycle

The RTC module executes an update cycle once per second, assuming one of the proper time bases is in place, and the SET bit in Register B is clear. The SET bit in the “1” state permits the program to initialize the time and calendar bytes, by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the Seconds byte, check for overflow, increment the Minutes byte when appropriate, and so forth, up through the month and year bytes. The update cycle also compares each alarm byte with the corresponding time byte, and issues an alarm if a match is present in all three positions.

Two methods of avoiding undefined output during updates are usable by the program. In discussing the two methods, it is assumed that at random points, user programs are able to call a subroutine to obtain the time of day.

The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle, which indicates that over 999 ms are available to read valid time and date information. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A, to determine if the update cycle is in progress. The UIP bit will pulse once per second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 3,640 attempts. After the UIP bit goes high, the update cycle begins 244.1 μs later. Therefore, if a low is read on the UIP bit, the user has at least 244.1 μs before the time/calendar data will be changed. If a “1” is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines which would cause the time needed to read valid time/calendar data to exceed 244.1 μs.

The RTC uses seven synchronous counters to increment the time and calendar values. All seven timekeeping registers are clocked by the same internal 1.0 Hz clock, so updates occur simultaneously, even during rollover. After the counters are incremented, the current time is compared to the time-of-day alarm registers 30.5 μs later, and if they match, the AF bit in register C will be set.

The Update-cycle begins when the clock and calendar registers are incremented, and ends when the alarm comparison is complete. During this 30.5 μs update cycle, the time, calendar, and alarm bytes are fully accessible by the processor program. If the processor reads these locations during an update, the transitional output may be undefined. The update in progress (UIP) status bit is set 244.1 μs before this interval, and is cleared when the update cycle completes.

Interrupts

The RTC includes two separate, fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at a rate of once per day. The update-ended interrupt may be used to indicate to the program that an update cycle is completed.

The processor program selects which interrupts, if any, it wishes to receive. Two bits in Register B enable the two interrupts. Writing a “1” to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A “0” in the interrupt-enable bit, prohibits the IRQF bit from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the IRQF bit is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such earlier initiated interrupts before enabling new interrupts.

When an interrupt event occurs, a flag bit is set to a “1” in Register C. Each of the two interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The interrupt flag bit becomes a status bit, which the software interrogates when it wishes. When the software detects the flag is set, it is an indication to the software an interrupt event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C, so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One or two flag bits may be found to be set when Register C is used. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the IRQF bit is asserted high. IRQF is asserted as long as at least one of the two interrupt sources has its flag and enable bits both set.

The processor program can determine that the RTC initiated the interrupt by reading Register C. A “1” in bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the part. The act of reading Register C clears all the then active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte, which have the corresponding interrupt mask bits set and service each interrupt which is set. Again, more than one interrupt flag bit may be set.

ALARM INTERRUPT

The three alarm bytes may be used to generate a daily alarm interrupt. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day, if the alarm enable bit is high.

Update-Ended Interrupt

If enabled, an interrupt occurs after every update cycle which indicates that there is over 999 ms available to read valid time and date information.

RTC Timer Calibration

By default, the calibration circuit is off and clock accuracy is limited to the performance of the 32.768 kHz crystal input. For clock accuracy beyond the limits of the crystal oscillator, a calibration circuit is included. The processor can use a high-frequency clock to sample the 32.768 kHz output to determine if it is fast or slow, and calculate an adjustment value. The adjustment algorithm has a resolution of ±477 nanoseconds-per-second average adjustment, which equates to a time accuracy of approximately 1.2 seconds per month.

Calibration can be turned on by setting the RTC ADJ bit of the ADJ register. A "0" in the ADJ bit turns calibration off. The Sign bit in the Trim register determines if periodic adjustments are made to speed up or slow down the clock.

When calibration is enabled, the Trim register is used to grow or shrink the average 1.0 Hz clock period. By default, one second is defined as 32,768 periods of the CLK32K input pin. Each period of the input clock is approximately 30.5 μs. By occasionally adding (or subtracting) one extra cycle per second, the average second can be adjusted. If SIGN is high (subtract one), occasional seconds will be trimmed to 32,767 cycles. If SIGN is low (add one), occasional seconds will be trimmed to 32,769 cycles.

The 6-bit TRIMVAL in the Trim register represents the number of seconds to adjust out of every 64 seconds, and can range from 0-63. For example, TRIMVAL = 0x08 then 8 seconds out of every 64 will be adjusted up or down, according to the SIGN bit.

CLOCK GENERATION AND REAL TIME CLOCK (RTC) REGISTERS AND BITS DESCRIPTION

Table 19. RTC Date/Time Configuration Register Structure and Bits Description

Name	Bits	Description
RTCS (ADDR 0x10 - R/W - Default Value: 0x00)		
SEC	6:0	Seconds Counter Register
Reserved	7	Reserved
RTCSA (ADDR 0x11 - R/W - Default Value: 0x00)		
SECALARM	6:0	Seconds Alarm Setting Register
Reserved	7	Reserved
RTCM1 (ADDR 0x12 -R/W - Default Value: 0x00)		
MIN	6:0	Minutes Counter Register
Reserved	7	Reserved
RTCMA (ADDR 0x13 - R/W - Default Value: 0x00)		
MINALARM	6:0	Minutes Alarm Setting Register
Reserved	7	Reserved
RTCH (ADDR 0x14 - R/W - Default Value: 0x00)		
HRS	5:0	Hours Counter Register
Reserved	6	Fixed to 0
PA-H	7	AM/PM Indication, Only active during 12 Hr. mode x0 = AM x1 = PM

Table 19. RTC Date/Time Configuration Register Structure and Bits Description

Name	Bits	Description
RTCHA (ADDR 0x15 - R/W - Default value: 0x00)		
HRSALARM	5:0	Hours Alarm Setting Register
Reserved	6	Reserved (Fixed to 0)
PA-HA	7	AM/PM Alarm Setting, Only active during 12 Hr. mode x0 = AM x1 = PM
RTCDW (ADDR 0x16 - R/W - Default Value: 0x01)		
DOW	2:0	Day of Week counter register: 1= Sunday... 7= Saturday
Reserved	7:3	Reserved
RTCDM (ADDR 0x17 - R/W - Default Value: 0x01)		
DOM	5:0	Day Of Month Counter Register
Reserved	7:6	Reserved
RTCM2 (ADDR 0x18 - R/W - Default Value: 0x01)		
MONTH	4:0	Months Counter Register
Reserved	6:5	Reserved
19/20	7	THIS BIT IS NOT SUPPORTED Always Reads 0 (treated as a reserved bit)
RTCY (ADDR 0x19 - R/W - Default Value: 0x00)		
YEAR	7:0	Year Counter Register. Note: Values range from 0 to 99

Table 20. RTC Control Registers Structure and Bit Description

Name	Bits	Description
RTCA (ADDR 0x1A - R - Default Value: 0x20)		
Reserved	6:0	Fixed to 010000
UIP	7	This is the Update In Progress (UIP) bit used as a status flag x0 = Update cycle not in progress x1 = Update cycle is in progress or will begin soon
RTCB (ADDR 0x1B - R/W - Default Value: 0x02)		
Reserved	0	Fixed to 0
HRMODE	1	Hour Format Control x0 = 12 Hour Mode x1 = 24 Hour Mode
DM	2	Data Mode for Time and Calendar Updates x0 = Binary-Coded-Decimal (BCD) x1 = Binary
Reserved	3	Fixed to 0
UIE	4	Update-Ended Interrupt Enable x0 = Update-End (UF) bit in Register C is not permitted to assert the interrupt request flag (IRQF) in Register C x1 = Update-End (UF) bit in Register C is permitted to assert the interrupt request flag (IRQF) in Register C

Table 20. RTC Control Registers Structure and Bit Description

Name	Bits	Description
AIE	5	Alarm Interrupt Enable x0 = Alarm flag (AF) bit in Register C is not permitted to assert the interrupt request flag (IRQF) in Register C x1 = Alarm flag (AF) bit in Register C is permitted to assert the interrupt request flag (IRQF) in Register C
Reserved	6	Fixed to 0
SET	7	Set mode enable bit for the program to initialize the time and calendar bytes x0 = The update cycle functions normally by advancing the counts once-per-second. x1 = Any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing.
RTCC (ADDR 0x1C - R - Default Value: 0x00)		
Reserved	3:0	Reserved
UF	4	Update-Ended Interrupt Flag. Set after each update cycle. X0 = UIE bit will not effect IRQF state x1 = When UIE bit goes high, the IRQF bit goes high
AF	5	Alarm Interrupt Flag. Indicates that the current time has matched the alarm time. X0 = AIE bit will not effect IRQF state x1 = When AIE bit goes high, the IRQF bit goes high
Reserved	6	Fixed to 0
IRQF	7	Interrupt Request Flag. IRQF = (AF&AIE) + (UF&UIE) The interrupt request flag (IRQF) is set to a “1” when one or more of the following are true: AF = AIE = “1” UF = UIE = “1” x0 = Above Equation is not true x1 = Above Equation is true
RTCD (ADDR 0x1D - R - Default Value: 0x00)		
Reserved	6:0	Fixed to 000000
VRT	7	The Valid RAM and Time (VRT) bit indicates the condition of the contents of the RTC time and calendar registers. A "0" appears in the VRT bit when the RTC registers have been reset. The processor program should set the VRT bit after the time and calendar are initialized to indicate that the time and calendar are valid. The VRT bit can only be set by reading register D.
RTCE (ADDR 0x1E - R/W - Default Value: 0x05)		
OSCSTP	0	Oscillator (32 kHz) Clock Stop Flag x0 = XTAL Oscillator x1 = Internal RC Oscillator
BKDET	1	Coin Cell Backup Voltage Status x0 = No change x1 = Coin Cell below "low-voltage" threshold When this bit is set to 1, the SW takes corresponding action for a coin cell well below the operating voltage, and clears the BKDET to get ready for the next event.
POR	2	RTC Reset Flag x0 = No reset was detected x1 = POR occurred
SCRATCH	7:3	These bits shall not exert any control over the operation of the RTC, and are intended to be used as scratch pad registers by the system controller. Their contents are erased on RTCPORB.

Table 20. RTC Control Registers Structure and Bit Description

Name	Bits	Description
ADJ (ADDR 0x1F - R/W - Default Value: 0x00)		
ADJ	0	RTC Trim Enable Signal x0 = Do Not Trim x1 = Trim
Reserved	7:1	Fixed to 0000000
TRIM (ADDR 0x20 - R/W - Default Value: 0x00)		
TRIMVAL	5:0	6-Bit Trim Control This is a number from 0 to 63 that represents the number of seconds to adjust out of every 64 seconds
SIGN	6	RTC Calibration Sign Bit x0 = Add x1 = Subtract
Reserved	7	Fixed to 0
CLKOUT (ADDR 0x21 - R/W - Default Value: 0x00)		
M32KCLK	0	32 kHz clock output mask x0 = 32 kHz clock output enabled x1 = 32 kHz clock output masked (disabled)
Reserved	7:1	Fixed to 0000000

POWER STATES AND CONTROL

OVERVIEW

There are three different power states in the operation of the 900844 PMIC:

1. No Power State: No input voltage is available at the main supply or the coin cell battery input.
2. Active State: The PMIC has enough power to supply the system.
3. RTC State: The PMIC has enough power to support the RTC operation and the Keep Alive Registers, but not enough to power the rest of the system.

The power state of the PMIC at any given time is determined by the conditions of the following inputs:

1. VPWR: This is the main supply to the system. It must be externally connected to VBAT.
2. VBAT: This is the main supply voltage sensing input.
3. VCOINCELL: This is the backup input voltage, typically from a rechargeable coin cell battery.

INTERNAL SUPPLIES POWER TREE

Figure 17 shows the 900844 internal power tree.

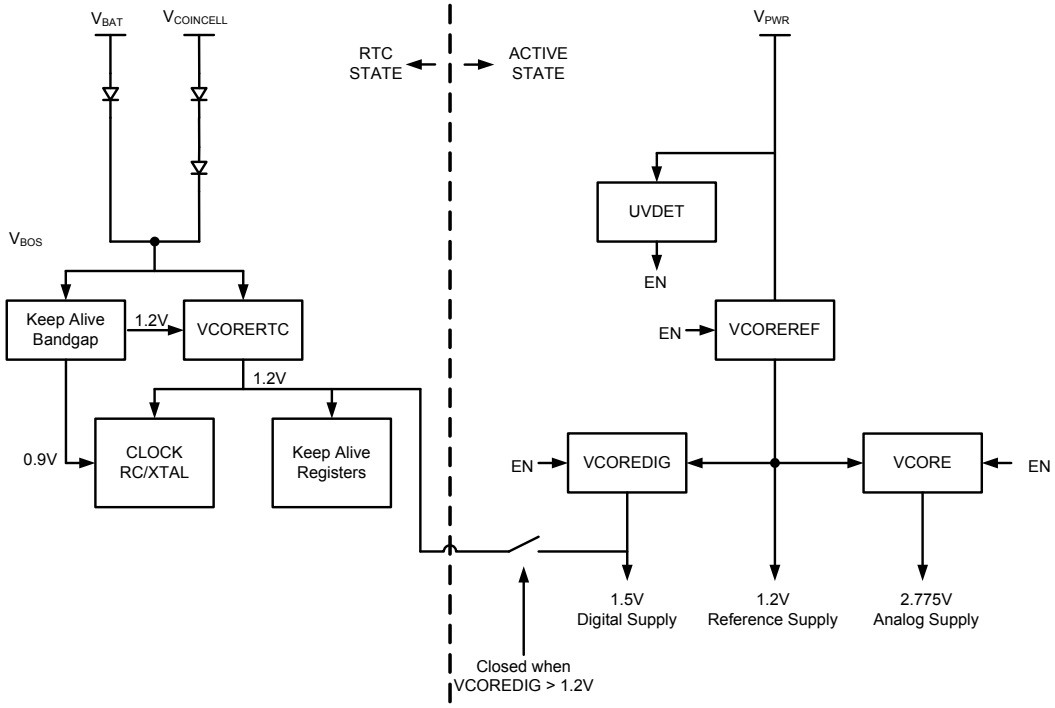


Figure 17. 900844 Internal Power Tree Block Diagram

As part of the turn on sequence, the 900844 enables a set of internal supplies that provide power to the rest of the circuitry:

1. $V_{CORE REF}$: This is the main bandgap and reference voltage for all internal circuitries.
2. V_{CORE}: This is the supply for the internal analog circuitry.
3. $V_{COREDIG}$: This is the supply for the internal digital circuitry.

Table 21 summarizes the voltage references on the 900844.

Table 21. 900844 Internal Power Supply Summary

Reference	Parameter	Target
VCOREREF (Bandgap & Regulators Reference)	Output Voltage	1.2 V
	Bypass Capacitor	100 nF typ.
VCOREDIG (Digital Core Supply)	Output Voltage	1.5 V
	Bypass Capacitor	2.2 μF typ.
VCORE (Analog Core Supply)	Output Voltage	2.775 V
	Bypass Capacitor	2.2 μF typ.

There is an internal node called the Best of Supply node (VBOS), which supplies the Real Time Clock and the Keep Alive Registers. This ensures that power to these critical circuits is maintained for maximum life. VBOS represents the highest of the VBAT and VCOINCELL input voltages. When VCOREDIG is > 1.2 V, an internal switch is closed, and the circuitry that was powered from VBOS is now powered from VCOREDIG.

POWER STATES

Figure 18 shows the flow of power, the different power states, and the conditions necessary to transition between the different states. This diagram serves as the basis for the description in the remainder of this section.

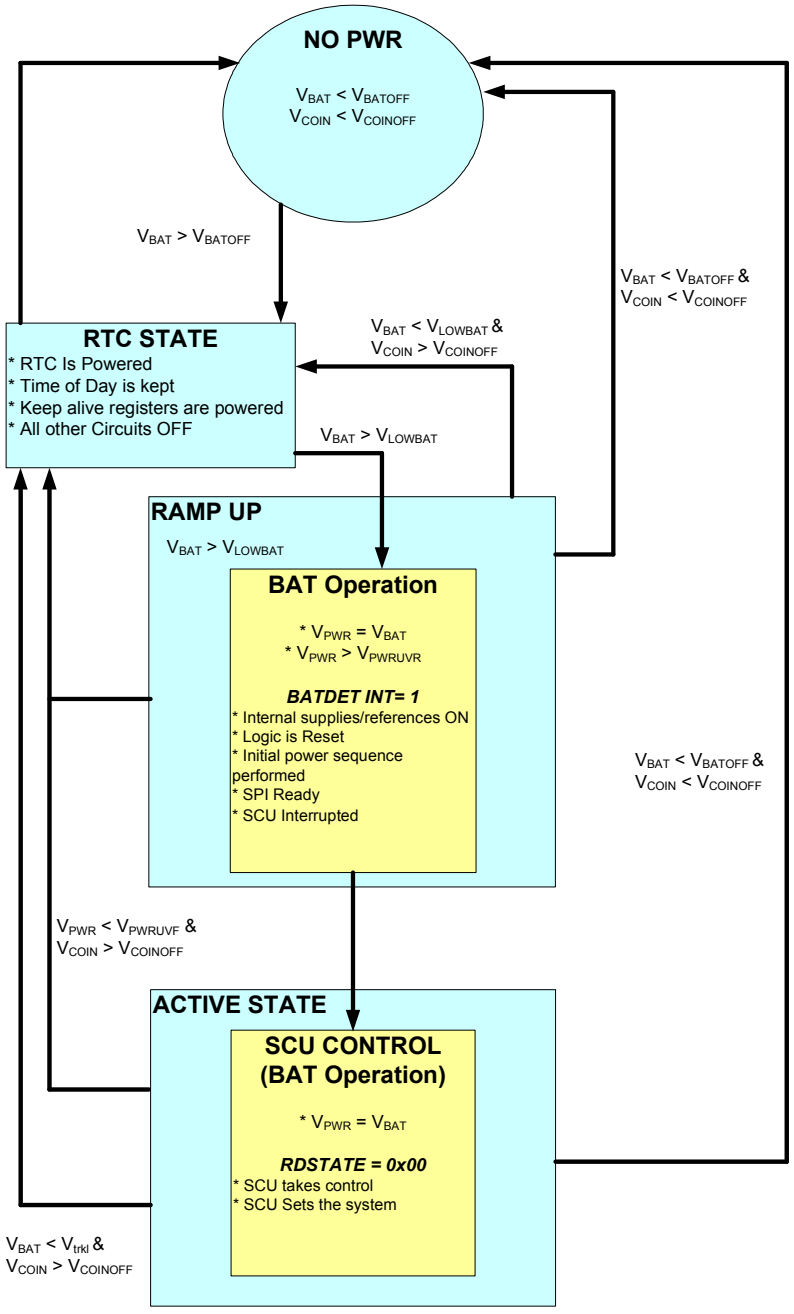


Figure 18. 900844 Power States

No Power State

In this state, every source of power has been removed or is fully depleted:

- $V_{BAT} < V_{BATOFF}$: The input voltage is under the cutoff threshold, indicating that the main supply has been removed, or has been isolated by its own protection circuitry, and
- $V_{COIN} < V_{COINOFF}$: The coin cell backup battery has been removed or has been isolated by the 900844 coin cell discharge prevention circuitry (see Coin Cell Battery Backup/Charger)

The 900844 has lost any source of power to maintain the RTC and its keep alive registers, and all the internal circuits power down and time of day cannot be kept.

RTC State

In this state, the 900844 has limited power. The VBOS is available and powers the RTC and the Keep Alive Registers. However, the system does not have enough power to enter the active state:

- V_{COIN} > COINOFF: The backup battery is above the coin cell disconnect threshold.
- $V_{PWR} < V_{PWRUVF}$: The system voltage is less than the under-voltage falling threshold.

During this mode, all voltage regulators are off and cannot be powered. The RTC is operating (Real Time Clock (RTC)), and the time of day and all keep alive registers are maintained.

Active State

In this state, the 900844 internal circuits are fully powered:

- $V_{PWR} > V_{PWRUVR}$: The system voltage, V_{PWR}, is available and valid, and
- $V_{BAT} > V_{LOWBAT}$: The main input voltage is above a low battery condition.

All features of the 900844 are either operating or can be enabled, which is under the control of the System Control Unit (SCU) within the Platform Controller Hub (PCH).

Power State Transitions

When power is applied to the 900844 for the first time, it goes from the No Power state into the Active state, with a brief transition through the RTC state. The RTC and the Keep Alive Registers are powered, and the time of day is initialized to a factory set value (See Real Time Clock (RTC)).

When V_{PWR} crosses the under-voltage rising detection threshold (V_{PWRUVR}), the internal supplies power on, the logic is reset, the initial power sequence is performed, SPI communication is enabled, and an interrupt to the Platform Controller Hub is generated. The PMIC enters the Active state and the system is under control of the SCU.

If V_{PWR} crosses the under-voltage falling detection threshold (V_{PWRUVF}), and at least one of the VBOS supplies (V_{COIN} or V_{BAT}) is still valid, the 900844 enters the RTC state. Only the RTC is operating and the RTC and Keep Alive registers are maintained.

If the 900844 is in the RTC state, full operation is obtained when the voltage at VPWR crosses again the under-voltage rising detection threshold (VPWRUVR).

TURN ON EVENTS

A turn on event occurs when a valid input voltage is present at VBAT ($V_{BAT} > V_{LOWBAT}$), and the system voltage goes above the under-voltage rising threshold ($V_{PWR} > V_{PWRUVR}$). Otherwise, the 900844 is in the RTC or No Power State.

When a turn on event occurs, the BATDET interrupt bit is set. Reference Interrupt Controller for more information on the different system interrupts.

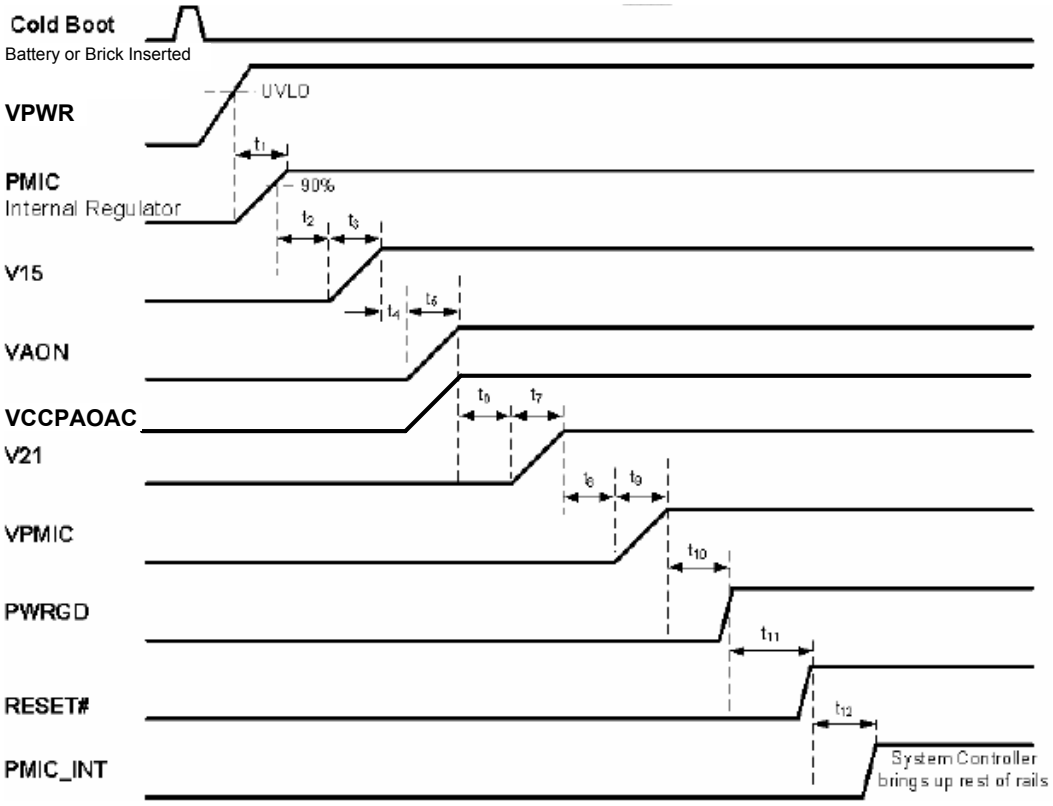


Figure 19. 900844 Initial Power Up Sequence

Initial Power Up Sequence

Figure 19 shows the 900844 initial power up sequence:

1. A valid system voltage is applied
2. V_{PWR} ramps up
3. The 900844 internal circuits are powered
4. The 900844 turns on a minimal set of voltage rails as outlined in Figure 19
5. SPI communication is ready
6. PMICINT pin is asserted
7. The system controller unit (SCU) reads the 900844 interrupt flag register (over SPI) to see why the 900844 interrupted the platform controller hub.
8. The SCU decides whether to boot the rest of the system, or just run SCU code to manage various functions.
9. If the SCU decides to power up system, then CPU (central processing unit) drives VNN VID, VIDEN[1:0] = 10 to the 900844 and BSEL to the Platform controller hub.
10. The 900844 drives CPU selected voltage for VNN
11. There will be no explicit signaling from the 900844 that indicates that the VNN ramp has been complete.
12. VIDEN[1:0] is driven to 00 to avoid it switching from 10 to 01 directly.
13. The CPU drives the VCC boot VID on the VID pins. The VIDEN[1:0] = 1 enables, only after HPLL has locked.
14. X86 Instruction Executions starts.

Table 22. 900844 Initial Power Up Timing

Parameter	Description	Min	Typ	Max
t_1	PMIC internal regulator Ramp-up	-	-	100 µs
t_2	V15 turn on delay	18 ms	-	550 ms
t_3	V15 Ramp-up	-	-	10 µs
t_4	VAON/VCCPAOAC turn on delay	0 µs	-	31 µs
t_5	VAON/VCCPAOAC ramp-up	-	-	700 µs

Table 22. 900844 Initial Power Up Timing

Parameter	Description	Min	Typ	Max
t_6	V21 turn on delay	0 µs	-	31 µs
t_7	V21 ramp-up	-	-	100 µs
t_8	VPMIC turn on delay	0 µs	-	31 µs
t_9	VPMIC ramp-up	-	-	700 µs
t_{10}	PWRGD delay	70 ms	-	90 ms
t_{11}	RESET delay	1.0 µs	-	31 µs
t_{12}	PMICINT delay	31 µs	-	124 µs

TURN OFF EVENTS

The following conditions cause the 900844 to power off the system, including the SCU, but the 900844 internal circuitry and logic are still active:

- PWRBTN pressed for more than 5 seconds. See Power Button Functionality (PWRBTN).
- The 900844 junction temperature is above the thermal shutdown threshold. See Thermal Management for more details.
- A THERMTRIPB assertion. See THERMTRIPB Pin for more details.

Power Button Functionality (PWRBTN)

The Power Button is pulled up internally through a 132 k resistor to the $V_{COREDIG}$ output voltage node. See Figure 20 for more details.

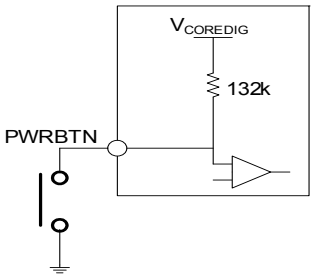


Figure 20. PWRBTN Circuit Diagram

Figure 21 describes the functionality of the PWRBTN

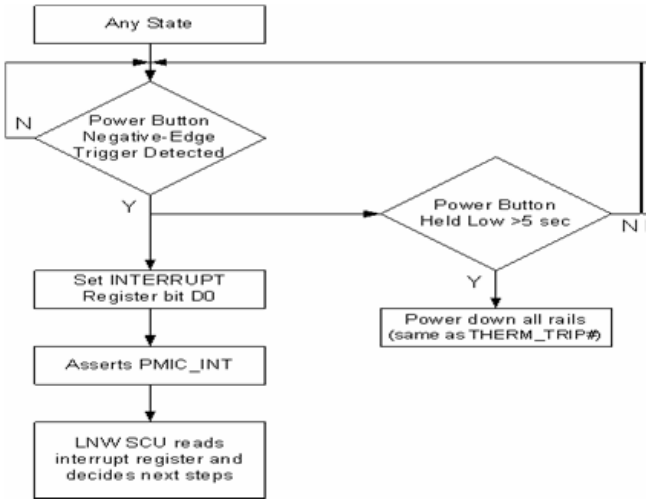


Figure 21. PWRBTN Function Flow Diagram

DETECTION THRESHOLDS

Table 23 summarizes the various detection thresholds between the different states:

Table 23. Power States Detection Thresholds

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Cutoff Threshold	V_{BATOFF}	2.2	-	2.4	V
Coin Cell Disconnect Threshold	$V_{COINOFF}$	1.8	-	2.0	V
Low input voltage Threshold	V_{LOWBAT}	3.2	-	-	V
Valid input voltage Threshold	V_{TRKL}	-	3.0	-	V
VPWR Rising Under-voltage Threshold	V_{PWRUVR}	-	3.1	-	V
VPWR Falling Under-voltage Threshold	V_{PWRUVF}	-	2.55	-	V

POWER SUPPLIES

POWER MAP

Figure 22 is a power map of Freescale's power management solution for Ultra-mobile platforms for Netbooks/ and tablet PC:

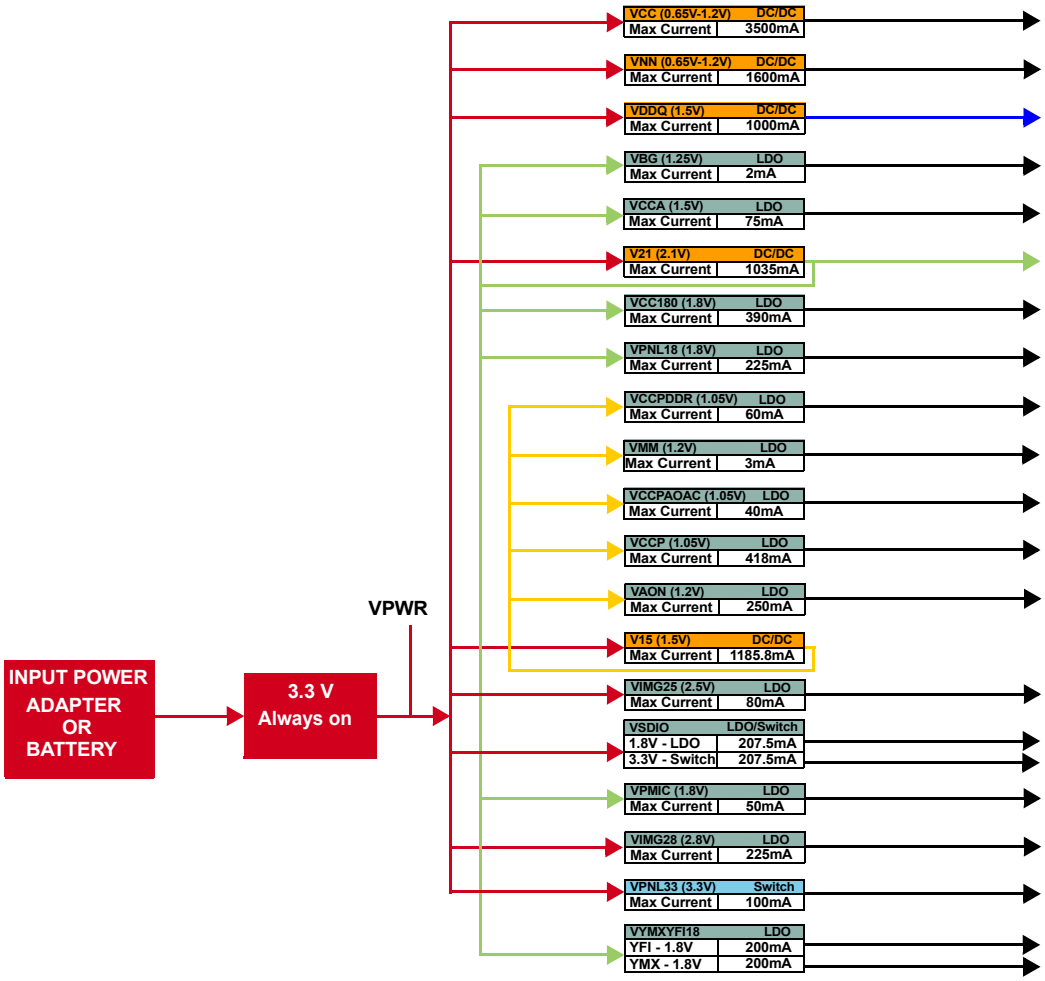


Figure 22. 900844 Power Map

DC/DC POWER SUPPLIES

Freescale's power management solution for the Ultra-mobile platform for Netbook/Tablets and Slates, includes 5 DC/DC switching regulators integrated on the 900844 PMIC. the five DC-DC regulators are Buck converters, and these can be set to work in the following operation modes:

Buck converters Operation Modes Selections (VCC, VNN, VDDQ, V21, V15)

- OFF - The regulator is switched off and the output voltage is discharged.
- PFM - The regulator is switched on and set to PFM mode operation. In this mode, the regulator is always running in PFM mode. Useful at light loads for optimized efficiency.
- Automatic Pulse Skip - The regulator is switched on and set to Automatic Pulse Skipping. In this mode, the regulator moves automatically between pulse skipping and full PWM mode depending on load conditions.
- PWM - The regulator is switched on and set to PWM mode. In this mode, the regulator is always in full PWM mode operation regardless of load conditions.
- TEST/TRIM - This is not a functional mode, thus requiring certain steps to prevent unintentional activation of this mode. During this mode, the device performs measurements and trimming.

DC-DC Power Supply Summary Table

Table 24 provides a summary of all DC/DC regulators on the 900844.

Table 24. 900844 DC-DC power supplies.

Regulator	Typ. Voltage	Max Continuous Current	Description
VCC	0.3 - 1.2 V	3.5 A	1.0 MHz synchronous Buck converter with external switching MOSFETs. Internally compensated. VID is controlled using a shared 7-bit bus for voltage coding and 2 VID enable signals for VCC or VNN selection.
VNN	0.3 - 1.2 V	1.6 A	1.0 MHz synchronous Buck converter with external switching MOSFETs. Internally compensated. VID is controlled using a shared 7-bit bus for voltage coding and 2 VID enable signals for VCC or VNN selection.
VDDQ	1.8 V/1.5 V	1.3 A	4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.
V21	2.1 V	1.0 A	4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.
V15	1.5 V	1.5 A	4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.

Note that all of the DC/DC regulators specify an extended input voltage range beyond the 3.0 to 4.4 V applications range. Below this, extended range functionality is maintained, but parametric performance could be compromised.

VCC

This is a VID controlled single-phase 1.0 MHz 2-switch synchronous Buck PWM voltage mode control DC/DC regulator, designed to power high performance CPUs. VCC uses external MOSFETs, P-Ch high side and N-Ch low side.

VCC includes support for VID active voltage positioning requirements. A 7-bit DAC reads the VID input signals and sets the output voltage level. The output voltage has a range of 0.3 to 1.2 V. The programming step size is 12.5 mV. Values will be read in real time and will be stored in internal registers not accessible to the system host. Reference VIDEN[1:0] & VID[6:0] Pins for more details.

The same VID input signals are shared between VCC and VNN, where a latch signal for each regulator decides which regulator takes control of the VID input signals.

The DAC value represents the output voltage value. The output voltage node is connected directly to the inverting input of the error amplifier that uses the DAC output as its reference, unity gain configuration. Using this configuration with internal compensation eliminates the need for the feedback and compensation network, which saves board space and cost. The DAC/ output voltage slew rate is internally set 25 mV/µs to minimize transient currents and audible noise.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The above selection is optimized to maximum battery life based on load conditions.

VCC will be discharged every time the regulator is shutting down.

The output current will be sensed using an intelligent implementation of the DCR sensing method using internal sensing circuitry, which eliminates the need for an external RC filter network in parallel with the output inductor and its winding resistance.

DCR sensing theory is that if the impedance of the two filters are matching by insuring that R*C = L/R_W, then the voltage across the capacitor is equal to the value of the voltage across the winding resistance R_W, $V_{CAP} = I_{LOAD}*R_W$. Based on this, the voltage across the capacitor is measured, and with a known R_W value, the load current can be extracted. The measured current value will be digitized by the ADC and stored in a register for the processor to access. The method used on the 900844 measures the voltage across R_W in a similar fashion, while using internal sensing circuitry.

The sensed output current value will also be used for over-current protection. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation, and alert the system through the VCCFAULT signal, which will in turn assert the VRFAULT Interrupt signal.

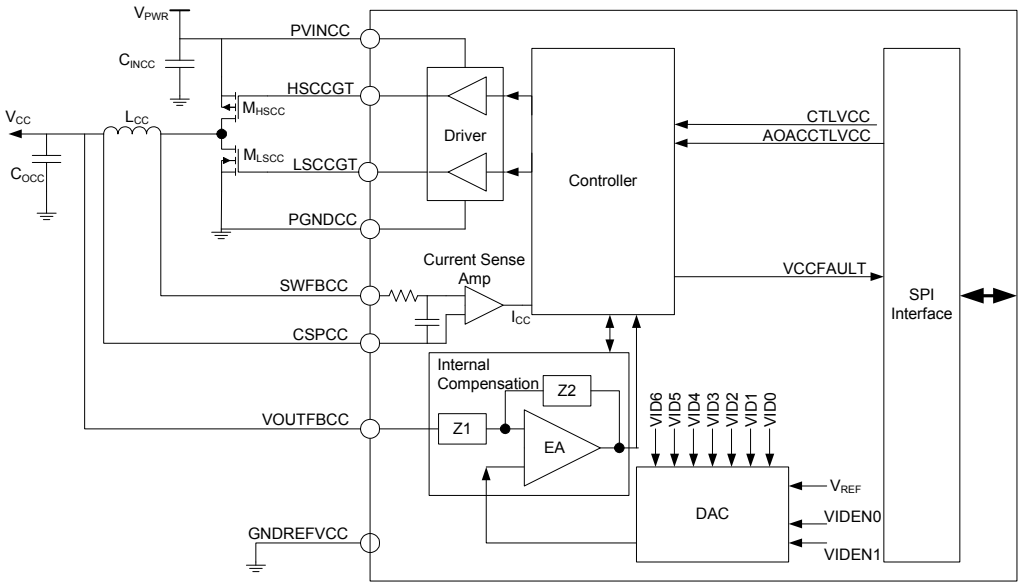


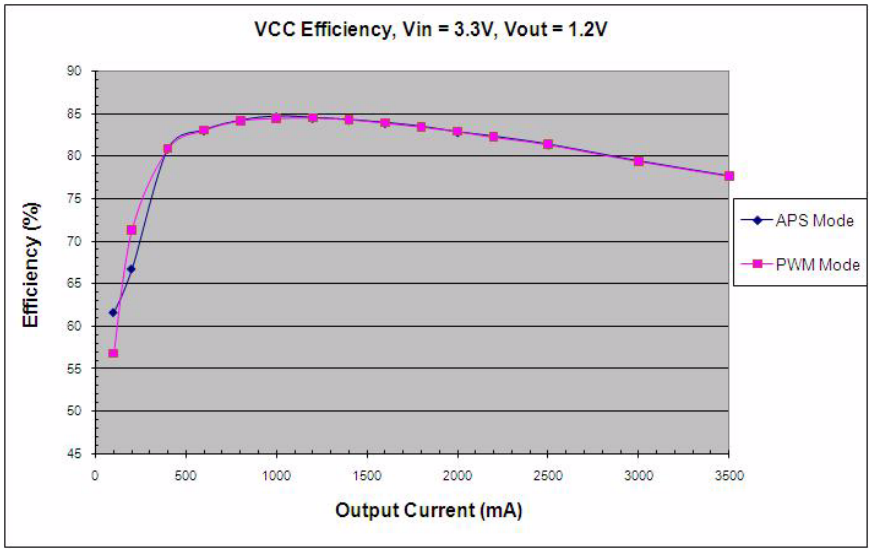
Figure 23. VCC Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used to provide power to the CPU Core.
- Single-phase Solution with Integrated Drivers and external MOSFETs
- VID Controlled for dynamic voltage scaling requirements of high performance processors
- 1.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Loss-Less Output Current Sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

The efficiency curves in Figure 24 are calculated under PWM mode, based on the recommended external component values and typical output voltage of 1.2 V. 3.0 V ≤ VPWR ≤ 4.4 V.



4

Figure 24. VCC Efficiency Curve

VCC Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 25. VCC Status Registers Structure and Bits Description

Name	Bits	Description	
VCCCNT (ADDR 0X35 - R/W - DEFAULT VALUE: 0X24)			
CTLVCC	2:0	VCC State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLVCC	5:3	VCC State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	
VCCLATCH (ADDR 0X32 - R/W - DEFAULT VALUE: 0X7F)			
VIDVCC	6:0	VID VCC Control Through SPI. Signal codes are identical to the VID signal codes. Reference Figures 15 for more details	
DVP1VRD	7	VCC Register override enable bit. X0 = VCC VID control follows the external pins x1 = VCC VID control follows the VIDVCC control register bits	

VNN

This is a VID controlled single-phase 1.0 MHz 2-switch synchronous Buck PWM voltage mode control DC/DC regulator, designed to power high performance CPUs. VNN uses external MOSFETs, P-ch high side and N-ch low side.

VNN includes support for VID active voltage positioning requirements. A 7-bit DAC reads the VID input signals and sets the output voltage level. The output voltage has a range of 0.3 to 1.2 V. The programming step size is 12.5 mV. Values will be read in real time and will be stored in internal registers not accessible to the system host. Reference VIDEN[1:0] & VID[6:0] Pins.

The same VID input signals are shared between VNN and VNN, where a latch signal for each regulator decides which regulator takes control of the VID input signals.

The DAC value represents the output voltage value. The output voltage node is connected directly to the inverting input of the error amplifier that uses the DAC output as its reference, unity gain configuration. Using this configuration with internal compensation eliminates the need for the feedback and compensation network, which saves board space and cost. The DAC/ output voltage slew rate is internally set 25 mV/µs to minimize transient currents and audible noise.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The previous selection is optimized to maximum battery life based on load conditions.

VNN will be discharged every time the regulator is shutting down.

The output current is sense in the same way as it is done on VCC regulator. (See VCC)

The sensed output current value will also be used for over-current protection. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation and alert the system through the VNNFAULT signal, which will in turn assert the VRFAULT Interrupt signal.

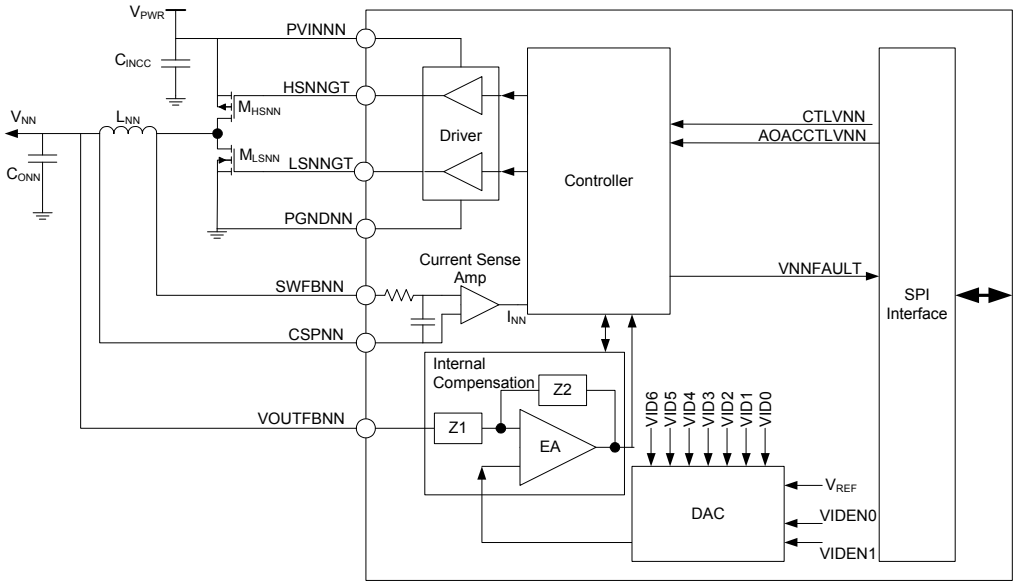


Figure 25. VNN Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used to provide power to the Graphics Core.
- Single-phase Solution with Integrated Drivers and external MOSFETs
- VID Controlled for dynamic voltage scaling requirements of high performance processors
- 1.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Loss-Less Output Current Sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

Figure 26 efficiency curves are calculated under PWM mode based on the recommended external component values and typical output voltage of 1.2 V. 3.0 V ≤ VPWR ≤ 4.4 V.

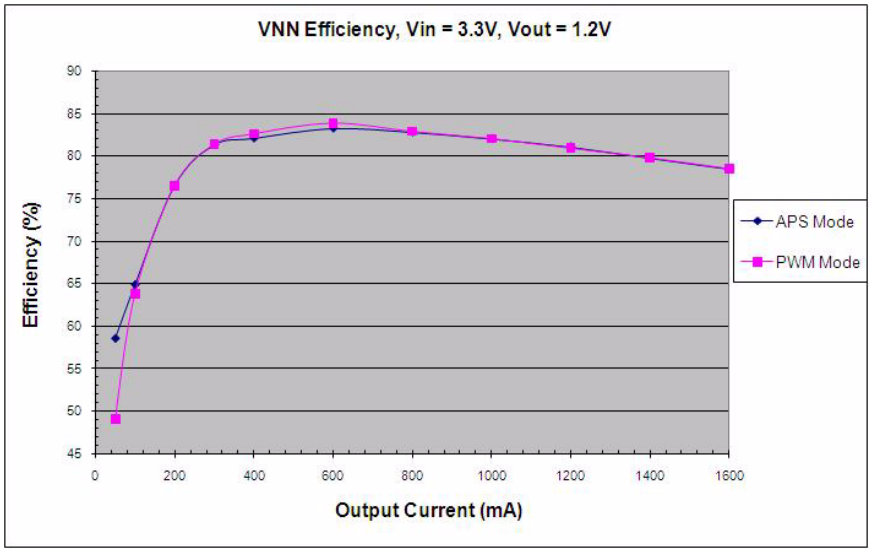


Figure 26. VNN Efficiency Curve

VNN Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers

Table 26. VNN Status and Control Registers Structure and Bits Description

Name	Bits	Description	
VNNCNT (ADDR 0x36 - R/W - Default value: 0x04)			
CTLVNN	2:0	VNN State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLVNN	5:3	VNN State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	
VNNLATCH (ADDR 0x33 - R/W - Default value: 0x7F)			
VIDVNN	6:0	VID VNN Control Through SPI. Signal codes are identical to the VID signal codes. Reference Figure 15 for more details	
DVP1VRD	7	VNN Register override enable bit. X0 = VNN VID control follows the external pins x1 = VNN VID control follows the VIDVNN control register bits	

VDDQ

This is a 4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage mode control DC/DC regulator.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode.

VDDQ will be discharged every time the regulator is shutting down.

The output current is measured internally, digitized by the ADC, and stored in a register for the processor to access. The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through a cycle by cycle operation and alert the system through the VDDQFAULT signal, which will in turn assert the VRFAULT Interrupt signal.

VDDQ is originally prepared to provide 1.8 V by connecting VDDQ output voltage directly to FBDDQ node, refer to Figure 27. To provide flexibility, VDDQ can also be set to 1.5 V by adding a resistor divider from VDDQ output to the FBDDQ using VCORE as voltage reference, refer to Figure 28. The following are the recommended resistor values for the feedback divider:

- RFBDDQ15_1 = 680 Ω
- RFBDDQ15_2 = 2.21 kΩ

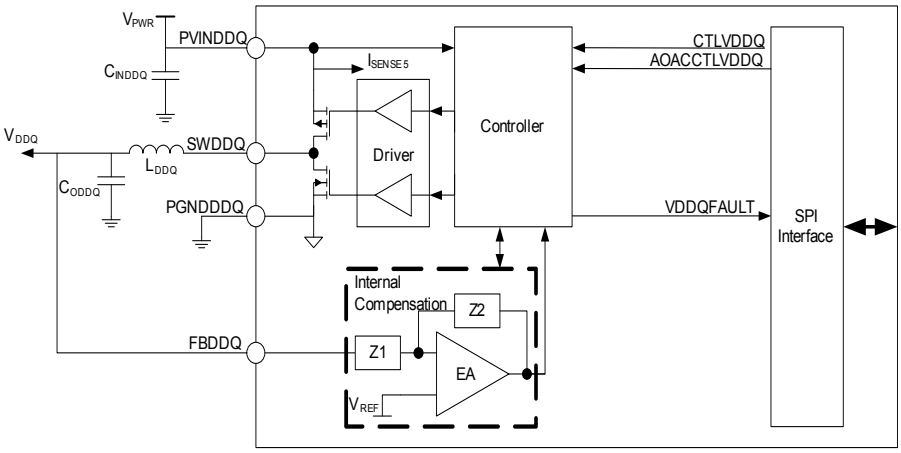


Figure 27. VDDQ Detailed Internal Block Diagram (VDDQ at 1.8 V)

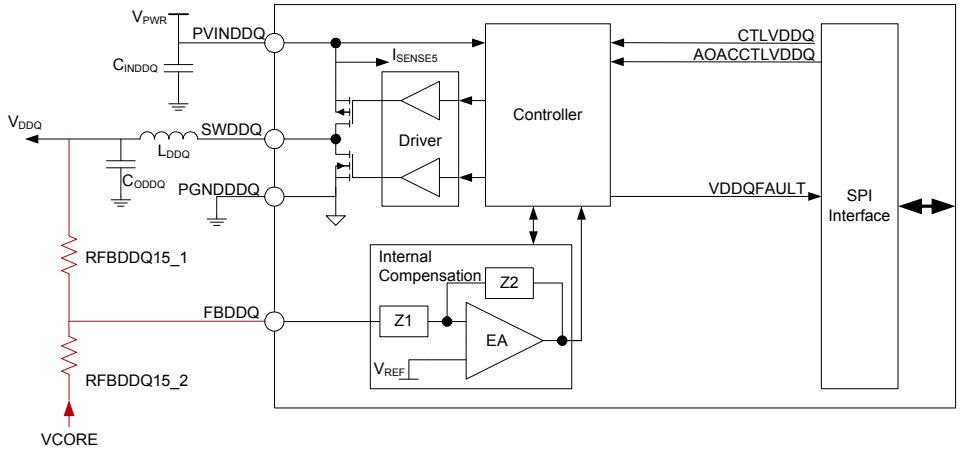


Figure 28. VDDQ Detailed Internal Block Diagram (VDDQ at 1.5 V)

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used as a pre-regulator to many LDO rails, for enhanced efficiency and reduced thermal dissipation. It also supplies power to rails in the CPU (central processing unit), Platform controller hub, and the platform
- Uses Integrated MOSFETs
- 4.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Peak current sensing with over-current protection

- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

Figure 29 efficiency curves are calculated under PWM mode, based on the recommended external component values and typical output voltage of 1.8 V. 3.0 V ≤ VPWR ≤ 4.4 V.

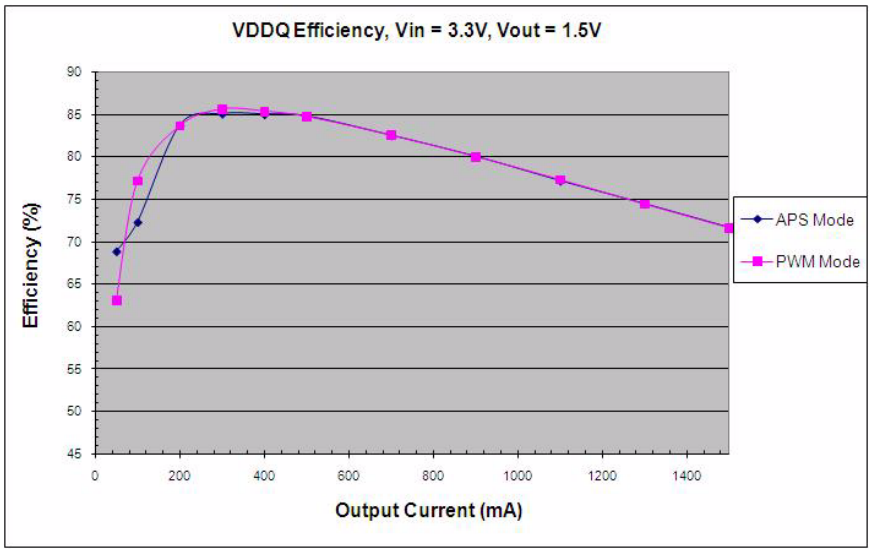


Figure 29. VDDQ Efficiency Curves

VDDQ Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 27. VDDQ Status and Control Register Structure and Bits Description

Name	Bits	Description	
VDDQCNT (ADDR 0x37 - R/W - Default Value: 0x04)			
CTLVDDQ	2:0	VDDQ State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLVDDQ	5:3	VDDQ State Control during AOAC Exit (when EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	

V21

This is a 4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage-mode control DC/DC regulator.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The previous selection is optimized to maximum battery life based on load conditions.

V21 will be discharged every time the regulator is shutting down.

The output current is measured internally, digitized by the ADC, and stored in a register for the processor to access.

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation and alert the system through the V21FAULT signal, which will in turn assert the VRFAULT Interrupt signal.

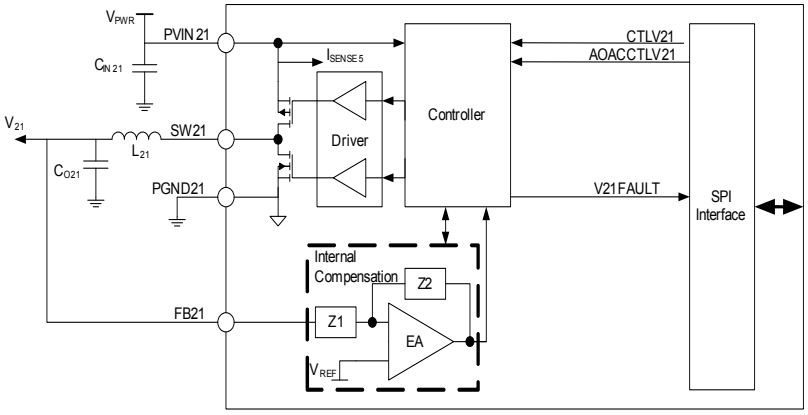


Figure 30. V21 Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used as a pre-regulator to many LDO rails, for enhanced efficiency and reduced thermal dissipation.
- Uses Integrated MOSFETs
- 4.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Peak current sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

Figure 31 efficiency curves are calculated under PWM mode, based on the recommended external component values and typical output voltage of 2.1 V. 3.0 V ≤ V_{PW} ≤ 4.4 V.

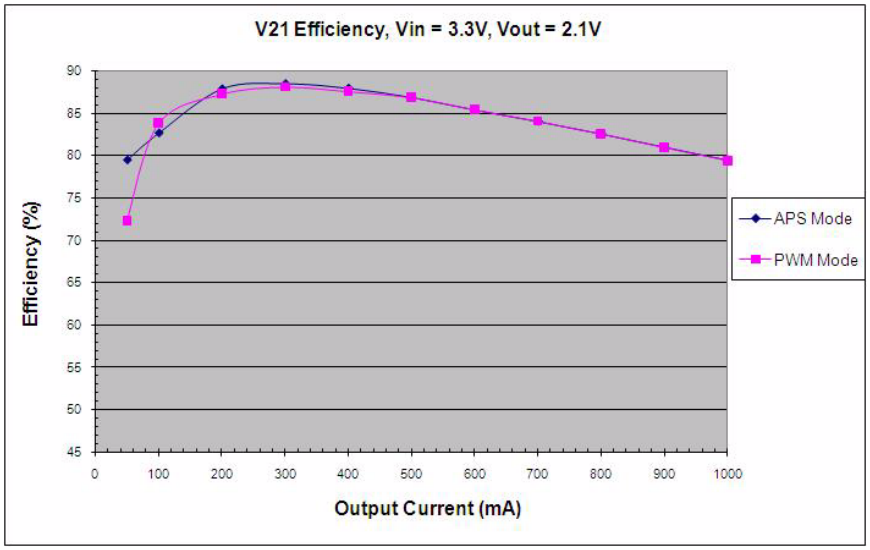


Figure 31. V21 Efficiency Waveforms

V21 Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 28. V21 Status/Control Registers Structure and Bits Description

Name	Bits	Description	
V21CNT (ADDR 0x38 - R/W - Default value: 0x07)			
CTLV21	2:0	V21 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLV21	5:3	V21 State Control during AOAC Exit (when EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
Reserved	7:6	Reserved	

V15

This is a 4.0 MHz fully integrated 2-switch synchronous Buck PWM voltage-mode control DC/DC regulator.

The switcher can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode, and a PWM mode. The above selection is optimized to maximum battery life based on load conditions.

V15 will be discharged every time the regulator is shutting down.

The output current is measured internally, digitized by the ADC, and stored in a register for the processor to access.

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation and alert the system through the V15FAULT signal, which will in turn assert the VRFAULT Interrupt signal.

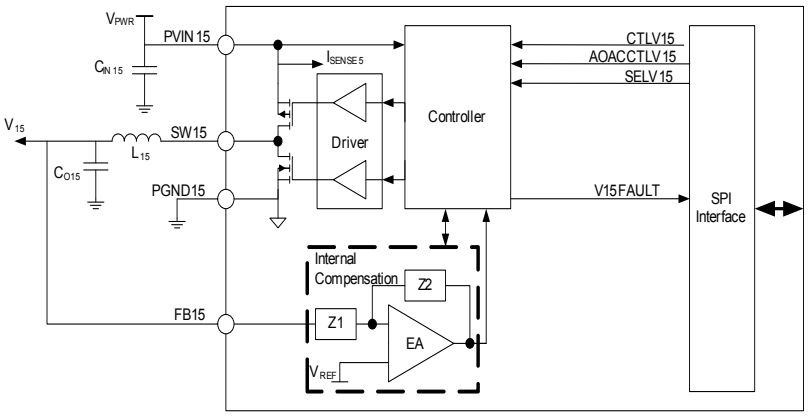


Figure 32. V15 Detailed Internal Block Diagram

Main Features

- Uses the V_{PWR} rail as its power supply
- It is used as a pre-regulator to many LDO rails, for enhanced efficiency and reduced thermal dissipation. It also supplies power to rails in the Platform controller hub
- Uses Integrated MOSFETs

- 4.0 MHz switching frequency
- High efficiency operating modes depending on load conditions
- Output can be discharged through the low side switch.
- Peak current sensing with over-current protection
- Uses internal compensation
- Gate drive circuits are supplied directly from VPWR

Efficiency Curves

Figure 33 efficiency curves are calculated under PWM mode, based on the recommended external component values and typical output voltage of 1.5 V. 3.0 V ≤ V_{PWR} ≤ 4.4 V.

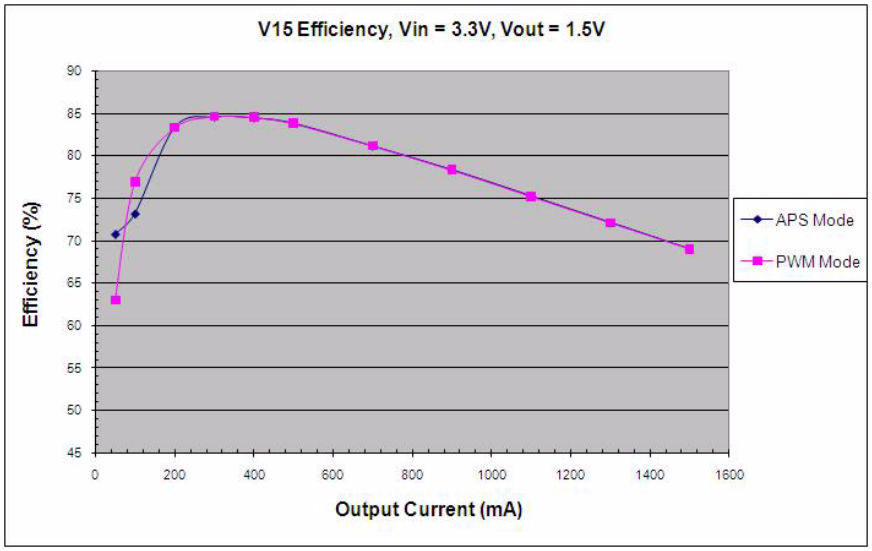


Figure 33. V15 Efficiency Curves

V15 Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 29. V15CNT Register Structure and Bits Description

Name	Bits	Description	
V15CNT (ADDR 0x39 - R/W - Default value: 0x07)			
CTLV15	2:0	V15 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
AOACCTLV15	5:3	V15 State Control during AOAC Exit (when EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = PFM x6 = Automatic Pulse Skipping x7 = PWM
SELV15	7:6	V15 Output Voltage Selection (FSL Usage Only) X0 = 1.5 V x1 = 1.6 V x2, x3 = Reserved	

LDO POWER SUPPLIES

Freescale's power management solution for the Ultra-mobile platform for Netbooks, Tablets, and Slates includes 14 LDO regulators, all of which are housed in the 900844 PMIC.

LDO OPERATION MODES SELECTIONS

- OFF - The regulator is switched off
- ACTIVE - The regulator is switched on and the output is at the programmed level. The maximum load current is allowed.
- LOW POWER - The regulator is switched on and the outputs is at the programmed level. The load current is limited.
- TEST/TRIM - This is not a functional mode, thus requiring certain steps to prevent unintentional activation of this mode. During this mode, the device performs measurements and trimming.

All LDOS are able to work in a low power mode, in which the bias current is reduced. The output drive capability and performance are limited in this mode. This mode occurs automatically when the load current decreases below the low power mode limit, except on VBG and VMM, in which this mode can only be set through SPI programming. All other LDOS can set the low power mode through SPI programming.

Note: If low power mode is set through the SPI at a load current higher than the maximum allowed, the performance of the LDO is not guaranteed.

Table 30 is a summary of LDO characteristics

Table 30. 900844 LDO Power Supplies Summary

Regulator	Typ. Voltage	Max Continuous Current	Description
VBG	1.25 V	2.0 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCCA	1.5 V	150 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCC180	1.8 V	390 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VPNL18	1.8 V	225 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VPMIC	1.8 V	50 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VYMXYFI18	1.8 V	200 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCCPAOAC	1.05 V	155 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCCPDDR	1.05 V	60 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VAON	1.2 V	250 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VMM	1.2 V	5.0 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VCCP	1.05 V	445 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VIMG25	2.5 V	80 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VIMG28	1.5 - 2.9 V	225 mA	Low Dropout (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR with a low quiescent current and fast transient response.
VSDIO	1.8 or 3.3 V	215 mA	VSDIO is a combo Low Dropout (LDO) and power switch. It uses an external P-CH Pass FET, applicable only in power switch mode. VSDIO serves as an LDO when its output voltage is set to 1.8 V, and as a switch when its output voltage is set to 3.3 V.

VBG

VBG is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VBG is actively discharged during shutdown.

VBG shares an input voltage pin (PVIN1P8) and a reference ground pin (GND1P8) with the VCCA regulator, yet each has independent control. PVIN1P8 is supplied from the VDDQ voltage if VDDQ output is set to 1.8 V, otherwise connect to V21 when VDDQ is set to 1.5 V.

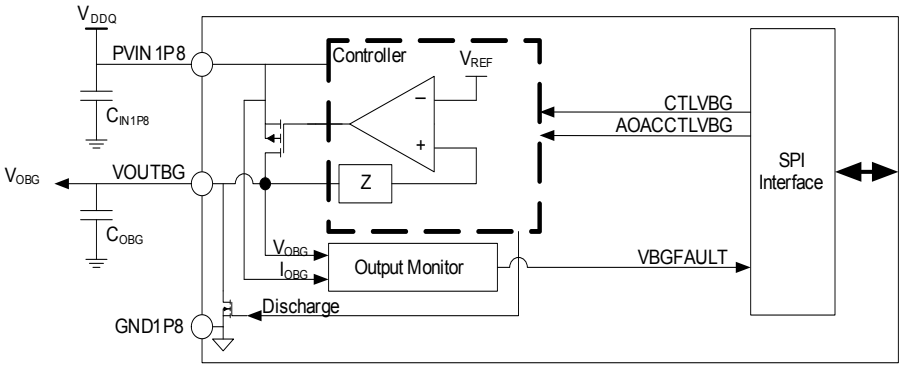


Figure 34. VBG Detailed Internal Block Diagram

Main Features

- Uses VDDQ or V21 as the main power supply
- 2.0 mA maximum continuous output current
- Optimized for a 1.0 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

VBG Status/Control Registers and Bits Description

Reference the register map for read/write conditions and default state for each of these registers.

Table 31. VBG Control Register Structure and Bits Description

Name	Bits	Description	
VLBGCNT (ADDR 0x3F - R/W - Default Value: 0 x24)			
CTLVBG	2:0	VBG State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVBG	5:3	VBG State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCCA

VCCA is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCA is actively discharged during shutdown.

VCCA shares an input voltage pin (PVIN1P8) and a reference ground pin (GND1P8) with VBG regulator, yet each has independent control. PVIN1P8 is supplied from the VDDQ voltage if VDDQ output is set to 1.8 V, otherwise connect to V21 when VDDQ is set to 1.5 V.

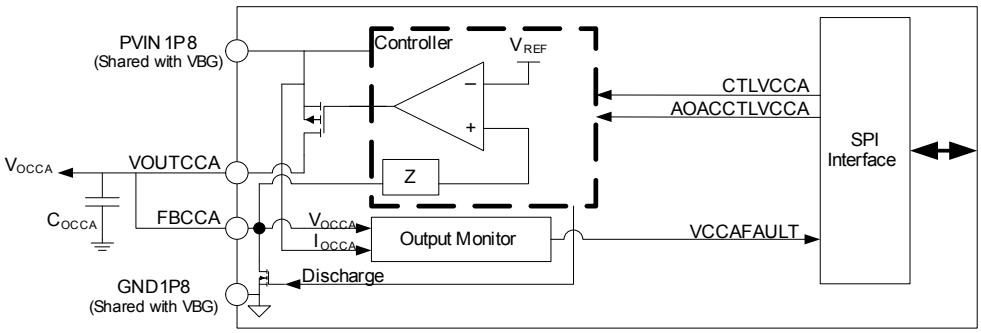


Figure 35. VCCA Detailed Internal Block Diagram

Main Features

- Uses VDDQ or V21 as the main power supply
- 150 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 32. VCCA Control Register Structure and Bits Description

Name	Bits	Description	
VCCACNT (ADDR 0x40 - R/W - Default Value: 0x3C)			
CTLVCCA	2:0	VCCA State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVCCA	5:3	VCCA State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCC180

VCC180 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCC180 is actively discharged during shutdown.

VCC180 shares an input voltage pin (PVIN2P1) and a reference ground pin (GND2P1) with VPNL18 and VPMIC regulators, yet each has independent control. PVIN2P1 is supplied from the V21 voltage.

The output current for VCC180 is measured and reported through the ADC. Reference ADC Subsystem for more information.

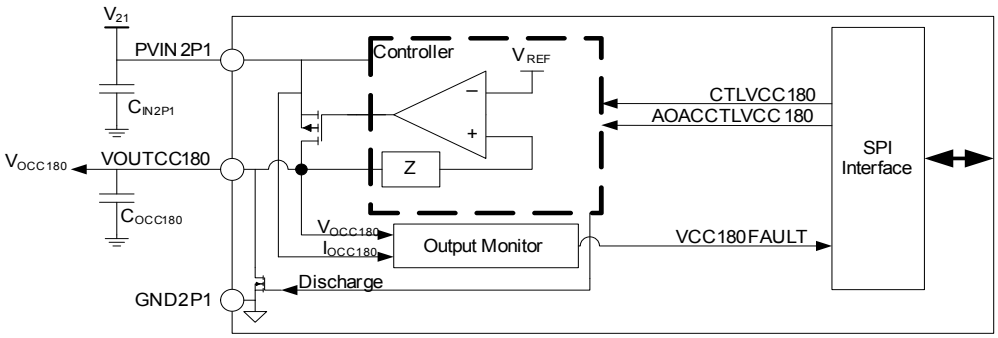


Figure 36. VCC180 Detailed Internal Block Diagram

Main Features

- Uses V21 as the main power supply
- 390 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 33. VCC180CNT Register Structure and Bits Description

Name	Bits	Description	
VCC180CNT (ADDR 0x43 - R/W - 0x3C)			
CTLVCC180	2:0	VCC180 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVCC180	5:3	VCC180 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VPNL18

VPNL18 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VPNL18 is actively discharged during shutdown.

VPNL18 shares an input voltage pin (PVIN2P1) and a reference ground pin (GND2P1) with VCC180 and VPMIC regulators, yet each has independent control. PVIN2P1 is supplied from the V21 voltage.

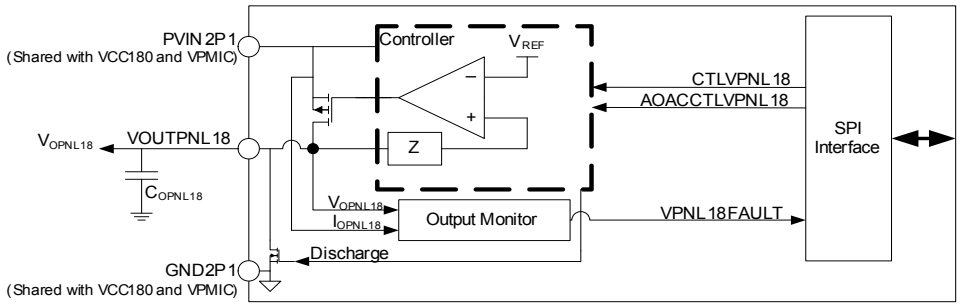


Figure 37. VPNL18 Detailed Internal Block Diagram

Main Features

- Uses V21 as the main power supply
- 225 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 34. VPNL18 Control Register Structure and Bits Description

Name	Bits	Description	
VPANEL18CNT (ADDR 0x46 - R/W - Default value: 0x24)			
CTLVPANEL18	2:0	VPNL18 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVPANEL18	5:3	VPNL18 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VPMIC

VPMIC is a low drop-out (LDO) fully integrated regulator with a P-CH pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VPMIC is actively discharged during shutdown.

VPMIC shares an input voltage pin (PVIN2P1) and a reference ground pin (GND2P1) with VCC180 and VPNL18 regulators, yet each has independent control. PVIN2P1 is supplied from the V21 voltage.

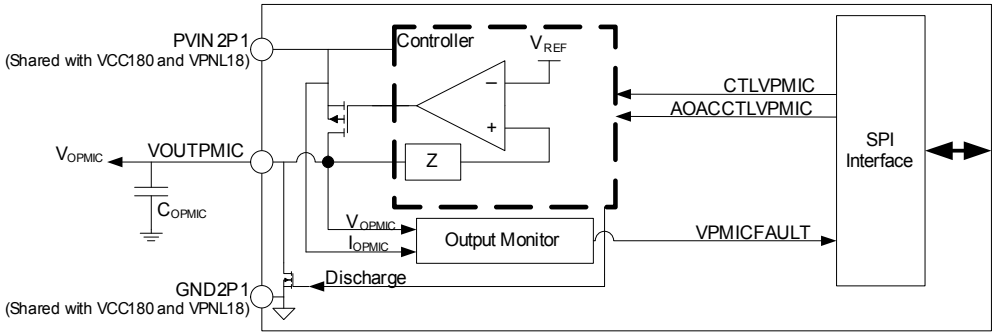


Figure 38. VPMIC Detailed Internal Block Diagram

Main Features

- Uses V21 as the main power supply
- 100 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 35. VPMIC Register Structure and Bits Description

Name	Bits	Description	
VPMICCNT (ADDR 0x41 - R/W - Default Value: 0x07)			
CTLVPMIC	2:0	VPMIC State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVPMIC	5:3	VPMIC State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VYMXYFI18

VYMXYFI18 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VYMXYFI18 is actively discharged during shutdown.

VYMXYFI18 can be supplied by either the V21 output voltage (V21) or directly from the VPWR node. Using V21 as the input voltage supply offers enhanced thermal performance and higher efficiency. Using the VPWR node can offer enhanced performance against noise coupling from an output of a DC/DC regulator. Users are encouraged to take the resulting thermal dissipation in account when supplying VYMXYFI18 directly from VPWR. For more information about package thermal capabilities, reference Thermal Management.

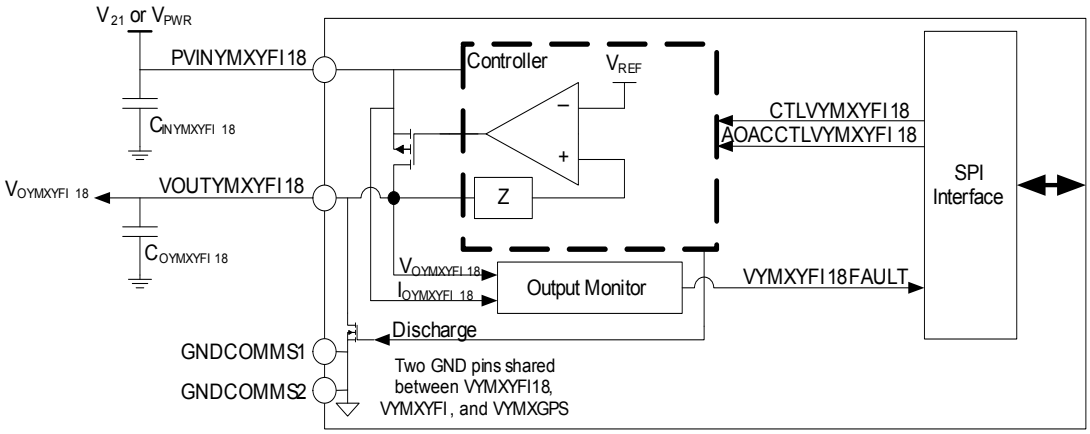


Figure 39. VYMXYFI18 Detailed Internal Block Diagram

Main Features

- Uses V21 or VPWR as the main power supply
- 200 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 36. VYMXYFI18 Register Structure and Bits Description

Name	Bits	Description	
VWYMXARFCNT (ADDR 0x4C - R/W - Default Value: 0x24)			
CTLVWYMXARF	2:0	VYMXYFI18 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVWYMXARF	5:3	VYMXYFI18 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCCPAOAC

VCCPAOAC is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCPAOAC is actively discharged during shutdown.

VCCPAOAC shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with VCCPDDR, VAON, VMM, and the VCCP regulator. Each has independent control. PVIN1P5 is supplied from the V15 voltage.

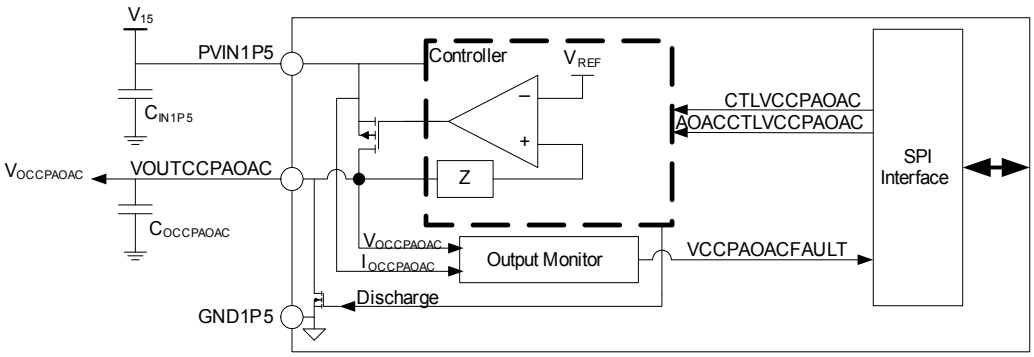


Figure 40. VCCPAOAC Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply.
- 155 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 37. VCCPAOACCNT Register Structure and Bits Description

Name	Bits	Description	
VCCPAOACCNT (ADDR 0x3D - R/W - Default Value: 0x07)			
CTLVCCPAOAC	2:0	VCCPAOAC State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVCCPAOAC	5:3	VCCPAOAC State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCCPDDR

VCCPDDR is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCPDDR is actively discharged during shutdown.

VCCPDDR shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VAON, VMM, and VCCP regulators, yet each has independent control. PVIN1P5 is supplied from the V15 voltage.

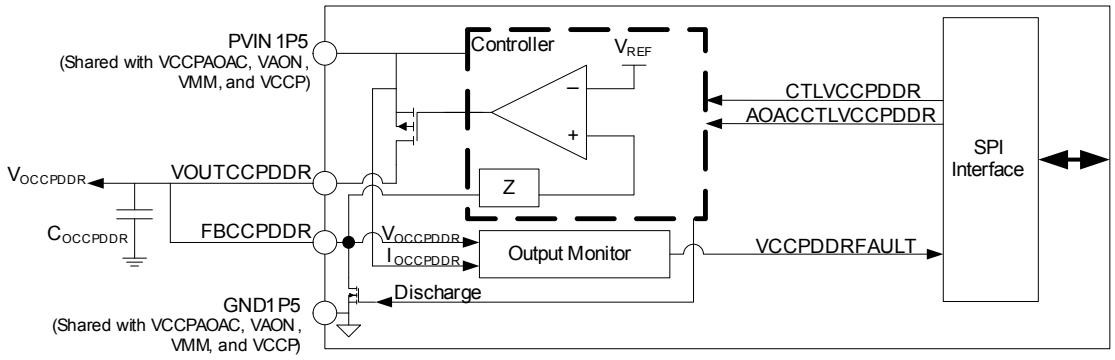


Figure 41. VCCPDDR Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 60 mA maximum continuous output current
- Optimized for a 1.0 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 38. VCCPDDR Control Register Structure and Bits Description

Name	Bits	Description	
VCCPDDRCNT (ADDR 0x3E - R/W - Default value: 0x3C)			
CTLVCCPDDR	2:0	VCCPDDR State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVCCPDDR	5:3	VCCPDDR State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VAON

VAON is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VAON is actively discharged during shutdown.

VAON shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VCCPDDR, VMM, and VCCP regulators, yet each has independent control. PVIN1P5 is supplied from the V15 voltage.

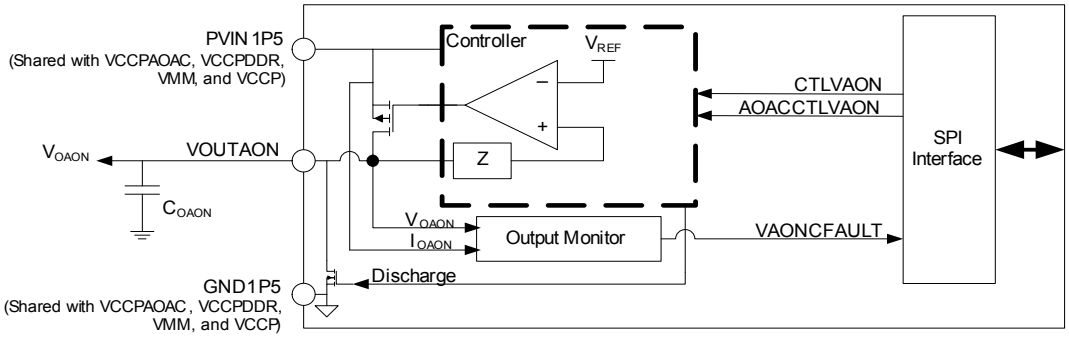


Figure 42. VAON Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 250 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 39. VAON Control Register Structure and Bits Description

Name	Bits	Description	
VAONCNT (ADDR 0x45 - R/W - Default Value: 0x07)			
CTLVAON	2:0	VAON State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVAON	5:3	VAON State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VMM

VMM is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VMM will be actively discharged during shutdown.

VMM shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VCCPDDR, VAON, and VCCP regulators, yet each has independent control. PVIN1P5 is supplied from V15 voltage.

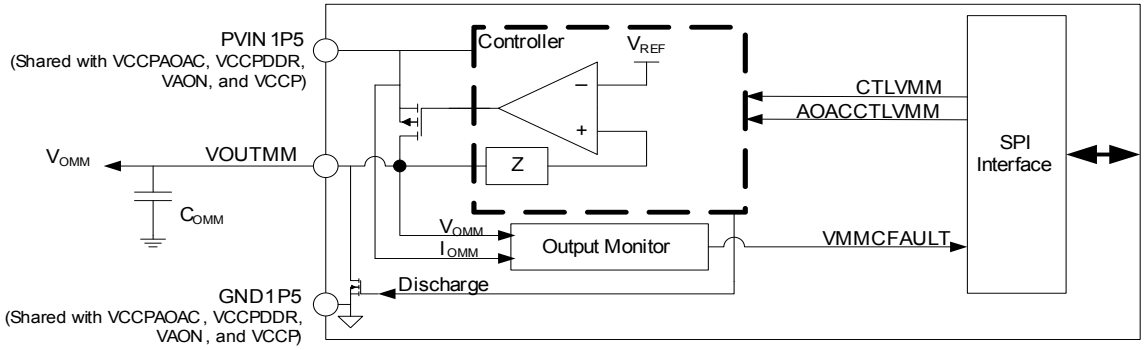


Figure 43. VMM Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 5.0 mA maximum continuous output current
- Optimized for a 1.0 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 40. VMM control Register Structure and Bits Description

Name	Bits	Description	
VMMCNT (ADDR 0x47 - R/W - Default Value: 0x24)			
CTLVMM	2:0	VMM State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVMM	5:3	VMM State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VCCP

VCCP is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VCCP is actively discharged during shutdown.

VCCP shares an input voltage pin (PVIN1P5) and a reference ground pin (GND1P5) with the VCCPAOAC, VCCPDDR, VAON, and VMM regulators, yet each has independent control. PVIN1P5 is supplied from V15 voltage.

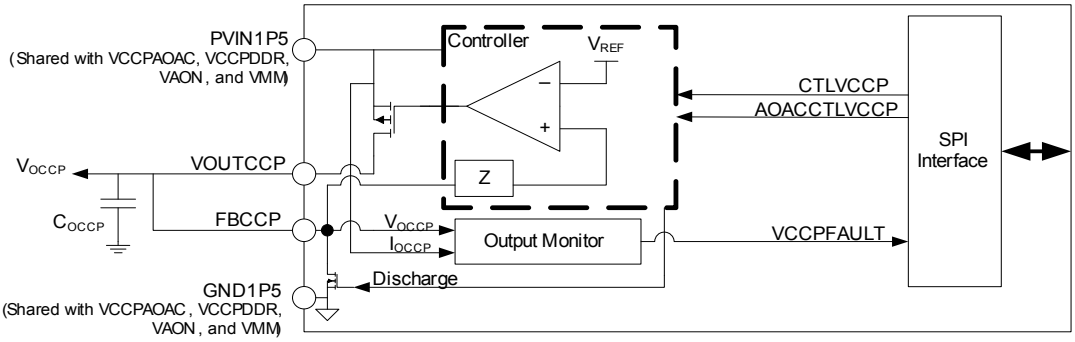


Figure 44. VCCP Detailed Internal Block Diagram

Main Features

- Uses V15 as the main power supply
- 445 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 41. VCCP Control Register Structure and Bits Description

Name	Bits	Description	
VCCPCNT (ADDR 0x44 - R/W - Default Value: 0x3C)			
CTLVCCP	2:0	VCCP State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVCCP	5:3	VCCP State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VIMG25

VIMG25 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VIMG25 is actively discharged during shutdown.

VIMG25 shares an input voltage pin (PVINIMG) and a reference ground pin (GNDIMG) with the VIMG28 regulator, yet each has independent control. Both can be supplied by the VPWR (3.3 V) node.

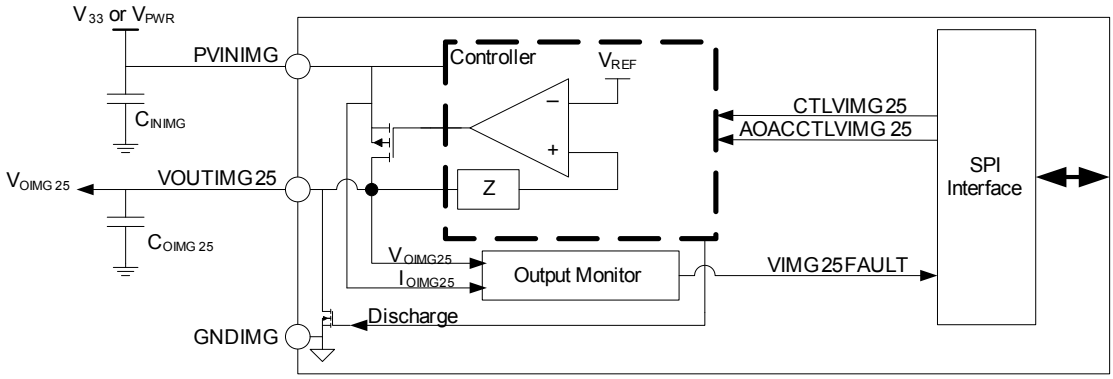


Figure 45. VIMG25 Detailed Internal Block Diagram

Main Features

- Uses VPWR (3.3V) as the main power supply
- 80 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 42. VIMG25 Register Structure and Bits Description

Name	Bits	Description	
VIMG25CNT (ADDR 0x42 - R/W - Default Value: 0x04)			
CTLVIMG25	2:0	VIMG25 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVIMG25	5:3	VIMG25 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

VIMG28

VIMG28 is a low drop-out (LDO) fully integrated regulator with a P-CH Pass FET. It is high performance, low noise, and high PSRR, with a low quiescent current and fast transient response. VIMG28 is actively discharged during shutdown.

VIMG28 shares an input voltage pin (PVINIMG) and a reference ground pin (GNDIMG) with the VIMG25 regulator, yet each has independent control. Both can be supplied by the VPWR (3.3 V) node. This LDO is optimized to work with 300 mV headroom, which leaves enough margin between the input and the highest output of this LDO. For more information about package thermal capabilities, reference Thermal Management.

- Note: At high VIMG28 output voltage selections, the output will start tracking the battery voltage when V_{BAT} decreases below V_{OIMG28} + 300 mV.

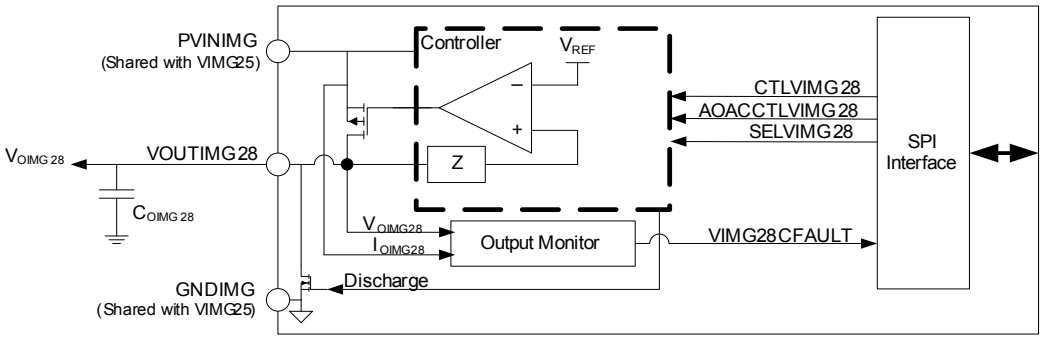


Figure 46. VIMG28 Detailed Internal Block Diagram

Main Features

- Uses 3.3 V or V_{PWR} as the main power supply
- 225 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses internal pass FET
- The output for each LDO is monitored for over-current conditions and under-voltage events

Table 43. VIMG28 Control Register Structure and Bits Description

Name	Bits	Description	
VIMGACNT (ADDR 0x0x48 - R/W - Default Value: 0x24)			
CTLVIMGA	2:0	VIMG28 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVIMGA	5:3	VIMG28 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
SELVIMGA	7:6	VIMG28 output voltage selections:	
		X0 = 1.5 V x1 = 2.7 V x2 = 2.8 V x3 = 2.9 V	

VSDIO

VSDIO is a combo low drop-out (LDO) and power switch. It uses an external P-CH pass FET in Switch mode, and internal pass FET on LDO mode.

VSDIO serves as an LDO when its output voltage is set to 1.8 V, and as a switch when its output voltage is set to 3.3 V. It takes its input voltage directly from the 3.3 V output voltage node.

VSDIO supplies the SDIO card module. The card is initially powered up to 3.3 V. If the card is detected to be a low voltage card, then the rail will be shutdown, configured as 1.8 V, and then turned on.

VSDIO will be actively discharged during shutdown.

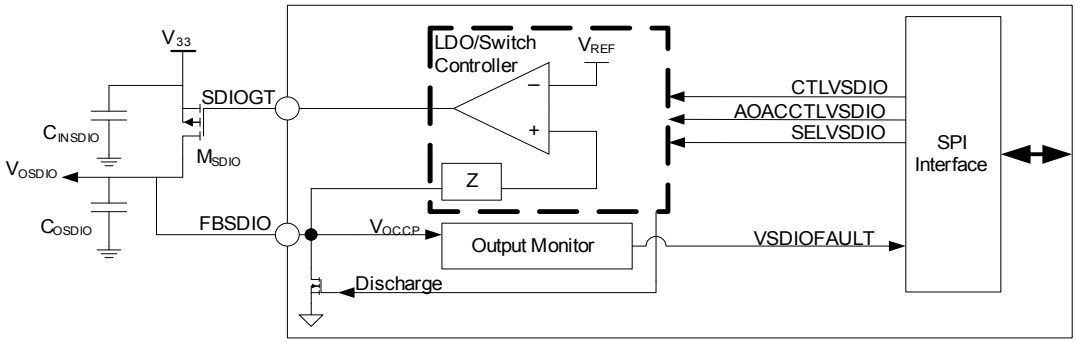


Figure 47. VSDIO Detailed Internal Block Diagram

MAIN FEATURES

- Uses 3.3 V as the main power supply
- 215 mA maximum continuous output current
- Optimized for a 2.2 µF external filter capacitor with a maximum of 10 mΩ ESR
- Uses an internal pass FET on LDO mode, and external pass FET on Switch mode.
- The output is monitored for under-voltage and over-current conditions in LDO mode.

Table 44. VSDIO Control Register Structure and Bits Description

Name	Bits	Description	
VSDIOCNT (ADDR 0x4D - R/W - Default Value: 0x64)			
CTLVSDIO	2:0	VSDIO State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVSDIO	5:3	VSDIO State Control during AOAC Exit (when Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
SELVSDIO	7:6	VSDIO output voltage selections:	
		X0 = 1.8 V x1 = 3.3 V x2 = Reserved x3 = Reserved	

POWER SWITCHES

Freescale's power management solution for the Ultra-mobile platform for Netbooks, Tablets and Slates, includes 1 dedicated power switch, housed in the 900844 PMIC. Table 45 shows its power characteristics.

VPNL33 uses an internal switch and are supplied from the 3.3 V output voltage.

Table 45. 900844 Power Switch Voltage Rail

Switch	Typ. Voltage	Max Current	Description
VPNL33	3.3 V	100 mA	Power Switch with integrated MOSFET and less than 1% voltage drop.

VPNL33 uses an internal switch and are supplied from the 3.3 V output voltage.

Table 46. Power Switches Control Registers Structure and Bits Description

Name	Bits	Description	
VPANEL33CNT (ADDR 0x4F - R/W - Default Value: 0x24)			
CTLVPANEL33	2:0	VPNL33 State Control	
		x0 = Reserved x1 = Reserved x2 = Reserved x3 = Reserved	x4 = OFF x5 = Low Power x6 = Active x7 = Active
AOACCTLVPANEL33	5:3	VPNL33 State Control during AOAC Exit (when the Exit pin is EXITSTBY pin is asserted). These bits will be initialized by the system SPI controller after power up.	
		X0 = Do not copy x1 = Do not copy x2 = Do not copy x3 = Do not copy	x4 = OFF x5 = Low Power x6 = Active x7 = Active
Reserved	7:6	Reserved	

POWER SUPPLY REGISTER MASK

Mask writes to the power supply registers, in order to avoid the need for the system controller to do read-modify-write cycles. The mask register is shown in Table 47.

Table 47. Mask Register

Register name	ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	initial
PWRMASK	0x34	R/W	M7	M6	M5	M4	M3	M2	M1	M0	0x00

Figure 48 shows an example of the operation of the PWRMASK register.

	D7	D6	D5	D4	D3	D2	D1	D0
Power Supply Register Before Write	1	0	1	0	1	0	1	0
PWRMASK Register Settings	1	1	1	1	0	0	0	0
Example SPI Write to Power Supply	1	1	1	1	1	1	1	1
Power Supply Register After Write	1	0	1	0	1	1	1	1

Figure 48. PWRMASK Register Implementation Example

POWER SUPPLY PROGRAMMABLE RAMP RATE

Turn on time of all buck regulators can be programmed through the SPI, reference Table 48

Table 48. Ramp Rate Control Registers (Freescale Defined)

Name	Bits	Description
FSLTONTCNTL1 (ADDR 0x1C8 - R/W - Default Value: 0xAA)		
VCCTONT	1:0	Turn On Time Settings for VCC Regulator x0 = 180 µs x1 = 90 µs x2 = 45 µs x3 = 22 µs
VNNTONT	3:2	Turn On Time Settings for VNN Regulator x0 = 180 µs x1 = 90 µs x2 = 45 µs x3 = 22 µs

Table 48. Ramp Rate Control Registers (Freescale Defined)

Name	Bits	Description
VDDQTONT	5:4	Turn On Time Settings for VDDQ Regulator x0 = 240 µs x1 = 120 µs x2 = 60 µs x3 = 30 µs
RSVD	7:6	RSVD
FSLTONTCNTL2 (ADDR 0x1CB - R/W - Default Value: 0xAA)		
V21TONT	1:0	Turn On Time Settings for V21 Regulator x0 = 320 µs x1 = 160 µs x2 = 80 µs x3 = 40 µs
V15TONT	3:2	Turn On Time Settings for V15 Regulator x0 = 200 µs x1 = 100 µs x2 = 50 µs x3 = 25 µs
Reserved	7:4	Reserved

POWER SUPPLIES FAULT MANAGEMENT

This section discusses faults related to, or caused by power supplies (directly or indirectly) operating outside their specified boundaries.

Reference Interrupt Controller for more information on the various interrupt signals, and the interrupt mechanism used to communicate to the system controller.

THERMAL MANAGEMENT

The thermal protection is based on a circuit with a voltage output that is proportional to the absolute temperature. This voltage can be read out via the ADC for precise temperature readouts. See ADC Subsystem.

This voltage is monitored by an integrated comparator. Interrupt THRM will be generated, if not masked, when crossing the thermal warning threshold TWARN, and sets the VRFAULT 1st level interrupt that causes the PMICINT pin to assert, notifying the system controller of a system event.

In addition to the previous, the 900844 includes integrated thermal protection that shuts down and powers off the system, in cases of over dissipation, if the junction temperature exceeds the TSHUTDOWN threshold. This thermal protection will act above the maximum junction temperature, to avoid any unwanted power downs. The protection is de-bounced by one period of the 32 kHz clock in order to suppress any (thermal) noise. This protection should be considered as a fail-safe mechanism. Therefore, the application design should execute a thermal shutdown under normal conditions.

Once the thermal event is cleared and the temperature is back to its normal range, the 900844 restarts automatically, by following the steps outlined in Initial Power Up Sequence

Table 49. Thermal Warning/Shutdown Thresholds

Parameter	Min	Typ	Max	Unit
Thermal Warning Threshold	115	120	125	°C
Thermal Warning Hysteresis	2	-	4	°C
Thermal Shutdown Threshold	130	140	150	°C

VRFAULT

Every supply is equipped with a fault reporting signal called xxxFAULT, where xxx is the name of the power supply. This FAULT signal is an OR function of all of the following possible faults, or just a subset of them depending on the power supply:

- Output under-voltage
- Output over-voltage
- Over-current
- Short-circuit

Reference each power supply's section for more information on what faults are included, and how the supply protects itself and the load in response to the fault.

All of the xxxFAULT signals from all power supplies are ORed together into the BATOCP interrupt signal, which if unmasked, sets the VRFAULT 1st level interrupt that causes the PMICINT pin to assert, notifying the SC of a system event. The SC can service the VRFAULT register and access the FAULTx registers for more information on which supply caused the fault. The SC can then take different measures, depending on the supply in question.

The xxxFAULT signals are stored in the Freescale defined registers section (Addr 0x180 - 0x1FF), which is meant for extended functionality.

Table 50. FSLFAULT1 Fault Status Register Structure and Bit Description

Name	Bits	Description
FSLFAULT1 (ADDR 0X1CC - R/W - DEFAULT VALUE: 0X00)		
VCCFAULT	0	VCC Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VNNFAULT	1	VNN Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VDDQFAULT	2	VDDQ Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
V21FAULT	3	V21 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
V15FAULT	4	V15 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
RSVD	7:5	Reserved

Table 51. FSLFAULT2 Fault Status Register Structure and Bit Description

Name	Bits	Description
FSLFAULT2 (ADDR 0X1CD - R/W - DEFAULT VALUE: 0X00)		
RSVD	2:0	Reserved
VBGFAULT	3	VBG Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCCAFAULT	4	VCCA Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCC180FAULT	5	VCC180 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VPNL18FAULT	6	VPNL18 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VPMICFAULT	7	VPMIC Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists

Table 52. FSLFAULT3 Fault Status Register Structure and Bit Description

Name	Bits	Description
FSLFAULT3 (ADDR 0X1CE - R/W - DEFAULT VALUE: 0X00)		
VYMXYFI18FAULT	0	VYMXYFI18 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
RSVD	2:1	Reserved
VCCPAOACFAULT	3	VCCPAOAC Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCCPDDRFAULT	4	VCCPDDR Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VAONFAULT	5	VAON Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VMMFAULT	6	VMM Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VCCPFAULT	7	VCCP Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists

Table 53. FSLFAULT4 Fault Status Register Structure and Bit Description

Name	Bits	Description
FSLFAULT4 (ADDR 0X1CF - R/W - DEFAULT VALUE: 0X00)		
VIMG25FAULT	0	VIMG25 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
VIMG28FAULT	1	VIMG28 Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
RSVD	2	Reserved
VSDIOFAULT	3	VSDIO Regulator Fault Signal x0 = No Fault Exists x1 = Fault Exists
Reserved	7:4	Reserved

Power Supplies Fault Management Interrupt/Mask Registers.

Table 54. Fault Management Status and Control Register Structure and Bits Description

Name	Bits	Description
VRFAULTINT (ADDR 0X30 - R - DEFAULT VALUE: 0X00)		
THRM	0	PMIC Thermal Warning Flag x0 = PMIC temperature below warning threshold x1 = PMIC temperature above warning threshold
RSVD	1	Reserved
VRFAIL	2	Regulator fault present flag x0 = No fault x1 = Fault Exists
Reserved	7:3	Reserved
MVRFAULTINT (ADDR 0X31 - R/W - DEFAULT VALUE: 0X03)		
MTHRM	0	PMIC Thermal Warning Flag Mask x0 = Flag unmasked x1 = Flag masked
RSVD	1	Reserved
VRFAIL	2	Regulator fault present flag Mask x0 = Flag unmasked x1 = Flag masked
Reserved	7:3	Reserved

COIN CELL BATTERY CHARGER INTERFACE

COIN CELL BATTERY BACKUP/CHARGER

The COIN CELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged or removed, and in the absence of a USB/Wall input source, the RTC system and coin cell maintained logic, will switch over to the COIN CELL for backup power. A small capacitor should be placed from the COIN CELL pin to ground under all circumstances.

The coin cell charger circuit will function as a current limited voltage source, resulting in the CC/CV taper characteristic, typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHGEN bit. which is enabled by default. The output voltage (V_{COIN}) is programmable through the VCOIN[2:0] bits. The coin cell charger voltage is programmable in the active state, where the charge current is fixed at I_{COINHI}. The coin cell charging will be stopped when V_{PWR} goes below V_{PWRUVF}. Reference Power Path Manager SPI Registers for a more detailed description of the coin cell related bits.

A large capacitor, electrolytic or super cap, can also be used instead of a lithium based coin cell. To avoid discharge by leakage currents from external components or by the 900844, the COINCHGEN bit should always remain set.

Coin cell charge is equipped with a disconnect circuitry that isolates the coin cell from any loads, if V_{COIN} goes below 2.0 V, to prevent the coin cell from being deeply discharged and damaged. This will also cause the ADC reading of the coin cell voltage to yield zero.

POWER PATH MANAGER SPI REGISTERS

Table 55. Input Power Interrupt/Mask Registers Structure and Bits Description

Name	Bits	Description
CHRGINT (ADDR 0XD0 - R - DEFAULT VALUE: 0X00)		
Reserved	0	Reserved
BATOVP	1	Input voltage over-voltage Interrupt Signal (V_{BAT} > V_{CHGCV} + $V_{OVRVOLT}$) x0 = No over-voltage condition x1 = Over-voltage condition
TEMP	2	Battery over/under-temperature Interrupt Signal (Battery temperature is out of valid window) x0 = No over/under-temperature condition x1 = Over/under-temperature condition
RSVD	3	Reserved
RSVD	4	Reserved
BATDET	5	Input voltage detection Interrupt Signal This is a dual edge interrupt signal that is set any time a valid Input Voltage (VBAT > VTRKL) is connected or disconnected x0 = No interrupts pending x1 = 3.3 V supply is connected/disconnected (refer to the SCHRGINT register)
RSVD	7:6	Reserved
MCHRGINT (ADDR 0XD1 - R/W - DEFAULT VALUE: 0X00)		
Reserved	0	Reserved
MBATOVP	1	Input voltage over-voltage Interrupt Signal Mask x0 = Unmask x1 = Mask
MTEMP	2	Input voltage over/under-temperature Interrupt Signal Mask x0 = Unmask x1 = Mask
RSVD	3	Reserved
RSVD	4	Reserved

Table 55. Input Power Interrupt/Mask Registers Structure and Bits Description

Name	Bits	Description
MBATDET	5	Battery Detection Interrupt Signal Mask x0 = Unmask x1 = Mask
RSVD	7:6	Reserved
SCHRGINT (ADDR 0XD2 - R - DEFAULT VALUE: 0X00)		
Reserved	0	Reserved
SBATOVP	1	Input voltage over-voltage Status x0 = Input voltage is lower than the limit (< V_{CHGCV} + $V_{OVRVOLT}$) x1 = Input voltage is higher than the limit (> V_{CHGCV} + $V_{OVRVOLT}$)
STEMP	2	Battery temperature Status x0 = Battery temperature is within valid window x1 = Battery temperature is out of valid window
RSVD	3	Reserved
RSVD	4	Reserved
SBATDET	5	Battery Present Status Signal x0 = Battery not present (VBAT < VTRKL) x1 = Battery present (VBAT > VTRKL)
RSVD	7:6	Reserved

INPUT POWER PATH REGISTERS AND BITS DESCRIPTION

Table 56. FSL Charger Control Register Structure and Bits Description

Name	Bits	Description
FSLCHRGCNTL (ADDR 0X1D1 - R/W - DEFAULT VALUE: 0X13)		
RSVD	0	Reserved
COINCHEN	1	Coin cell Charger Enable/Disable x0 = Disable x1 = Enable (Default)
VCOIN	4:2	Coin cell Charger Output Voltage Setting x0 = 2.5 V x1 = 2.7 V x2 = 2.8 V x3 = 2.9 V x4 = 3.0 V (Default) x5 = 3.1 V x6 = 3.2 V x7 = 3.3 V
Reserved	7:5	Reserved

ADC SUBSYSTEM

CONVERTER CORE

The ADC core is a 10 bit converter. The ADC core and logic run at an internally generated frequency of approximately 1.33 MHz. If an ADC conversion is requested while the PLL was not active, it will automatically be enabled by the ADC. A 32.768 kHz equivalent time base is derived from the 2.0 MHz clock to time ADC events. The ADC is supplied from VCORE. The ADC core has an integrated auto calibration circuit which reduces the offset and gain errors.

The ADC will be used for sensing the current through select voltage regulators, touch screen support, PMIC thermal sensor, battery voltage, current, and temperature.

Figure 49 is a representation of the ADC block.

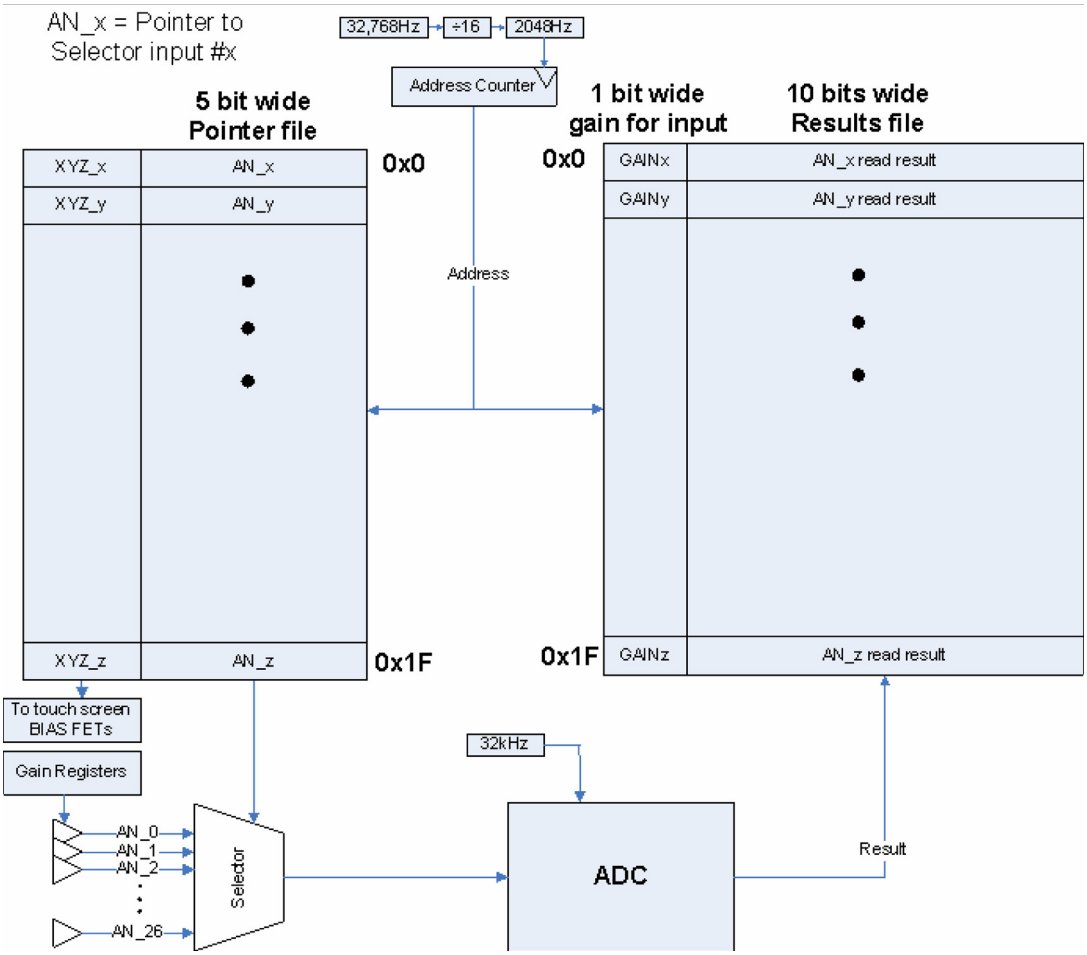


Figure 49. ADC Block Representation

INPUT SELECTOR

The ADC has 22 input channels selected through the ADSEL[4:0] bits in the ADCADDRx register. Table 57 gives an overview of the characteristics of each of these channels.

Table 57. ADC Inputs

Channel	SELECT[4:0]	ADC Input Signal	Input Level	Scaling	Scaled Version
0	00000	PMIC Die Temperature	1.2 – 2.4 V	x1	1.2 – 2.4 V
1	00001	VCC Current Sense	0 – 2.4 V	x1	0 – 2.4 V
2	00010	VNN Current Sense	0 – 2.4 V	x1	0 – 2.4 V
3	00011	VCC180 Current Sense	0 – 2.4 V	x1	0 – 2.4 V
4	00100	Reserved	Reserved	Reserved	Reserved
5	00101	Reserved	Reserved	Reserved	Reserved
6	00110	Input voltage (V_{BAT})	0 – 4.8 V	/2	0 – 2.4 V
7	00111	Reserved	Reserved	Reserved	Reserved

Table 57. ADC Inputs

Channel	SELECT[4:0]	ADC Input Signal	Input Level	Scaling	Scaled Version
8	01000	Reserved	Reserved	Reserved	Reserved
9	01001	Battery Pack Thermistor	0 – 2.4 V	x1	0– 2.4 V
10	01010	General Purpose ADIN10 Touch screen X+	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
11	01011	General Purpose ADIN11 Touch screen X-	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
12	01100	General Purpose ADIN12 Touch screen Y+	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
13	01101	General Purpose ADIN13 Touch screen Y-	0-200 mV / 0-2.0 V 0 – 1.2	10x / 1x x2	0 – 2.4 V 0 – 2.4 V
14	01110	General Purpose ADIN14	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
15	01111	General Purpose ADIN15	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
16	10000	General Purpose ADIN16	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
17	10001	General Purpose ADIN17	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
18	10010	General Purpose ADIN18	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
19	10011	General Purpose ADIN19	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
20	10100	General Purpose ADIN20	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
21	10101	General Purpose ADIN21	0-200 mV / 0-2.0 V	10x / 1x	0 – 2.4 V
22	10110	Reserved	Reserved	Reserved	Reserved
23	10111	Reserved	Reserved	Reserved	Reserved
24	11000	Reserved	Reserved	Reserved	Reserved
25	11001	Reserved	Reserved	Reserved	Reserved
26	11010	Reserved	Reserved	Reserved	Reserved
27	11011	Reserved	Reserved	Reserved	Reserved
28	11100	Reserved	Reserved	Reserved	Reserved
29	11101	Reserved	Reserved	Reserved	Reserved
30	11110	Reserved	Reserved	Reserved	Reserved
31	11111	Reserved	Reserved	Reserved	Reserved

Notes
18. Equivalent to -3.0 to +3.0 A of current with a 20 mOhm sense resistor

Some of the internal signals are first scaled to adapt the range to the input range of the ADC. Note that the 10 bit ADC core will convert over the entire scaled version of the input channel, so always from a 2.40 V, full scale.

For some applications, an external resistor divider network may be used to scale down the voltage to be measured to the ADC input range. The source resistance presented by this may be greater than the maximum specified Rs, see ADC Section on Table 3. In that case, the readout value will be lower than expected due to the dynamic input impedance of the ADC converter. This readout error presents itself as a gain error which can be compensated for by factory phasing. An alternative is to place a 100 nF bypass capacitor at the ADIN input concerned.

RESERVED CHANNELS POSSIBLE USAGE

Only 22 of the possible 32 ADC channels are currently associated with an specific function. The remaining channels are currently designated as reserved channels for future needs. Table 58 is a proposed usage for some of these channels for additional flexibility.

Table 58. Possible Reserved Channels Usage

Channel	ADC Input Signal	Input Level	Scaling	Scaled Version
22	Application Supply (V_{PWR})	0 – 4.8 V	/2	0 – 2.4 V
23	Reserved	Reserved	Reserved	Reserved
24	Reserved	Reserved	Reserved	Reserved
25	Backup Voltage ($V_{COINCELL}$)	0 – 3.6 V	x2/3	0 – 2.4 V
26	Reserved	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved	Reserved
29	Reserved	Reserved	Reserved	Reserved
30	Reserved	Reserved	Reserved	Reserved
31	Reserved	Reserved	Reserved	Reserved

Activating the prior channels to provide the signal specified occurs by asserting the following bits to 1. If the following bits are 0, then these channels are reserved:

- VPWRCON for channel 22
- LICON for channel 25

CONTROL

The ADC block consists of a 5-bit wide, 32-entry register file, which stores the address of the analog input for sampling. The 10-bit result is then stored in a separate register file 10+1 bits wide and 32 entries deep.

In order to operate the ADC, it has to be enabled first by setting the ADEN bit high in the ADCCNTL1 register. When the register ADCCNTL1 ADSTRT bit is enabled, the PMIC will cycle through the 3 + 5 bit selector addresses in registers ADCADDRx. The high 3-bits control the touch screen bias FETs, as described in Touch Screen Interface. The lower 5-bits address the ADC selector to connect one of 32 channels to the ADC. The result of the ADC conversion is stored into the result registers (ADCSNSx), along with the input gain setting (1 MSB). An address in the selector table of 0x1F designates the stop location of the selection loop. At which point the interrupt flag bit 0 (RND), which can be masked through the MRND bit in the MADCINT register, is set in register ADCINT, bit 1 of the INTERRUPT register (ADC) is set, and the external PMICINT signal is asserted, if bit 1 of the INTMASK register is clear. The ADC sleeps for 0 to 27 ms as set by ADC register ADCCNTL1 through the ADSLP[2:0] bits and then repeats the selector cycle. The new data overwrites the old in the result registers. At most, all 32 result registers will be filled within 15.625 ms (2048/32 = 1/64 Hz). The result registers will not be read until the RND flag is set.

DEDICATED CHANNELS READING

Two different LSB value settings are possible by using the LSBSEL bit in the FSLADCCNTL register. LSBSEL = 0 is the default setting. See Table 59 for more information

Table 59. ADC LSB Settings

#	SELECT[4:0]	ADC INPUT SIGNAL	SIGNAL RANGE	LSB VALUE (LSBSEL = 0)	LSB VALUE (LSBSEL = 1)
0	00000	PMIC Die Temperature	1.2 – 2.4 V	0.4244 K	1C
1	00001	VCC Current Sense	4.2 A	4.1015 mA	10 mA
2	00010	VNN Current Sense	1.9 A	1.8554 mA	10 mA
3	00011	VCC180 Current Sense	0.5 A	0.4883 mA	10 mA
4	00100	Reserved	Reserved	Reserved	Reserved
5	00101	Reserved	Reserved	Reserved	Reserved
6	00110	Battery Voltage (V_{BAT})	4.8 V	4.6875 mV	10 mV

Table 59. ADC LSB Settings

#	SELECT[4:0]	ADC INPUT SIGNAL	SIGNAL RANGE	LSB VALUE (LSBSEL = 0)	LSB VALUE (LSBSEL = 1)
7	00111	Reserved	Reserved	Reserved	Reserved
8	01000	Reserved	Reserved	Reserved	Reserved
9	01001	Battery Pack Thermistor	2.4 V	2.3438 mV	10mV
10	01010	General Purpose ADIN10 Touch screen X+	0-200 mV / 0-2.0 V 0 – 1.2	195.3 μV - 1.953 mv 1.17 mV	195.3 μV - 1.953 mv 1.17 mV
11	01011	General Purpose ADIN11 Touch screen X-	0-200 mV / 0-2.0 V 0 – 1.2	195.3 μV - 1.953 mv 1.17 mV	195.3 μV - 1.953 mv 1.17 mV
12	01100	General Purpose ADIN12 Touch screen Y+	0-200 mV / 0-2.0 V 0 – 1.2	195.3 μV - 1.953 mv 1.17 mV	195.3 μV - 1.953 mv 1.17 mV
13	01101	General Purpose ADIN13 Touch screen Y-	0-200 mV / 0-2.0 V 0 – 1.2	195.3 μV - 1.953 mv 1.17 mV	195.3 μV - 1.953 mv 1.17 mV
14	01110	General Purpose ADIN14	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
15	01111	General Purpose ADIN15	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
16	10000	General Purpose ADIN16	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
17	10001	General Purpose ADIN17	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
18	10010	General Purpose ADIN18	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
19	10011	General Purpose ADIN19	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
20	10100	General Purpose ADIN20	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
21	10101	General Purpose ADIN21	0-200 mV / 0-2.0 V	195.3 μV - 1.953 mv	195.3 μV - 1.953 mv
22	10110	Application Supply (V_{PWR})	0 – 4.8 V	4.6875 mV	4.6875 mV
23	10111	Reserved	Reserved	Reserved	Reserved
24	11000	Reserved	Reserved	Reserved	Reserved
25	11001	Backup Voltage ($V_{COINCELL}$)	0 – 3.6 V	3.5156 mV	3.5156 mV
26	11010	Reserved	Reserved	Reserved	Reserved
27	11011	Reserved	Reserved	Reserved	Reserved
28	11100	Reserved	Reserved	Reserved	Reserved
29	11101	Reserved	Reserved	Reserved	Reserved
30	11110	Reserved	Reserved	Reserved	Reserved
31	11111	Reserved	Reserved	Reserved	Reserved

PMIC DIE TEMPERATURE

The die temperature can be read out on Channel 0 of the ADC. The relation between the read out code and temperature is given in Table 60.

Table 60. PMIC Die Temperature Voltage Reading

Parameter	Typical
Die Temperature Read Out Code at 25 °C	1011000001
Temperature change per LSB	+0.4244 °C
Customer Defined LSB Value	1.0000 °C
Multiplier Value for Output Register	x2.36

CURRENT SENSING

The load current sourced by a select set of regulators can be measured and recorded by the ADC on channels 1 through 5. Table 61 shows a summary of these regulators, type, and their current ranges.

Table 61. Regulators Current Sensing

Regulator	Type	Current Range
VCC	Buck	0 – 3.5 A
VNN	Buck	0 – 1.6 A
VCC180	LDO	0 – 0.39 A

INPUT VOLTAGE

The input voltage is read at the VBAT pin at channel 6. The input voltage is first scaled by subtracting 2.40 V in order to fit the input range of the ADC.

Table 62. Battery Voltage Reading Coding

Conversion Code	Voltage at ADC input	Voltage at VBAT
1 111 111 111	2.400 V	4.800 V
1 000 010 100	1.250 V	2.500 V
0 000 000 000	0.000 V	0.000 V

GENERAL PURPOSE ANALOG INPUTS

There are twelve general purpose analog input channels that can be measured through the ADIN10-ADIN21 pins. Two voltage scaling (gain) settings can be selected to accommodate a wider range of inputs through the ADCCNTL3 and ADCCNTL4 registers. A gain of 0 sets a corresponding scaling factor of 1 (for an input range of 2.0 V) and a gain of 1 sets a corresponding scaling factor of 10 (for an input range of 200 mV).

Table 63. General Purpose Analog Inputs Reading Coding

Conversion Code	Voltage at ADC input	Voltage at ADINx Input	GAIN
1 111 111 111	2.400	0.200	1
1 011 111 111	1.800	0.150	
0 011 111 111	0.600	0.050	
0 000 000 000	0.000	0.000	
1 111 111 111	2.400	2.000	0
1 011 111 111	1.800	1.500	
0 011 111 111	0.600	0.500	
0 000 000 000	0.000	0.000	

APPLICATION SUPPLY (IF USED)

Channel 22 can be used to read the application supply voltage at the VPWR pin. This can be enabled by setting the VPWRCON bit in the FSLADCCNTL register high. The battery voltage is first scaled as VPWR/2 in order to fit the input range of the ADC.

Table 64. Application Supply Voltage Reading Coding

Conversion Code	Voltage at ADC input	Voltage at VPWR
1 111 111 111	2.400 V	4.800 V
1 000 010 100	1.250 V	2.500 V
0 000 000 000	0.000 V	0.000 V

BACKUP VOLTAGE (IF USED)

Channel 25 can be used to read the voltage of the coin cell connected to the COINCELL. This is enabled by setting the LICON bit in the FSLADCCNTL register to 1. Since the voltage range of the coin cell exceeds the input voltage range of the ADC, the COINCELL voltage is first scaled as
V_{COIN}*2/3.

Table 65. Backup (Coin Cell) Voltage Reading Coding

Conversion Code	Voltage at ADC input	Voltage at COINCELL
1 111 111 111	2.400 V	3.600 V
1 000 000 000	1.200 V	1.800 V
0 000 000 000	0.000 V	0.000 V

TOUCH SCREEN INTERFACE

The PMIC touch screen support consists of four analog input channels with built in bias control. The BIAS FET control bits are part of the ADC round robin address register ADCADDRx. The touch screen X plate is connected to ADIN10 (X+) and ADIN11 (X-), while the Y plate is connected to ADIN12(Y+) and ADIN13(Y-). A local supply, TSREF, of 1.2 V will serve as a reference.

The system processor will handle the touch screen sequencing and any necessary conversion delays. The system processor will direct the desired bias control for every reading though the ADCADDRx registers. If FET biasing is enabled though the ADCADDRx registers, then touch screen readings will start according based on the channels chosen, and also by the ADCADDRx registers. If the touch screen is not used, then the above inputs can be used as general purpose inputs. In this case, the bias control will always be programmed to no bias.

Figure 50 is a touch screen representation.

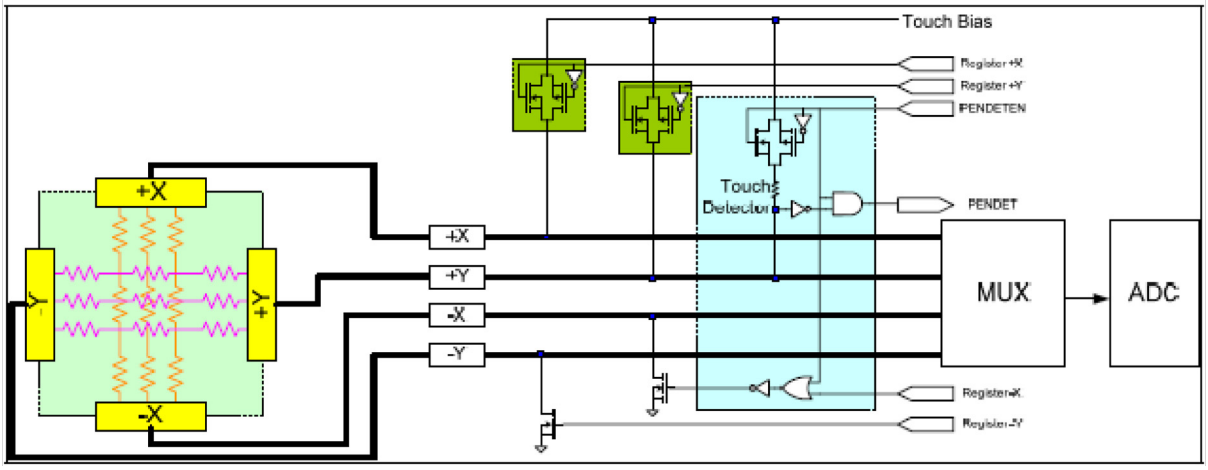


Figure 50. Touch Screen Configuration Example

900844

Touch Screen Pen detection bias can be enabled via the PENDETEN bit in the ADCCNTL1 register. When this bit is enabled and a pen touch is detected, the PENDET bit in register ADCINT is set and the PMICINT pin is asserted. This is to interrupt the system, because a touch screen pen touch has been detected at the next ADC cycle, unless the interrupt is masked.

The prior reference for the touch screen (Touch Bias) is TSREF and is powered from VCORE. In touch screen operation, TSREF is a dedicated regulator. No loads other than the touch screen should be connected here. When the ADC performs non touch screen conversions, the ADC does not rely on TSREF and the reference can be disabled.

The readouts are designed such that the on chip switch resistances are of no influence to the overall readout. The readout scheme does not account for contact resistances, as present in the touch screen connectors. Therefore, the touch screen readings have to be calibrated by the user or in the factory, where one has to point with a stylus to the opposite corners of the screen. When reading out the X-coordinate, the 10-bit ADC reading represents a 10-bit coordinate with '0' for a coordinate equal to X- and full scale '1023' when equal to X+. When reading out the Y-coordinate, the 10-bit ADC reading represents a 10-bit coordinate with '0' for a coordinate equal to Y- and full scale '1023' when equal to Y+. When reading the contact resistance the 10-bit ADC reading represents the voltage drop over the contact resistance created by the known current source multiplied by 2.

Table 66. Touch Screen System Requirements

Description	Symbol	Min	Typ	Max	Unit
Plate Resistance X, Y	-	100	-	1000	Ω
Resistance Between Plates, Contact	-	180	-	1200	Ω
Capacitance Between Plates	-	0.5	2.0	-	nF
Contact Resistance Current Source	-	-	100	-	μA
Interrupt Current Source	-	-	20	-	μA
Interrupt Threshold	-	40	-	60	kΩ
Current Source Inaccuracy	-	-	-	20	%
Quiescent Current (Active Mode)		-	20	-	μA
Max Load Current (Active Mode)		-	-	20	mA
Settling Time (Position Measurement)	-	3.0	-	5.5	μs

ADC STATUS/CONTROL REGISTERS AND BIT DESCRIPTION

Reference the Table 67 for read/write conditions and default state for each of these registers

Table 67. ADC Interrupt/Mask Registers Structure and Bits Description

Name	Bits	Description
ADCINT (ADDR 0x5F - R - Default Value: 0x00)		
RND	0	ADC Round Robin Cycle Completion Interrupt x0 = Not Completed x1 = Completed
PENDET	1	Touch Screen Pen Detection Interrupt x0 = Pen Not Detected x1 = Pen Detected
Reserved	7:2	Reserved
MADCINT (ADDR 0x60 - R/W -Default Value: 0x00)		
MRND	0	ADC Round Robin Cycle Completion Interrupt Mask x0 = Unmask x1 = Mask
MPENDET	1	Touch Screen Pen Detection Interrupt Mask x0 = Unmask x1 = Mask
Reserved	7:2	Reserved

Table 68. ADC Control Registers Structure and Bits Description

Name	Bits	Description	
ADCCNTL2 (ADDR 0x61 - R/W -Default Value: 0x00)			
ADSLP	2:0	ADC sleep time before starting another cycle	
		x0 = Continuous Loop x1 = 4.5 ms x2 = 9.0 ms x3 = 13.5 ms	x4 = 18 ms x5 = 22.5 ms x6 = 27 ms x7 = No Loop
RSVD	4:3	Reserved	
PENDETEN	5	Enable Touch Screen Pen Detect Bias x0 = Disabled x1 = Enabled	
ADSTRT	6	ADC Round Robin Start Signal x0 = Stop round robin after the current cycle x1 = Start round robin	
ADEN	7	Bring the ADC out of low power state, this overrides wake from sleep x0 = Disable in low power x1 = Enable at full power	
ADCCNTL3 (ADDR 0x62 - R/W -Default Value: 0x00)			
ADEXGAIN10	0	Gain bit for ADC channel 10, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN11	1	Gain bit for ADC channel 11, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN12	2	Gain bit for ADC channel 12, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN13	3	Gain bit for ADC channel 13, ignore when touch screen is biased x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN14	4	Gain bit for ADC channel 14 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN15	5	Gain bit for ADC channel 15 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN16	6	Gain bit for ADC channel 16 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN17	7	Gain bit for ADC channel 17 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADCCNTL4 (ADDR 0X63 - R/W -DEFAULT VALUE: 0X00)			
ADEXGAIN18	0	Gain bit for ADC channel 18 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	
ADEXGAIN19	1	Gain bit for ADC channel 19 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)	

Table 68. ADC Control Registers Structure and Bits Description

Name	Bits	Description
ADEXGAIN20	2	Gain bit for ADC channel 20 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
ADEXGAIN21	3	Gain bit for ADC channel 21 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
Reserved	7:4	Reserved

Table 69. ADC Channel Selector/Configuration Structure and bit Description

Name	Bits	Description
		ADCSNSxH (x = 0 to 31)
ADCHxH	6:0	7 MSBs of ADC result for Channel x
GAINx	7	Gain bit for ADC channel x, x = 0 to 31 x0 = x1 (0-2.0 V input range) x1 = x10 (0-200 mV input range)
		ADCSNSxL (x = 0 to 31)
ADCHxL	2:0	3 LSBs of ADC result for Channel x
Reserved	7:3	Reserved
		ADCADDRX (X = 0 TO 31)
ADSELx	4:0	ADC Channel to be read Selection bits x00 = Channel 0 x01 = Channel 1 ... x1F = Channel 31
XPXMx	5	Turns on X+ and X- bias FETs, Refer to Figure 50 x0 = FETS Off x1 = FETS On
YPYMx	6	Turns on Y+ and Y- bias FETs, Refer to Figure 50 x0 = FETS Off x1 = FETS On
XMYPx	7	Turns on X- and Y+ bias FETs, Refer to Figure 50 x0 = FETS Off x1 = FETS On

ADC STATUS/CONTROL REGISTERS AND BIT DESCRIPTION

Table 70. Extended ADC Control Register Structure and Bits Description

Name	Bits	Description
FSLADCCNTL (ADDR 0x1DE - R/W - Default Value: 0x00)		
VPWRCON	0	Enable channel 22 to read the V_{PWR} voltage x0 = Disable (Default) x1 = Enable
CHRGICON	1	Enable channel 24 to read the Battery charging current x0 = Disable (Default) x1 = Enable
LICON	2	Enable channel 25 to read the Backup Battery voltage x0 = Disable (Default) x1 = Enable
RSVD	3	Reserved
LSBSEL	4	ADC LSB Selection Bit x0 = Refer to Table 59 x1 = Refer to Table 59
RSVD	7:4	Reserved

GPIOS

DESCRIPTION

The 900844 has eight GPIOs, and eight GPOs for platform control.

As outputs, the GPIOs support CMOS/OD signaling levels, based on the voltage level on the GPIOVCC. The GPOs support CMOS signaling levels, based on the voltage level on the GPOVCC pin. As inputs, they are 3.6 V tolerant and are de-bounced for a period of no more than 10 ms minimum.

The 900844 provides one bank of eight configurable GPIO inputs/outputs, GPIO[7:0] for general purpose sensing and platform control. Only GPIOs support an input function.

GPIOs switch between a high-impedance (>1.0 MΩ) state and a low-impedance (20 Ω nominal) state when operating in open drain mode. When operating in CMOS mode, the outputs drive from the voltage supplied on the GPIOVCC pin with a 20 Ω output drive capability (for GPIOs).

The electrical characteristics of the output buffer will therefore be specified as relative percentages of the driving supply.

Any unused GPIO pin should be tied to ground on the board.

When any GPIO is configured as an open drain, the pull-up voltage cannot exceed that of the GPIOVCC Voltage level.

Table 71 shows the default state of the different GPIOs and their capabilities.

Table 71. GPIOs Capabilities and Default States

GPIO	Input	Output	CMOS	OD	Slew CNTL	Default Mode	Default Level
GPIO0	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO1	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO2	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO3	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO4	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO5	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO6	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPIO7	Yes	Yes	Yes	Yes	No	Input	HI-Z
GPO0	No	Yes	Yes	No	No	CMOS	Low
GPO1	No	Yes	Yes	No	No	CMOS	Low

Table 71. GPIOs Capabilities and Default States

GPIO	Input	Output	CMOS	OD	Slew CNTL	Default Mode	Default Level
GPO2	No	Yes	Yes	No	No	CMOS	Low
GPO3	No	Yes	Yes	No	No	CMOS	Low
GPO4	No	Yes	Yes	No	No	CMOS	Low
GPO5	No	Yes	Yes	No	No	CMOS	Low
GPO6	No	Yes	Yes	No	No	CMOS	Low
GPO7	No	Yes	Yes	No	No	CMOS	Low

GPIO MODULE STRUCTURE

Figure 51 illustrates the logical structure of the GPIOx modules.

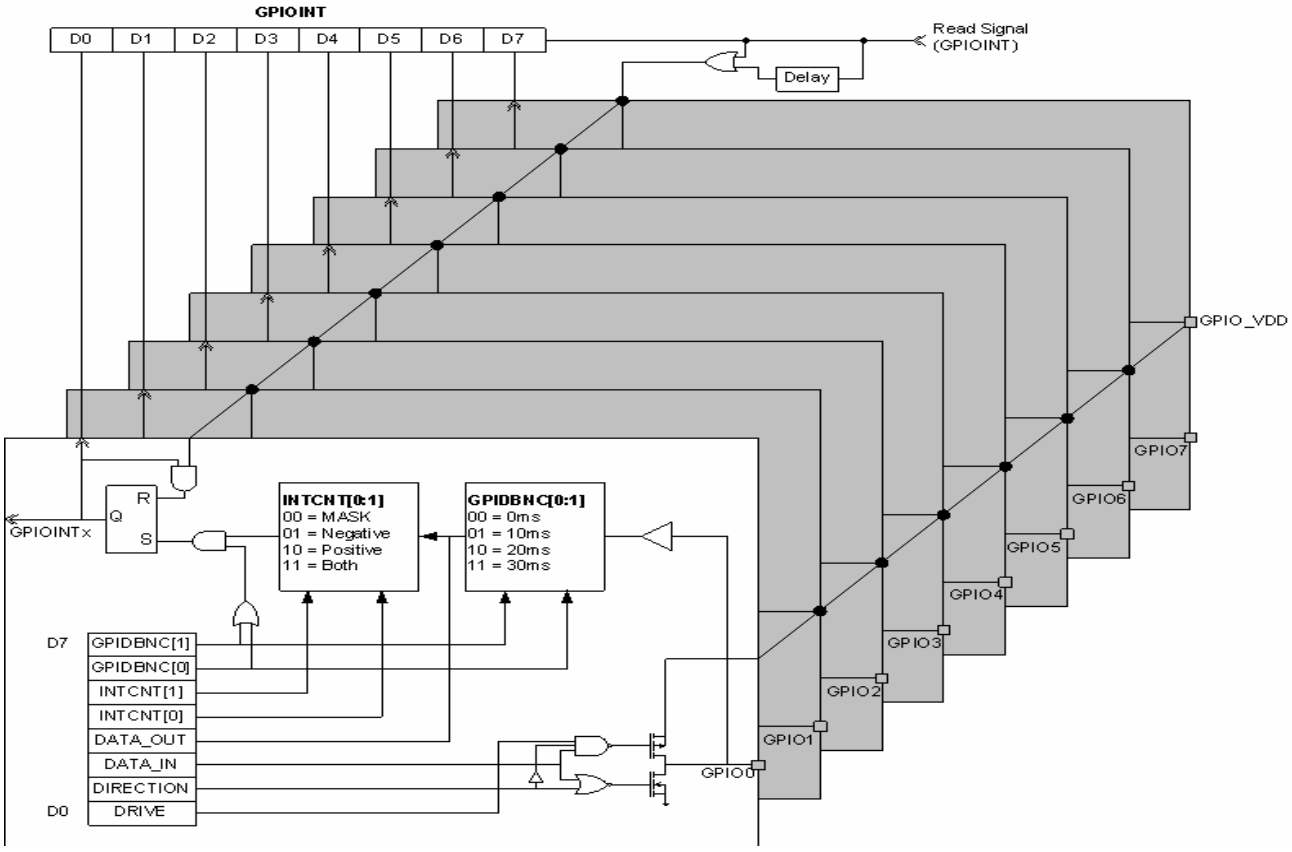


Figure 51. GPIO Module Structure

GPIO STATUS/CONTROL REGISTERS AND BIT DESCRIPTION

GPIO module has a single 8-bit status and control register assigned to it. See Table 72 for details.

The “x” in the bit names in the tables is from 0 to 7 for the GPIOs.

Table 72. GPIO Register Structure and Bits Description

Name	Bits	Description
		GPIOCNTLx (x = 0 to 7)
DRVx	0	GPIOx Output Driver Type x0 = Open Drain x1 = CMOS
DIRx	1	GPIOx Direction Configuration x0 = Output (Type selected by Bit 0) x1 = Input (Bit 0 is ignored)
DATAINx	2	The value in the DATA_IN bit reflects the electrical state of the GPIOx pin at the time the register read was initiated. When Bit 1, DIRECTION, is 0 (Output Mode), the contents of this register are not required to be updated on reads and is assumed to be invalid by the system controller. The PMIC should de-bounce the inputs over 1-10 ms to insure a clean transition. X0 = Electrical Low (19) x1 = Electrical High (19)
DATAOUTx	3	The value in the DATA_OUT bit reflects the desired electrical output state of the GPIOx pin. When Bit 1, DIRECTION, is 1 (Input Mode), the contents of this register may still be read or written, but will not be reflected until the GPIOx is reverted to an output (Bit 1, DIRECTION, is 0) x0 = Electrical Low (19) x1 = Electrical High (CMOS) or High-impedance Output (Open-Drain) (19)
INTCTLx	5:4	These bits set the interrupt definition. The MASK (00) determines if the corresponding interrupt flag bit is set or not on an interrupt. The other logic levels will set the corresponding interrupt flag bit in the register upon the specific edge detection defined by the level. They will also set bit 4 of the 1st level INTERRUPT register, see section Interrupt Controller for more details. (20) x0 = Mask. x1 = Negative Edge x2 = Positive Edge x3 = Both Edges
GPIDBNCx	7:6	These bits set the debounce time on the GPIOx when configured as inputs x0 = No Debounce x1 = 10 ms x2 = 20 ms x3 = 30 ms
		GPIOINT (ADDR 0xE8 - R - Default Value: 0x00)
GPIINT0	0	GPIO0 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT1	1	GPIO1 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT2	2	GPIO2 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT3	3	GPIO3 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred

Notes

19. See GPIOs electrical characteristics on Table 3
20. An unintended interrupt is caused if interrupt settings are reconfigured in the middle of an application, e.g. re-setting interrupt detection from detecting an interrupt on both edges to an interrupt on the rising edge. In this case, to mask any unwanted interrupt, change the GPIO interrupt detection to the new configuration, then clear Level 1 and level 2 interrupts, finally unmask the GPIO Interrupt.

Table 72. GPIO Register Structure and Bits Description

Name	Bits	Description
GPIINT4	4	GPIO4 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT5	5	GPIO5 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT6	6	GPIO6 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred
GPIINT7	7	GPIO7 Interrupt Flag x0 = No Interrupt occurred or Masked Interrupt x1 = Interrupt occurred

Table 73. GPO Register Structure and Bits Description

Name	Bits	Description
		GPO (ADDR 0xF4 - R/W - Default Value: 0x00)
GPO0	0	GPO0 Output Level x0 = Low0 x1 = High (To voltage supplied on GPOVCC Pin)
GPO1	1	GPO1 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO2	2	GPO2 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO3	3	GPO3 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO4	4	GPO4 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO5	5	GPO5 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO6	6	GPO6 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)
GPO7	7	GPO7 Output Level x0 = Low x1 = High (To voltage supplied on GPOVCC Pin)

SPI REGISTER MAP

OVERVIEW

The SPI frame is organized as 24 bits. The first 16 bits is the write enable bit, 10-bit address and 5 "dead" bits between the data and address fields. The next 8 bits are the data bits. The one write enable bit selects whether the SPI transaction is a read or a write.

The addressable register map spans 1024 registers of 8 data bits each. The map is not fully populated. A summarized structure of the register set is given in the following tables. Expanded bit descriptions are included in the individual functional sections for application guidance.

SPI BIT MAP

The tables include the following fields:

- Block: This corresponds directly to the chapter, section or topic in which the detailed register description is included.
- Address: The register memory map address allocation in HEX format
- Register Name
- R/W: Defines if the register is a Read/Write register or only a Read register
- D7-D0: The 8-bit data included in the register with each bit's name and location within the field included
- Initial: The register's default value after power up
- Function: A short description of the register's function

Some important notes about data in the table:

- Reserved registers/bits are not implemented in the design and they will always read as a 0
- Registers under the "FSL" block are Freescale dedicated registers and are not defined in the customer specifications. These registers represent additional functionality that Freescale is offering to enhance the performance of the overall system
- Registers under the "VD2" and "VD3" blocks are blocked from being used by Freescale
- The table only displays up to address 0x2FF. Address space between 0x300 and 0x3FF is reserved for future application use. Freescale is currently using the 0x300 to 0x3FF space for test and debug register implementation. This will not effect the application or any future use plans for this address space. The details of this space implementation are not discussed in this document.

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
Chip1	0x00	ID1	R	RSVD	RSVD	REV1[2:0]			VENDID1[2:0]			0x38	Chip1 ID
Chip2	0x01	ID2	R	RSVD	RSVD	REV2[2:0]			VENDID2[2:0]			0x00	Chip2 ID
Chip3	0x02	ID3	R	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Chip3 ID
Chip4	0x03	ID4	R	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Chip4 ID
IRQ	0x04	INTERRUPT	R	EXT	AUX	VRFAULT	GPIO	RTC	CHR	ADC	PWRBTN	0x00	PMIC_INT sources, read clears
IRQ	0x05	INTMASK	R/W	MEXT	MAUX	MVRFAULT	MGPIO	MRTC	MCHR	MADC	MPWRBTN	0xFA	IRQ mask
CNTRL	0x06	CHIPCNTRL	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	WARMRST	COLDRST	0x00	PWRGD/RESET# control
RSVD	0x07	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x08	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x09	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0A	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0B	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0C	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0D	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0E	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x0F	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RTC	0x10	RTCS	R/W	RSVD	SEC[6:0]							0x00	RTC Second
RTC	0x11	RTCSA	R/W	RSVD	SECALARM[6:0]							0x00	RTC Second Alarm
RTC	0x12	RTCM1	R/W	RSVD	MIN[6:0]							0x00	RTC Minutes
RTC	0x13	RTCMA	R/W	RSVD	MINIALARM[6:0]							0x00	RTC Minutes Alarm
RTC	0x14	RTCH	R/W	PA-H	RSVD	HRS[5:0]						0x00	RTC Hours
RTC	0x15	RTCHA	R/W	PA-HA	RSVD	HRSALARM[5:0]						0x00	RTC Hours Alarm
RTC	0x16	RTCDW	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	DOW[2:0]			0x01	RTC Day Of Week
RTC	0x17	RTCDM	R/W	RSVD	RSVD	DOM[5:0]						0x01	RTC Day Of Month
RTC	0x18	RTCM2	R/W	19/20	RSVD	RSVD	MONTH[4:0]					0x01	RTC Month

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
RTC	0x19	RTCY	R/W	YEAR[7:0]								0x00	RTC
RTC	0x1A	RTCA	R	UIP	DV[2:0] (=010b FIXED)			RS[3:0] (=000b FIXED)				0x20	RTC Control A
RTC	0x1B	RTCB	R/W	SET	PIE (=0) FIX	AIE	UIE	SQWE (=0) FIX	DM	HRMODE	DSE (=0) FIX	0x02	RTC Control B
RTC	0x1C	RTCC	R	IRQF	PF (=0) FIX	AF	UF	RSVD	RSVD	RSVD	RSVD	0x00	RTC Control C
RTC	0x1D	RTCD	R	VRT	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RTC Control D
RTC	0x1E	RTCE	R/W	SCRATCH[4:0]					POR	BKDET	OSCST	0x05	RTC Optional Detection
RTC	0x1F	ADJ	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ADJ	0x00	RTC Adjustment
RTC	0x20	TRIM	R/W	RSVD	SIGN	TRIMVAL[5:0]						0x00	RTC Trimming
RTC	0x21	CLKOUT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	M32KCLK	0x00	32kHz clock output enable
RSVD	0x22-0x2F	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
POWER	0x30	VRFAULTINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	VRFAIL	BATOCP	THRM	0x00	Voltage Regulators Fault interrupt
POWER	0x31	MVRFAULTINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MVRFAIL	MBATOCP	MTHRM	0x03	Voltage Regulators Fault interrupt Mask
POWER	0x32	VCCLATCH	R/W	DVP1VRD	VIDVCC[6:0]							0x7F	VCC VID CONTROL
POWER	0x33	VNNLATCH	R/W	DVP2VRD	VIDVNN[6:0]							0x7F	VNN VID CONTROL
POWER	0x34	PWRMASK	R/W	M7	M6	M5	M4	M3	M2	M1	M0	0x00	Power register write mask
POWER	0x35	VCCCNT	R/W	RSVD	RSVD	AOACTLVCC[2:0]			CTLVCC[2:0]			0x24	VCC
POWER	0x36	VNNCNT	R/W	RSVD	RSVD	AOACTLVNN[2:0]			CTLVNN[2:0]			0x04	VNN
POWER	0x37	VDDQCNT	R/W	RSVD	RSVD	AOACTLVDDQ[2:0]			CTLVDDQ[2:0]			0x04	VDDQ
POWER	0x38	V21CNT	R/W	RSVD	RSVD	AOACTLV21[2:0]			CTLV21[2:0]			0x07	V21
POWER	0x39	V15CNT	R/W	SELV15[1:0]		AOACTLV15[2:0]			CTLV15[2:0]			0x07	V15
RSVD	0x3A	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
RSVD	0x3B	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
RSVD	0x3C	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
POWER	0x3D	VCCPAOACCNT	R/W	RSVD	RSVD	AOACTLVCCPAOAC[2:0]			CTLVCCPAOAC[2:0]			0x07	VCCPAOAC
POWER	0x3E	VCCPDDRCNT	R/W	RSVD	RSVD	AOACTLVCCPDDR[2:0]			CTLVCCPDDR[2:0]			0x3C	VCCPDDR
POWER	0x3F	VLBGCNT	R/W	RSVD	RSVD	AOACTLVLBG[2:0]			CTLVLBG[2:0]			0x24	VLBG
POWER	0x40	VCCACNT	R/W	RSVD	RSVD	AOACTLVCCA[2:0]			CTLVCCA[2:0]			0x3C	VCCA
POWER	0x41	VPMICCNT	R/W	RSVD	RSVD	AOACTLVPMIC[2:0]			CTLVPMIC[2:0]			0x07	VPMIC
POWER	0x42	VIMG25CNT	R/W	RSVD	RSVD	AOACTLVIMG25[2:0]			CTLVIMG25[2:0]			0x04	VIMG25
POWER	0x43	VCC180CNT	R/W	RSVD	RSVD	AOACTLVCC180[2:0]			CTLVCC180[2:0]			0x3C	VCC180
POWER	0x44	VCCPCNT	R/W	RSVD	RSVD	AOACTLVCCP[2:0]			CTLVCCP[2:0]			0x3C	VCCP
POWER	0x45	VAONCNT	R/W	RSVD	RSVD	AOACTLVAON[2:0]			CTLVAON[2:0]			0x07	VAON
POWER	0x46	VPANEL18CNT	R/W	RSVD	RSVD	AOACTLVPANEL18[2:0]			CTLVPANEL18[2:0]			0x24	VPANEL18
POWER	0x47	VMMCNT	R/W	RSVD	RSVD	AOACTLVMM[2:0]			CTLVMM[2:0]			0x24	VMM
POWER	0x48	VIMGACNT	R/W	SELIMGA[1:0]		AOACTLVIMGA[2:0]			CTLVIMGA[2:0]			0x24	VIMGA
RSVD	0x49	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
RSVD	0x4A	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
RSVD	0x4B	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
POWER	0x4C	VWYMXARFCNT	R/W	RSVD	RSVD	AOACTLVWYMXARF[2:0]			CTLVWYMXARF[2:0]			0x24	WiFiBT_YMX_ANALOGRF

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
POWER	0x4D	VSDIOCNT	R/W	SELVSDIO[1:0]		AOACTLVSDIO[2:0]			CTLVSDIO[2:0]			0x64	VSDIO
RSVD	0x4E	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
POWER	0x4F	VPANEL33CNT	R/W	RSVD	RSVD	AOACTLVPANEL33[2:0]			CTLVPANEL33[2:0]			0x24	VCC_PANEL_3.3
RSVD	0x50	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
RSVD	0x51	RSVD	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	RSVD
RSVD	0x52	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x53	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x54	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
MEMORY	0x55	MEM1	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x56	MEM2	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x57	MEM3	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x58	MEM4	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x59	MEM5	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x5A	MEM6	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x5B	MEM7	R/W	SCRATCH[7:0]								0x00	Backup memory
MEMORY	0x5C	MEM8	R/W	SCRATCH[7:0]								0x00	Backup memory
RSVD	0x5D	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0x5E	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
ADC	0x5F	ADCINT	R	RSVD	RSVD	RSVD	RSVD	RSVD	OVERFLOW	PENDET	RND	0x00	ADC interrupt
ADC	0x60	MADCINT	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	MOVERFLOW	MPENDET	MRND	0x00	ADC interrupt Mask
ADC	0x61	ADCCNTL2	R/W	ADEN	ADSTRT	PENDETEN	CCCLEAR	CCEN	ADSLP[2:0]			0x00	ADC control
ADC	0x62	ADCCNTL3	R/W	ADEXGAIN17	ADEXGAIN16	ADEXGAIN15	ADEXGAIN14	ADEXGAIN13	ADEXGAIN12	ADEXGAIN11	ADEXGAIN10	0x00	GAIN for AN10-AN17
ADC	0x63	ADCCNTL4	R/W	RSVD	RSVD	RSVD	RSVD	ADEXGAIN21	ADEXGAIN20	ADEXGAIN19	ADEXGAIN18	0x00	GAIN for AN18-AN21
ADC	0x64	ADCSNS0H	R	GAIN0	ADCH0H[9:3]							0x00	ADC result
ADC	0x65	ADCSNS0L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH0L[2:0]			0x00	ADC result
ADC	0x66	ADCSNS1H	R	GAIN1	ADCH1H[9:3]							0x00	ADC result
ADC	0x67	ADCSNS1L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH1L[2:0]			0x00	ADC result
ADC	0x68	ADCSNS2H	R	GAIN2	ADCH2H[9:3]							0x00	ADC result
ADC	0x69	ADCSNS2L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH2L[2:0]			0x00	ADC result
ADC	0x6A	ADCSNS3H	R	GAIN3	ADCH3H[9:3]							0x00	ADC result
ADC	0x6B	ADCSNS3L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH3L[2:0]			0x00	ADC result
ADC	0x6C	ADCSNS4H	R	GAIN4	ADCH4H[9:3]							0x00	ADC result
ADC	0x6D	ADCSNS4L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH4L[2:0]			0x00	ADC result
ADC	0x6E	ADCSNS5H	R	GAIN5	ADCH5H[9:3]							0x00	ADC result
ADC	0x6F	ADCSNS5L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH5L[2:0]			0x00	ADC result
ADC	0x70	ADCSNS6H	R	GAIN6	ADCH6H[9:3]							0x00	ADC result
ADC	0x71	ADCSNS6L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH6L[2:0]			0x00	ADC result
ADC	0x72	ADCSNS7H	R	GAIN7	ADCH7H[9:3]							0x00	ADC result
ADC	0x73	ADCSNS7L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH7L[2:0]			0x00	ADC result
ADC	0x74	ADCSNS8H	R	GAIN8	ADCH8H[9:3]							0x00	ADC result
ADC	0x75	ADCSNS8L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH8L[2:0]			0x00	ADC result
ADC	0x76	ADCSNS9H	R	GAIN9	ADCH9H[9:3]							0x00	ADC result

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
ADC	0x77	ADCSNS9L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH9L[2:0]			0x00	ADC result
ADC	0x78	ADCSNS10H	R	GAIN10	ADCH10H[9:3]							0x00	ADC result
ADC	0x79	ADCSNS10L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH10L[2:0]			0x00	ADC result
ADC	0x7A	ADCSNS11H	R	GAIN11	ADCH11H[9:3]							0x00	ADC result
ADC	0x7B	ADCSNS11L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH11L[2:0]			0x00	ADC result
ADC	0x7C	ADCSNS12H	R	GAIN12	ADCH12H[9:3]							0x00	ADC result
ADC	0x7D	ADCSNS12L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH12L[2:0]			0x00	ADC result
ADC	0x7E	ADCSNS13H	R	GAIN13	ADCH13H[9:3]							0x00	ADC result
ADC	0x7F	ADCSNS13L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH13L[2:0]			0x00	ADC result
ADC	0x80	ADCSNS14H	R	GAIN14	ADCH14H[9:3]							0x00	ADC result
ADC	0x81	ADCSNS14L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH14L[2:0]			0x00	ADC result
ADC	0x82	ADCSNS15H	R	GAIN15	ADCH15H[9:3]							0x00	ADC result
ADC	0x83	ADCSNS15L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH15L[2:0]			0x00	ADC result
ADC	0x84	ADCSNS16H	R	GAIN16	ADCH16H[9:3]							0x00	ADC result
ADC	0x85	ADCSNS16L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH16L[2:0]			0x00	ADC result
ADC	0x86	ADCSNS17H	R	GAIN17	ADCH17H[9:3]							0x00	ADC result
ADC	0x87	ADCSNS17L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH17L[2:0]			0x00	ADC result
ADC	0x88	ADCSNS18H	R	GAIN18	ADCH18H[9:3]							0x00	ADC result
ADC	0x89	ADCSNS18L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH18L[2:0]			0x00	ADC result
ADC	0x8A	ADCSNS19H	R	GAIN19	ADCH19H[9:3]							0x00	ADC result
ADC	0x8B	ADCSNS19L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH19L[2:0]			0x00	ADC result
ADC	0x8C	ADCSNS20H	R	GAIN20	ADCH20H[9:3]							0x00	ADC result
ADC	0x8D	ADCSNS20L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH20L[2:0]			0x00	ADC result
ADC	0x8E	ADCSNS21H	R	GAIN21	ADCH21H[9:3]							0x00	ADC result
ADC	0x8F	ADCSNS21L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH21L[2:0]			0x00	ADC result
ADC	0x90	ADCSNS22H	R	GAIN22	ADCH22H[9:3]							0x00	ADC result
ADC	0x91	ADCSNS22L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH22L[2:0]			0x00	ADC result
ADC	0x92	ADCSNS23H	R	GAIN23	ADCH23H[9:3]							0x00	ADC result
ADC	0x93	ADCSNS23L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH23L[2:0]			0x00	ADC result
ADC	0x94	ADCSNS24H	R	GAIN24	ADCH24H[9:3]							0x00	ADC result
ADC	0x95	ADCSNS24L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH24L[2:0]			0x00	ADC result
ADC	0x96	ADCSNS25H	R	GAIN25	ADCH25H[9:3]							0x00	ADC result
ADC	0x97	ADCSNS25L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH25L[2:0]			0x00	ADC result
ADC	0x98	ADCSNS26H	R	GAIN26	ADCH26H[9:3]							0x00	ADC result
ADC	0x99	ADCSNS26L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH26L[2:0]			0x00	ADC result
ADC	0x9A	ADCSNS27H	R	GAIN27	ADCH27H[9:3]							0x00	ADC result
ADC	0x9B	ADCSNS27L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH27L[2:0]			0x00	ADC result
ADC	0x9C	ADCSNS28H	R	GAIN28	ADCH28H[9:3]							0x00	ADC result
ADC	0x9D	ADCSNS28L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH28L[2:0]			0x00	ADC result
ADC	0x9E	ADCSNS29H	R	GAIN29	ADCH29H[9:3]							0x00	ADC result
ADC	0x9F	ADCSNS29L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH29L[2:0]			0x00	ADC result
ADC	0xA0	ADCSNS30H	R	GAIN30	ADCH30H[9:3]							0x00	ADC result
ADC	0xA1	ADCSNS30L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH30L[2:0]			0x00	ADC result
ADC	0xA2	ADCSNS31H	R	GAIN31	ADCH31H[9:3]							0x00	ADC result
ADC	0xA3	ADCSNS31L	R	RSVD	RSVD	RSVD	RSVD	RSVD	ADCH31L[2:0]			0x00	ADC result

900844

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
ADC	0xA4	ADCADDR0	R/W	XMYP0	YPYM0	XPXM0	ADSEL0[4:0]					0x00	ADC selector address
ADC	0xA5	ADCADDR1	R/W	XMYP1	YPYM1	XPXM1	ADSEL1[4:0]					0x00	ADC selector address
ADC	0xA6	ADCADDR2	R/W	XMYP2	YPYM2	XPXM2	ADSEL2[4:0]					0x00	ADC selector address
ADC	0xA7	ADCADDR3	R/W	XMYP3	YPYM3	XPXM3	ADSEL3[4:0]					0x00	ADC selector address
ADC	0xA8	ADCADDR4	R/W	XMYP4	YPYM4	XPXM4	ADSEL4[4:0]					0x00	ADC selector address
ADC	0xA9	ADCADDR5	R/W	XMYP5	YPYM5	XPXM5	ADSEL5[4:0]					0x00	ADC selector address
ADC	0xAA	ADCADDR6	R/W	XMYP6	YPYM6	XPXM6	ADSEL6[4:0]					0x00	ADC selector address
ADC	0xAB	ADCADDR7	R/W	XMYP7	YPYM7	XPXM7	ADSEL7[4:0]					0x00	ADC selector address
ADC	0xAC	ADCADDR8	R/W	XMYP8	YPYM8	XPXM8	ADSEL8[4:0]					0x00	ADC selector address
ADC	0xAD	ADCADDR9	R/W	XMYP9	YPYM9	XPXM9	ADSEL9[4:0]					0x00	ADC selector address
ADC	0xAE	ADCADDR10	R/W	XMYP10	YPYM10	XPXM10	ADSEL10[4:0]					0x00	ADC selector address
ADC	0xAF	ADCADDR11	R/W	XMYP11	YPYM11	XPXM11	ADSEL11[4:0]					0x00	ADC selector address
ADC	0xB0	ADCADDR12	R/W	XMYP12	YPYM12	XPXM12	ADSEL12[4:0]					0x00	ADC selector address
ADC	0xB1	ADCADDR13	R/W	XMYP13	YPYM13	XPXM13	ADSEL13[4:0]					0x00	ADC selector address
ADC	0xB2	ADCADDR14	R/W	XMYP14	YPYM14	XPXM14	ADSEL14[4:0]					0x00	ADC selector address
ADC	0xB3	ADCADDR15	R/W	XMYP15	YPYM15	XPXM15	ADSEL15[4:0]					0x00	ADC selector address
ADC	0xB4	ADCADDR16	R/W	XMYP16	YPYM16	XPXM16	ADSEL16[4:0]					0x00	ADC selector address
ADC	0xB5	ADCADDR17	R/W	XMYP17	YPYM17	XPXM17	ADSEL17[4:0]					0x00	ADC selector address
ADC	0xB6	ADCADDR18	R/W	XMYP18	YPYM18	XPXM18	ADSEL18[4:0]					0x00	ADC selector address
ADC	0xB7	ADCADDR19	R/W	XMYP19	YPYM19	XPXM19	ADSEL19[4:0]					0x00	ADC selector address
ADC	0xB8	ADCADDR20	R/W	XMYP20	YPYM20	XPXM20	ADSEL20[4:0]					0x00	ADC selector address
ADC	0xB9	ADCADDR21	R/W	XMYP21	YPYM21	XPXM21	ADSEL21[4:0]					0x00	ADC selector address
ADC	0xBA	ADCADDR22	R/W	XMYP22	YPYM22	XPXM22	ADSEL22[4:0]					0x00	ADC selector address
ADC	0xBB	ADCADDR23	R/W	XMYP23	YPYM23	XPXM23	ADSEL23[4:0]					0x00	ADC selector address
ADC	0xBC	ADCADDR24	R/W	XMYP24	YPYM24	XPXM24	ADSEL24[4:0]					0x00	ADC selector address
ADC	0xBD	ADCADDR25	R/W	XMYP25	YPYM25	XPXM25	ADSEL25[4:0]					0x00	ADC selector address
ADC	0xBE	ADCADDR26	R/W	XMYP26	YPYM26	XPXM26	ADSEL26[4:0]					0x00	ADC selector address
ADC	0xBF	ADCADDR27	R/W	XMYP27	YPYM27	XPXM27	ADSEL27[4:0]					0x00	ADC selector address
ADC	0xC0	ADCADDR28	R/W	XMYP28	YPYM28	XPXM28	ADSEL28[4:0]					0x00	ADC selector address
ADC	0xC1	ADCADDR29	R/W	XMYP29	YPYM29	XPXM29	ADSEL29[4:0]					0x00	ADC selector address

900844

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
ADC	0xC2	ADCADDR30	R/W	XMYP30	YPYM30	XPXM30	ADSEL30[4:0]					0x00	ADC selector address
ADC	0xC3	ADCADDR31	R/W	XMYP31	YPYM31	XPXM31	ADSEL31[4:0]					0x00	ADC selector address
RSVD	0xC4	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC5	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC8	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xC9	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCB	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCC	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCE	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xCF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
CHARGER	0xD0	CHRGINT	R	RSVD	RSVD	BATDET	RSVD	RSVD	TEMP	BATOVP	RSVD	0x00	Charger Interrupt
CHARGER	0xD1	MCHRGINT	R/W	RSVD	RSVD	MBATDET	RSVD	RSVD	MTEMP	MBATOVP	RSVD	0x00	Charger Interrupt Mask
CHARGER	0xD2	SCHRGINT	R	RSVD	RSVD	SBATDET	RSVD	RSVD	STEMP	SBATOVP	RSVD	0x00	Charger State
CHARGER	0xD3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xD4	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xD5	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xD6	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xD7	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xD8	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xD9	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDA	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDB	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDC	RSVD	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDE	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xDF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
GPIO	0xE0	GPIOCNTL0	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE1	GPIOCNTL1	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE2	GPIOCNTL2	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE3	GPIOCNTL3	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE4	GPIOCNTL4	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE5	GPIOCNTL5	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE6	GPIOCNTL6	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE7	GPIOCNTL7	R/W	GPIDBNC0[1:0]		INTCTL0[1:0]		DATAOUT0	DATAIN0	DIR0	DRV0	0x03	GPIO control
GPIO	0xE8	GPIOINT	R	GPIINT7	GPIINT6	GPIINT5	GPIINT4	GPIINT3	GPIINT2	GPIINT1	GPIINT0	0x00	GPIO Interrupt
RSVD	0xE9	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xEA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xEB	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
RSVD	0xEC	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xED	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xEE	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xEF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF0	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF1	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
GPIO	0xF4	GPO	R/W	GPO7	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1	GPO0	0x00	GPO control
RSVD	0xF5	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
RSVD	0xF8	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
VD2	0xF9 - 0xFF	-	-	VD2								-	Reserved
VD3	0x100 - 0x132	-	-	VD3								-	Reserved
RSVD	0x133 - 0x199	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19A	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19B	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19C	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19D	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19E	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x19F	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A0	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A1	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A4	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A5	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A8	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1A9	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AB	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AC	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1AE	FSLMEM1	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1AF	FSLMEM2	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B0	FSLMEM3	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B1	FSLMEM4	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B2	FSLMEM5	R/W	SCRATCH[7:0]								0x00	Backup memory

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
FSL	0x1B3	FSLMEM6	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B4	FSLMEM7	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B5	FSLMEM8	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B6	FSLMEM9	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B7	FSLMEM10	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B8	FSLMEM11	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1B9	FSLMEM12	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BA	FSLMEM13	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BB	FSLMEM14	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BC	FSLMEM15	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BD	FSLMEM16	R/W	SCRATCH[7:0]								0x00	Backup memory
FSL	0x1BE	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1BF	FSLOUTDRVCNTL1	R/W	RESETBDRV[1:0]		PMICINTDRV[1:0]		VRCOMPBDRV[1:0]		PWRGDDRV[1:0]		0x00	Digital Outputs Drive Strength
FSL	0x1C0	FSLOUTDRVCNTL2	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CLK32KDRV[1:0]		0x04	Digital Outputs Drive Strength
FSL	0x1C1	FSLOUTDRVCNTL3	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SPISDODRV		0x01	Digital Outputs Drive Strength
FSL	0x1C2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C4	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C5	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1C8	FSLTONTCNTL1	R/W	RSVD	RSVD	VDDQTONT		VNNTONT		VCCTONT		0xAA	Buck Turn On time control (DVS Clk)
FSL	0x1C9	FSLVCCLATCH	R	RSVD	VIDVCC[6:0]							0x7F	VCC VID CONTROL
FSL	0x1CA	FSLVNNLATCH	R	RSVD	VIDVNN[6:0]							0x7F	VNN VID CONTROL
FSL	0x1CB	FSLTONTCNTL2	R/W	RSVD	RSVD	RSVD	RSVD	V15TONT	RSVD	V21TONT	RSVD	0xAA	Buck Turn On time control (DVS Clk)
FSL	0x1CC	FSLFAULT1	R	RSVD	RSVD	RSVD	V15FAULT	V21FAULT	VDDQFAULT	VNNFAULT	VCCFAULT	0x00	Regulator Fault Flag
FSL	0x1CD	FSLFAULT2	R	VPMICFAULT	VPNL18FAULT	VCC180FAULT	VCCAFAULT	VBGFAULT	RSVD	RSVD	RSVD	0x00	Regulator Fault Flag
FSL	0x1CE	FSLFAULT3	R	VCCPFAULT	VMMFAULT	VAONFAULT	VCCPDDRFAULT	VCCPAOACFAULT	RSVD	RSVD	VYMXYFI18FAULT	0x00	Regulator Fault Flag
FSL	0x1CF	FSLFAULT4	R	RSVD	RSVD	RSVD	RSVD	VSDIOFAULT	RSVD	VIMG28FAULT	VIMG25FAULT	0x00	Regulator Fault Flag
FSL	0x1D0	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D1	FSLCHRGCNTL	R/W	RSVD	RSVD	RSVD	VCOIN[4:2]			COINCHEN	CHGBYP	0x13	Charger Control
FSL	0x1D2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D4	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D5	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D6	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D7	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1D8	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved

Table 74. SPI Register Map

Block	Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Function
FSL	0x1D9	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1DA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1DB	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1DC	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1DD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1DE	FSLADCCNTL	R/W	RSVD	TSPAS	ADCCAL	LSBSEL	BATDETVCON	LICON	CHRGICON	VPWRCON	0x00	ADC Spare Channel Control
FSL	0x1DF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1E0	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1E1	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1E2	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1E3	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1E4	FSLPLLCNTL	R/W	RSVD	RSVD	RSVD	PLLEN	PLL16MEN	PLLDIVIDE[2:0]			0x1B	Reserved
RSVD	0x1E5 - 0x1FA	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1FB	BUCK_TOP_LVSH_5	R/W	BUCK_V15_EN	BUCK_V15_PWRSTG_EN<6:0>							0x7F	Switching Regulator Debug
FSL	0x1FC	BUCK_TOP_LVSH_4	R/W	BUCK_V21_EN	BUCK_V21_PWRSTG_EN<6:0>							0x7F	Switching Regulator Debug
FSL	0x1FD	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
FSL	0x1FE	BUCK_TOP_LVSH_2	R/W	BUCK_VDDQ_EN	BUCK_VDDQ_PWRSTG_EN[6:0]							0x7F	Switching Regulator Debug
RSVD	0x1FF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved
VD2	0x200 - 0x227	-	-	VD2								-	Reserved
RSVD	0x228 - 0x2FF	-	-	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	0x00	Reserved

Notes

21. RSVD: Reserved registers, not for customer use.
22. FSL: Freescale dedicated Registers for special PMIC control

HARDWARE DESIGN CONSIDERATIONS

EXTERNAL COMPONENT REQUIREMENT

Table 75. External Components BOM [23]

Component	Value	Package	Description	Qty	Part #	Manufacturer
Freescale Package						
900844	-	MAPBGA	Integrated Power Management IC for Ultra-mobile Platforms for Netbook Computers	1	SC900844JVK	Freescale
VCC - (0.65 - 1.2 V) / 3.5 A VID CPU BUCK with External FETs						
CINCC	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
COCC	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	4	AMK107BJ226MA-T	Taiyo Yuden
LCC	0.68 µH	4x4x2	Saturation current = 4.8 A for 10% drop, DCR_max = 25.3 mohm	1	XPL4020-681MLB	Coilcraft
MHSCC	46 mohm	BGA	High Side P-FET	1	FDZ293P, FDC638APZ or FDMA291P	Fairchild
MLSCC	23 mohm	BGA	Low Side N-FET	1	FDZ294N, FDC637BNZ or FDMA430NZ	Fairchild
VNN - (0.65 - 1.2 V) / 1.6 A VID CPU BUCK with External FETs						
CINNN	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
CONN	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	2	AMK107BJ226MA-T	Taiyo Yuden
LNN	1.0 µH	3.3x3.3x1.4	Saturation current = 2.3 A for 10% drop, DCR_max = 55 mohm	1	LPS3314-102ML	Coilcraft
MNN	95 mohm 68 mohm	MicroFET	High Side P-FET and Low Side N-FET housed in one package	1	FDMA1032CZ	Fairchild
VDDQ - 1.8/1.5 V / 1.3 A BUCK						
CINDDQ	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
CODDQ	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	2	AMK107BJ226MA-T	Taiyo Yuden
LDDQ	0.50 µH	2.0x2.0x1.0	Saturation current = 1.8 A for 10% drop, DCR_max = 45 mohm	1	XPL2010-501ML	Coilcraft
RFBDDQ15_1[24]	681 ohm	0402	Chip resistor 1% 1/10W	1	CRCW0402681RFKED	Vishay/Dale
RFBDDQ15_2[24]	2.21 kohm	0402	Chip resistor 1% 1/10W	1	CRCW04022K21FKED	Vishay/Dale
V21 - 2.1 V / 1.0 A BUCK						
CIN21	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
CO21	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	1	AMK107BJ226MA-T	Taiyo Yuden
L21	0.50 µH	2.0x2.0x1.0	Saturation current = 1.8 A for 10% drop, DCR_max = 45 mohm	1	XPL2010-501ML	Coilcraft
V15 - 1.5 V(or 1.6 V) / 1.5 A BUCK						
CIN15	10 µF	0603	Ceramic Capacitor, 6.3 V, X5R	1	GRM188R60J106ME47D	Murata
CO15	22 µF	0603	Ceramic Capacitor, 4.0 V, X5R	2	AMK107BJ226MA-T	Taiyo Yuden
L15	0.50 µH	2.0x2.0x1.0	Saturation current = 1.8 A for 10% drop, DCR_max = 45 mohm	1	XPL2010-501ML	Coilcraft

Notes

23. Throughout this document, there are references to non-Freescale components. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
24. To operate the VDDQ as a 1.5 V buck regulator, the recommended resistors, RFBDDQ15_1 and RFBDDQ15_2 are needed in the feedback path, as shown in Figure 28.

Table 75. External Components BOM [(23)]

Component	Value	Package	Description	Qty	Part #	Manufacturer
VBG - 1.25 V/2.0 mA LDO & VCCA - 1.5 V/150 mA LDO						
CIN1P8	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
COBG	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
COCCA	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VCC180- 1.8 V/390 mA LDO & VPNL18- 1.8 V/225 mA LDO & - 1.8 V/50 mA LDO						
CIN2P1	0.47 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J474KE19D	Murata
COCC180	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
COPNL18	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
COPMIC	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VYMXYFI18 - (YMX:1.8 V/200 mA - YFI:1.8 V/200 mA) LDO						
CINYMXYFI18	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
COYMXYFI18	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VCCPAOAC- 1.05 V/155 mA LDO & VCCPDDR - 1.05 V/60 mA LDO & VAON - 1.2 V/250 mA LDO &VMM- 1.2 V/5.0 mA LDO & VCCP - 1.05 V/445 mA LDO						
CIN1P5	0.47 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J474KE19D	Murata
COCCPAOAC	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
COCCPDDR	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
COAON	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
COMM	1.0 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
COCCP	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VIMG25- 2.5 V/80 mA LDO & VIMG28- 2.8 V/225 mA LDO						
CINIMG	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
COIMG25	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
COIMG28	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
VPNL33 - 3.3 V/100 mA Switch						
COPNL33	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
VSDIO - 3.3 V/215 mA Switch OR 1.8 V/215 mA LDO						
CINSDIO	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
COSDIO	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
RSDIO	0 ohm	0402	Chip Resistor, 1%	1	ERJ-2GE0R00X	Panasonic
MSDIO	95 mohm	SC70	PFET, switch	1	FDG332PZ	Fairchild
Internal Supplies						
CCORE	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
CCOREDIG	2.2 µF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J225ME15D	Murata
CCOREREF	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata
Input power path						
RNTCEV	10 kohm	0201	Chip Resistor, 1%	1	ERJ-1GEF1002C	Panasonic
RNTC	10 kohm	0201	Chip Resistor, 1%	1	ERJ-1GEF1002C	Panasonic
CBAT	22 µF	0805	Ceramic Capacitor, 10 V, X5R	2	LMK212BJ226MG-T	Taiyo Yuden
Coin cell						
CCOIN	100 nF	0201	Ceramic Capacitor, 6.3 V, X5R	1	GRM033R60J104KE19D	Murata

Table 75. External Components BOM [23]

Component	Value	Package	Description	Qty	Part #	Manufacturer
ADC						
CADREF	1.0 μF	0402	Ceramic Capacitor, 6.3 V, X5R	1	GRM155R60J105ME19D	Murata
Oscillator and Real Time Clock - RTC						
XTALRTC	32.768 kHz	3.2x1.5x0.9	CRYSTAL 32.768 kHZ 12.5 pF SMD	1	ABS07-32.768KHZ-T	Abracon
CXTALRTC1	22 pF	0201	Ceramic Capacitor, 25 V, C0G	1	GRM0335C1E220JD01D	Murata
CXTALRTC2	22 pF	0201	Ceramic Capacitor, 25 V, C0G	1	GRM0335C1E220JD01D	Murata
GPIOs & GPOs & Power Button						
RPULLUPX[25]	100 kohm	0201	Chip Resistor, 1% - Pull-up Resistors for OD configured GPIOs	0	ERJ-1GEF1003C	Panasonic
Total Component Count				62		

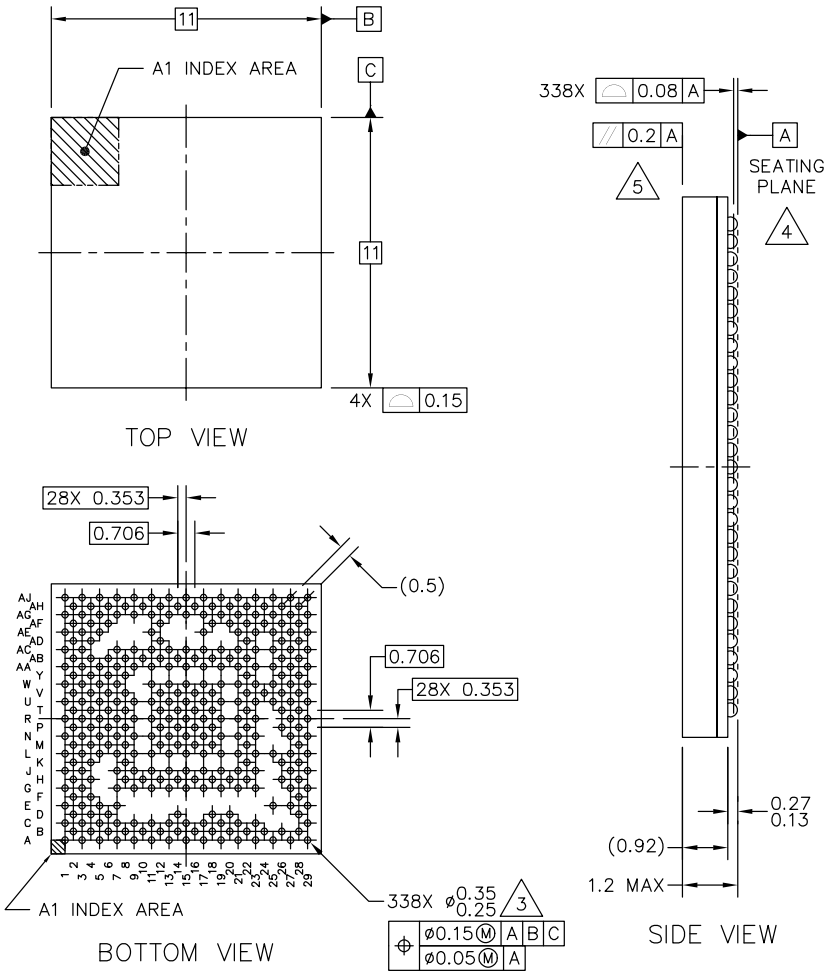
Notes

25. This is a recommended resistor when required by a specific GPIO.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PBGA, THIN PROFILE, FINE PITCH, 338 I/O, 11 X 11 PKG, INTERSTITIAL PITCH (MAP)	DOCUMENT NO: 98ASA10841D	REV: O
	CASE NUMBER: 2037–01	11 JUN 2008
	STANDARD: NON–JEDEC	

JVK SUFFIX
338-PIN
98ASA10841D
REVISION 0

900844

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: PBGA, THIN PROFILE, FINE PITCH, 338 I/O, 11 X 11 PKG, INTERSTITIAL PITCH (MAP)	DOCUMENT NO: 98ASA10841D	REV: O
	CASE NUMBER: 2037–01	06 JUN 2008
	STANDARD: NON–JEDEC	

JVK SUFFIX
338-PIN
98ASA10841D
REVISION 0

900844

PACKAGE MECHANICAL OUTLINE DRAWING

The package style is an 11x11 fine interstitial pitch, thin profile PBGA. The package has a semi populated matrix that includes 338 balls. The ball count includes 322 assigned signal pins and four sets of 4 corner balls.

PACKAGE ASSEMBLY RECOMMENDATIONS

For improved protection against mechanical shock, Freescale recommends applying corner glue to the mounted 900844 MAPBGA package. This corner glue application is described in the AN3954 - "PCB Layout Guidelines for SC900841 and SCCSP900842" application note.

Freescale's preferred material for the corner glue application is the Loctite 3128 board level adhesive, applied at a 0° or 45° dispense angle in a continuous motion, and with the fillet length extended to a minimum of 3 ball rows and columns, at each corner.

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	8/2010	• Initial release • Ball map updates • Fix Default Values for Various VR control registers. • Fix Package Suffix to “JVK” • Freescale format, form and style corrections.
2.0	5/2011	• No parametrics were altered. Only various adjustments, corrections, and clarifications were made to text, tables, and images, for improved accuracy.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

SC900844
Rev. 2.0
5/2011