FAIRCHILD SEMICONDUCTOR®

June 2011

# FAN7314A — LCD Backlight Inverter Drive IC

## Features

- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range: 6V to 25.5V
- Backlight Lamp Ballast and Soft Dimming
- Minimal Required External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS Half-Bridge Topology
- Soft-Start
- PWM Control at Fixed Frequency
- Analog and Burst Dimming Function
- Programmable Striking Frequency
- Open-Lamp Protection
- Open-Lamp Regulation
- Thermal Shutdown
- 20-Pin SOIC

## Applications

- LCD TV
- LCD Monitor

## Description

The FAN7314A provides all the control functions for a series parallel resonant converter as well as a pulse width modulation (PWM) controller to develop a supply voltage. Typical operating frequency range is between 30kHz and 250kHz, depending on the CCFL and the transformer's characteristics.

The FAN7314A is available in a 20-SOIC package.

**20-SOIC**

## Ordering Information

| Part Number | Package | Operating Temperature | Packing Method |
|---|---|---|---|
| FAN7314AM | 20-SOIC | -25 to +85°C | RAIL |
| FAN7314AMX | 20-SOIC | -25 to +85°C | TAPE & REEL |

## Important Note:

For complete performance specifications, please contact one of the following:

| | | | |
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## Block Diagram

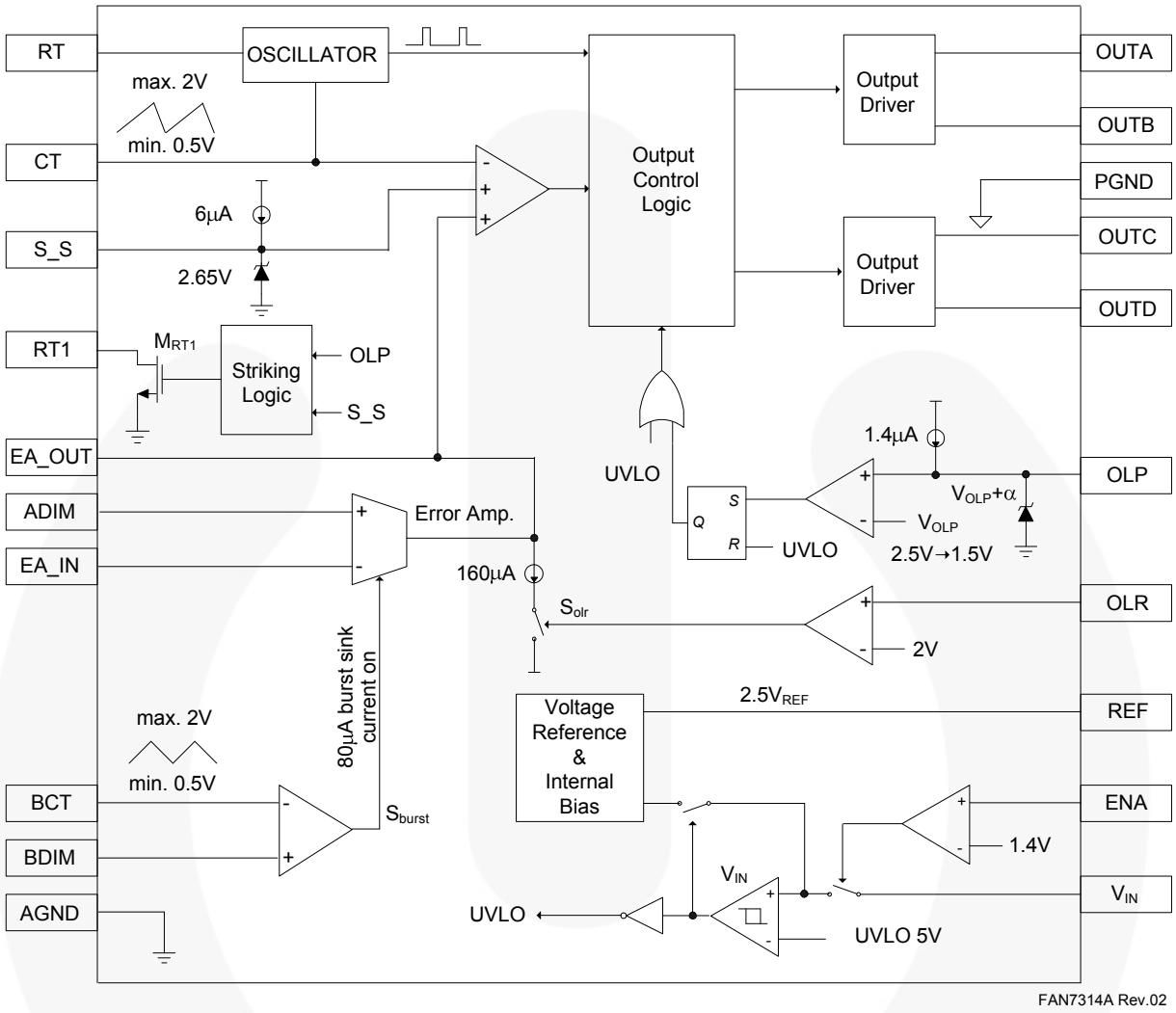
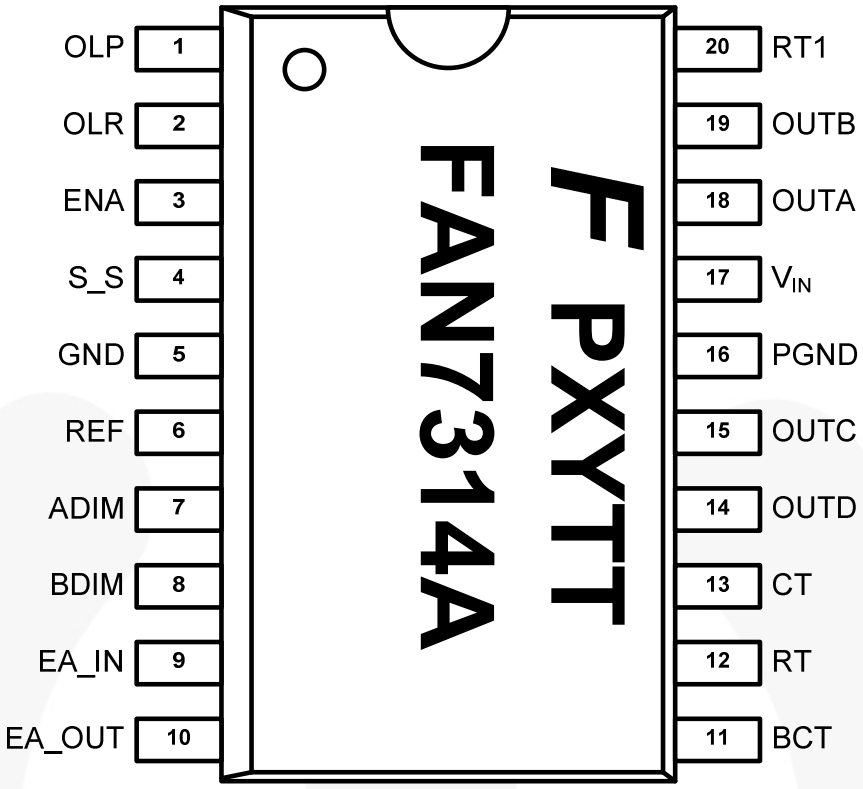



**Figure 1. Internal Block Diagram**

## Pin Configuration




**F** : Fairchild logo
**P** : Assembly site code
**XY** : Year & weekly code
**TT** : Die run code
**FAN7314A** : Device name

**Figure 2. Package Diagram**

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## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | OLP | **Open-Lamp Protection**. Typically, a capacitor is connected to this pin from the ground. The capacitor is charged by the 1.4μA internal current source and when its voltage is more than 2.5V the IC enters into the shutdown mode. |
| 2 | OLR | **Open-Lamp Regulation**. If the voltage of the OLR pin is more than 2V, the voltage of the EA_OUT pin voltage will be discharged by the 160μA internal current source. |
| 3 | ENA | **Enable**. Turns on/off the IC. |
| 4 | S_S | **Soft-Start**. Typically, a capacitor is connected to this pin from the ground. The capacitor is charged by the 6μA internal current source. Soft start operation is working while the S_S pin voltage is less than the EA_OUT pin voltage. |
| 5 | GND | **Ground**. Control block. |
| 6 | REF | **Reference**. 2.5V reference output. |
| 7 | ADIM | **Analog Dimming**. This pin is the input for positive polarity. The lamp current decreases with decreasing this pin voltage. |
| 8 | BDIM | **Burst Dimming**. This pin is the input for negative polarity. The voltage range of 0.5 to 2V at this pin controls burst mode duty cycle from 0% to 100%. |
| 9 | EA_IN | **Error Amplifier Inverting Input**. This pin voltage is regulated at ADIM voltage. |
| 10 | EA_OUT | **Error Amplifier Output**. Typically, a compensation capacitor is connected to this pin from the ground. |
| 11 | BCT | **Burst Timing Capacitor**. This pin is for programming the frequency of the burst dimming. Typically, a capacitor is connected to this pin from the ground. The BCT frequency increases with decreasing its capacitance. |
| 12 | RT | **Timing resistor**. This pin is for programming the switching frequency. Typically, a resistor is connected to this pin from the ground. The switching frequency increases with decreasing its resistance. |
| 13 | CT | **Timing Capacitor**. This pin is for programming the switching frequency. Typically, a capacitor is connected to this pin from the ground. The switching frequency increases with decreasing its capacitance. |
| 14 | OUTD | **NMOS Gate-Drive Output**. |
| 15 | OUTC | **PMOS Gate-Drive Output**. |
| 16 | PGND | **Power Ground**. |
| 17 | VIN | **Supply Voltage**. |
| 18 | OUTA | **PMOS Gate-Drive Output**. |
| 19 | OUTB | **NMOS Gate-Drive Output**. |
| 20 | RT1 | **Striking Timing Resistor**. Typically, a resistor is connected to this pin from the RT pin. The striking frequency increases with decreasing its resistance. |

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IN}$ | IC Supply Voltage | 6 | 25.5 | V |
| $T_A$ | Operating Temperature Range | -25 | +85 | °C |
| $T_J$ | Operating Junction Temperature | | +150 | °C |
| $T_{STG}$ | Storage Temperature Range | -65 | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance Junction-Air[1,2] | | 90 | °C/W |
| $P_D$ | Power Dissipation | | 1.4 | W |

**Notes:**
1. Thermal resistance test board. Size: 76.2mm x 114.3mm x 1.6mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.
2. Assume no ambient airflow.

## Pin Breakdown Voltage

| Pin # | Name | Value | Unit | Pin # | Name | Value | Unit |
|---|---|---|---|---|---|---|---|
| 1 | OLP | 7 | V | 11 | BCT | 7 | V |
| 2 | OLR | 7 | | 12 | RT | 7 | |
| 3 | ENA | 7 | | 13 | CT | 7 | |
| 4 | S_S | 7 | | 14 | OUTD | 10.5 | |
| 5 | GND | 7 | | 15 | OUTC | 25.5 | |
| 6 | REF | 7 | | 16 | PGND | 7 | |
| 7 | ADIM | 7 | | 17 | VIN | 25.5 | |
| 8 | BDIM | 7 | | 18 | OUTA | 25.5 | |
| 9 | EA_IN | 7 | | 19 | OUTB | 10.5 | |
| 10 | EA_OUT | 7 | | 20 | RT1 | 7 | |

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## Electrical Characteristics

For typical values, $T_A$ = 25°C, $V_{IN}$ = 12V, and -25°C ≤ $T_A$ ≤ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **REFERENCE SECTION (Recommended X7R Capacitor)** | | | | | | |
| $\Delta V_{ref}$ | Line Regulation | 5 ≤ $V_{IN}$ ≤ 25.5V | | 2 | 25 | mV |
| $V_{25}$ | 2.5V Regulation Voltage | | 2.45 | 2.5 | 2.55 | V |
| **OSCILLATOR SECTION (MAIN)** | | | | | | |
| $f_{OSC}$ | Oscillation Frequency | $T_A$=25°C, CT=270pF, RT=18kΩ | 110.4 | 115.0 | 119.6 | kHz |
| | | CT=270pF, RT=18kΩ | 108 | 115 | 122 | |
| $V_{cth}$ | CT High Voltage | | | 2.0 | | V |
| $V_{ctl}$ | CT Low Voltage | | | 0.5 | | V |
| **OSCILLATOR SECTION (BURST)** | | | | | | |
| $f_{oscb}$ | Oscillation Frequency | $T_A$=25°C, $C_{tb}$=10nF, RT=18kΩ | 195 | 220 | 246 | Hz |
| | | $C_{tb}$=10nF, RT=18kΩ | 191 | 220 | 249 | |
| $V_{bcth}$ | BCT High Voltage | | | 2 | | V |
| $V_{bctl}$ | BCT Low Voltage | | | 0.5 | | V |
| **ERROR AMPLIFIER SECTION** | | | | | | |
| $G_m$ | Error Amplifier Trans-conductance | EA_OUT=1V, ADIM=1V | 100 | 360 | 600 | umho |
| $A_v$ | Error Amplifier Open-loop Gain(3) | | | 50 | | dB |
| $V_{eh}$ | EA_OUT Clamping Voltage | | 2.3 | 2.7 | 3.0 | V |
| $I_{sin}$ | Output Sink Current | ADIM=1V, EA_IN=2V | 35 | 70 | 105 | µA |
| $I_{sur}$ | Output Source Current | ADIM=1V, EA_IN=0V | -154 | -110 | -66 | µA |
| $I_{olr}$ | EA_OUT Sink Current on OLR | OLR>2.5V | -210 | -160 | -110 | µA |
| $I_{burst}$ | EA_OUT Sink Current on Burst Dimming | | -100 | -80 | -60 | µA |
| **SOFT-START SECTION** | | | | | | |
| $I_{SS}$ | Soft-Start Current | S_S=1V | 4 | 6 | 8 | µA |
| $V_{ssh}$ | Soft-Start Clamping Voltage | | 2.3 | 2.65 | 3.00 | V |
| **PROTECTION SECTION** | | | | | | |
| $V_{olp0}$ | Open-Lamp Protection Voltage 0 | Start at open lamp | 2.2 | 2.5 | 2.8 | V |
| $V_{olp1}$ | Open-Lamp Protection Voltage 1 | Normal -> open lamp | 1.3 | 1.5 | 1.7 | V |
| $V_{olr}$ | Open-Lamp Regulation Voltage | | 1.75 | 2.00 | 2.25 | V |
| $I_{olp}$ | Open-Lamp Protection Charging Current | | 0.7 | 1.4 | 2.1 | µA |

**Note:**

3. These parameters, although guaranteed, are not 100% tested in production.

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## Electrical Characteristics (Continued)

For typical values, $T_A$ = 25°C, $V_{IN}$ = 15V, and -25°C ≤ $T_A$ ≤ 85°C, unless otherwise specified. Specifications to -25°C ~ 85°C are guaranteed by design based on final characterization results.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **UNDER VOLTAGE LOCK OUT SECTION** | | | | | | |
| $V_{th}$ | Start Threshold Voltage | | | | 5 | V |
| $I_{st}$ | Start-up Current | $V_{IN}$=$V_{th}$-0.2 | | 130 | 180 | µA |
| $I_{op}$ | Operating Supply Current | $V_{IN}$=12V | | 1.5 | 4.0 | mA |
| $I_{sb}$ | Stand-by Current | $V_{IN}$=12V | | 200 | 370 | µA |
| **ON/OFF SECTION** | | | | | | |
| $V_{on}$ | On State Input Voltage | | 2 | | 5 | V |
| $V_{off}$ | Off Stage Input Voltage | | | | 0.7 | V |
| **OUTPUT SECTION** | | | | | | |
| $V_{pdhv}$ | PMOS Gate Drive High Voltage | $V_{IN}$=12V | | $V_{IN}$ | | V |
| $V_{phlv}$ | PMOS Gate Drive Low Voltage | $V_{IN}$=12V | $V_{IN}$-10.5 | $V_{IN}$-8.5 | $V_{IN}$-6.5 | V |
| $V_{ndhv}$ | NMOS Gate Drive High Voltage | $V_{IN}$=12V | 6.5 | 8.5 | 10.5 | V |
| $V_{ndlv}$ | NMOS Gate Drive Low Voltage | $V_{IN}$=12V | | 0 | | V |
| $V_{puv}$ | PMOS Gate Voltage with UVLO Activated | $V_{IN}$=$V_{th}$-0.2 | $V_{IN}$-0.3 | | | V |
| $V_{nuv}$ | NMOS Gate Voltage with UVLO Activated | $V_{IN}$=$V_{th}$-0.2 | | | 0.3 | V |
| $t_r$ | Rising Time[4] | $V_{IN}$=12V, $C_{load}$=2nF | | 200 | 500 | ns |
| $t_f$ | Falling Time[4] | $V_{IN}$=12V, $C_{load}$=2nF | | 200 | 500 | ns |
| **MAXIMUM / MINIMUM OVERLAP** | | | | | | |
| | Min. Overlap between diagonal switches[4] | $f_{osc}$ = 100kHz | | 0 | | % |
| | Max. Overlap between diagonal switches[4] | $f_{osc}$ = 100kHz | | 100 | | % |
| **DELAY TIME** | | | | | | |
| | PDR_A/NDR_B[4] | RT=18kΩ | | 450 | | ns |
| | PDR_C/NDR_D[4] | RT=18kΩ | | 450 | | ns |

**Note:**
4. These parameters, although guaranteed, are not 100% tested in production.

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## Functional Description

**UVLO:** The under-voltage lockout (UVLO) circuit guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the VIN value. The UVLO circuit turns on the control circuit when VIN exceeds 5V. When VIN is lower than 5V, the IC's standby current is less than 200μA.

**ENA:** Applying voltage higher than 2V to the ENA pin enables the operation of the IC. Applying voltage lower than 0.7V to the ENA pin disables the operation of the inverter.

**Soft-start:** The soft-start function requires that the S_S pin is connected through a capacitor to GND. A soft-start circuit ensures a gradual increase in the input and output power. The capacitor connected to the S_S pin determines the rate at which the duty ratio rises. It is charged by a 6μA current source.

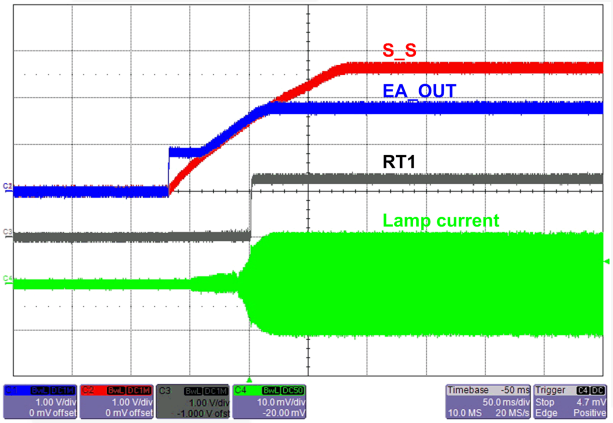


**Figure 3. Soft-start during Initial Operation**

**Main Oscillator**: The timing capacitors (CTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next, the timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed by adjusting the RT and CT values. The main frequency can be calculated as shown below.

$$f_{OSC} = \frac{19}{32 \cdot RT \cdot CT} \quad (1)$$

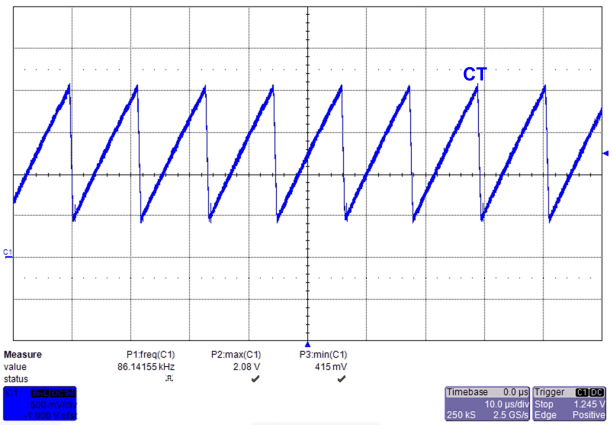


**Figure 4. Main Oscillator Waveform**

**Burst Oscillator and Burst Dimming**: The timing capacitors (BCTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next the timing capacitors start charging again and a new switching cycle begins. The burst dimming frequency can be programmed by adjusting the RT and BCT values. The burst dimming frequency can be calculated as shown below.

$$f_{OSCB} = \frac{3.75}{96 \cdot RT \cdot CT} \quad (2)$$

To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.

By comparing the input of BDIM pin with the 0.5~2V triangular wave of the burst oscillator the PWM pulses for burst dimming. The PWM pulse controls EA_OUT's voltage by summing 85μA into the EA_IN pin.

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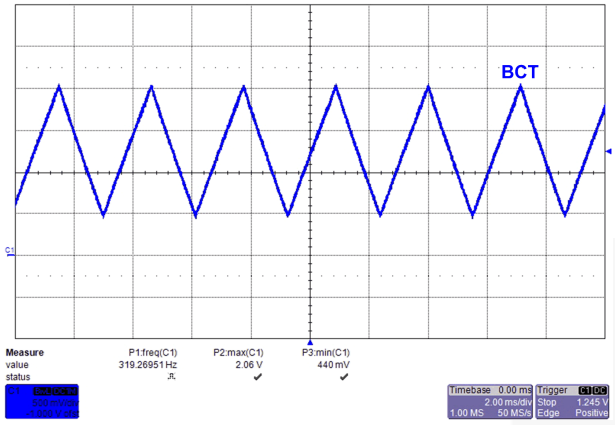


**Figure 5. Burst Oscillator Waveform**

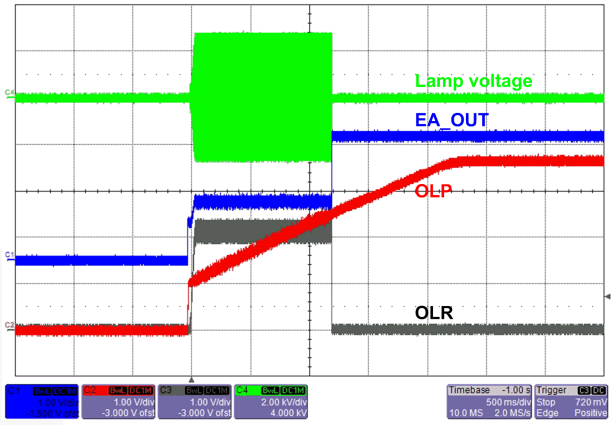


**Figure 7. OLR Voltage during Striking Mode**

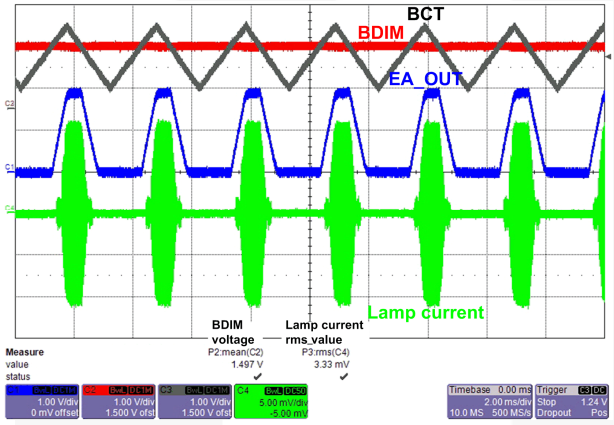


**Figure 6. Burst Dimming**

**Output Drives**: The four output drives are designed so that switches A and B, C and D never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair drives the other half-bridge.

**Open-Lamp Regulation and Open-Lamp Protection**: It is necessary to suspend power stage operation if an open lamp occurs because the power stage has high gain. When a voltage higher than 2V is applied to the OLR pin, the part enters regulation mode and controls the EA_OUT voltage. This limits the lamp voltage by summing 105μA into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 1.4μA internal current source. Once it reaches 2.5V, the IC shuts down and all output is high.

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## Timing Diagram

The FAN7314A uses the half-bridge to drive CCFL.

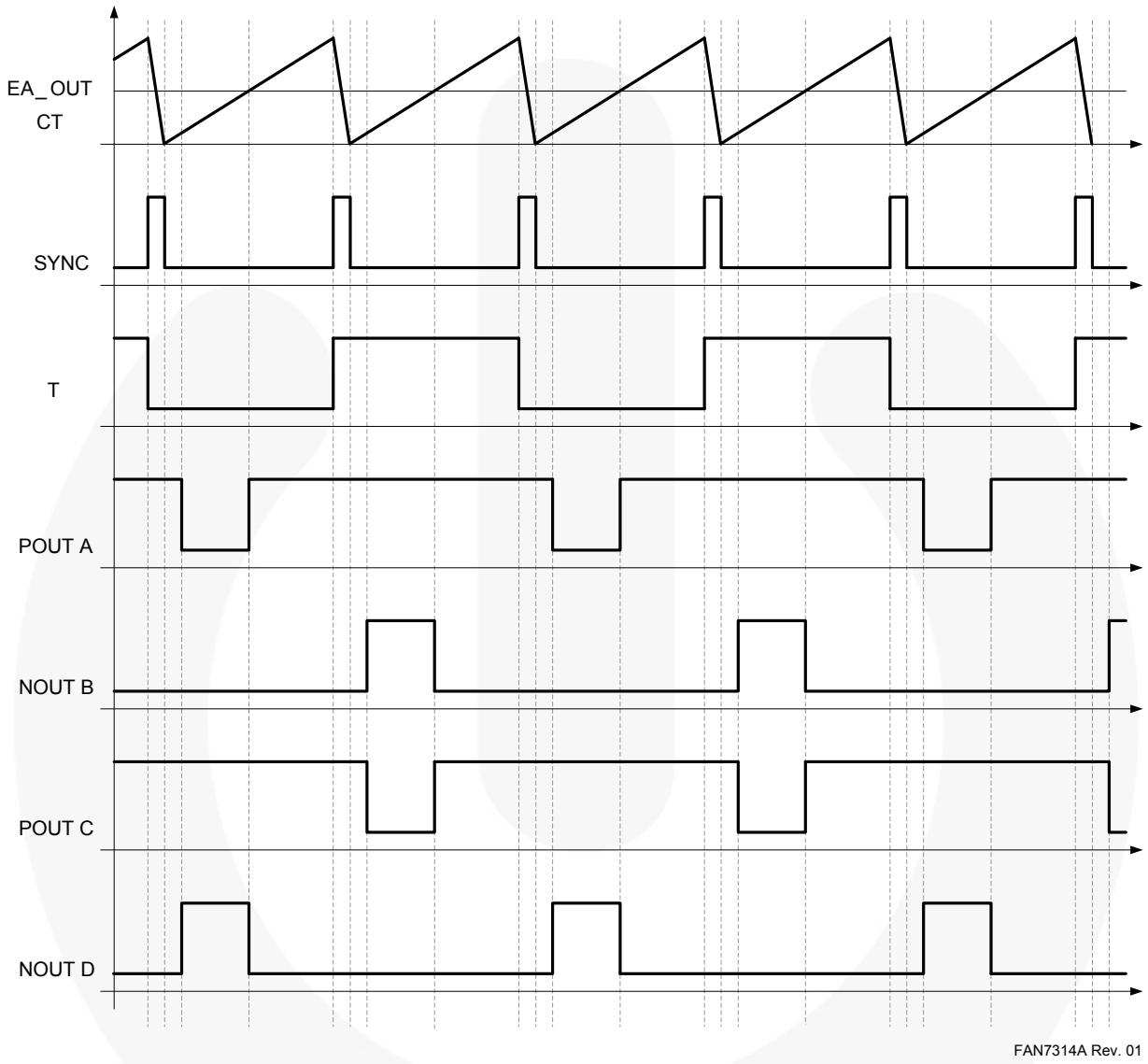


**Figure 8. MOSFET Gate Drive Signal**

## Typical Application Circuit (LCD Backlight Inverter)

| Application | Device | Input Voltage Range | Number of lamps |
|---|---|---|---|
| 22-Inch LCD Monitor | FAN7314A | 22V±5% | 4 |

### 1. Features

- High-Efficiency Single-Stage Power Conversion
- P-N Half-Bridge Topology
- Reduces Required External Components
- Enhanced System Reliability through Protection Functions

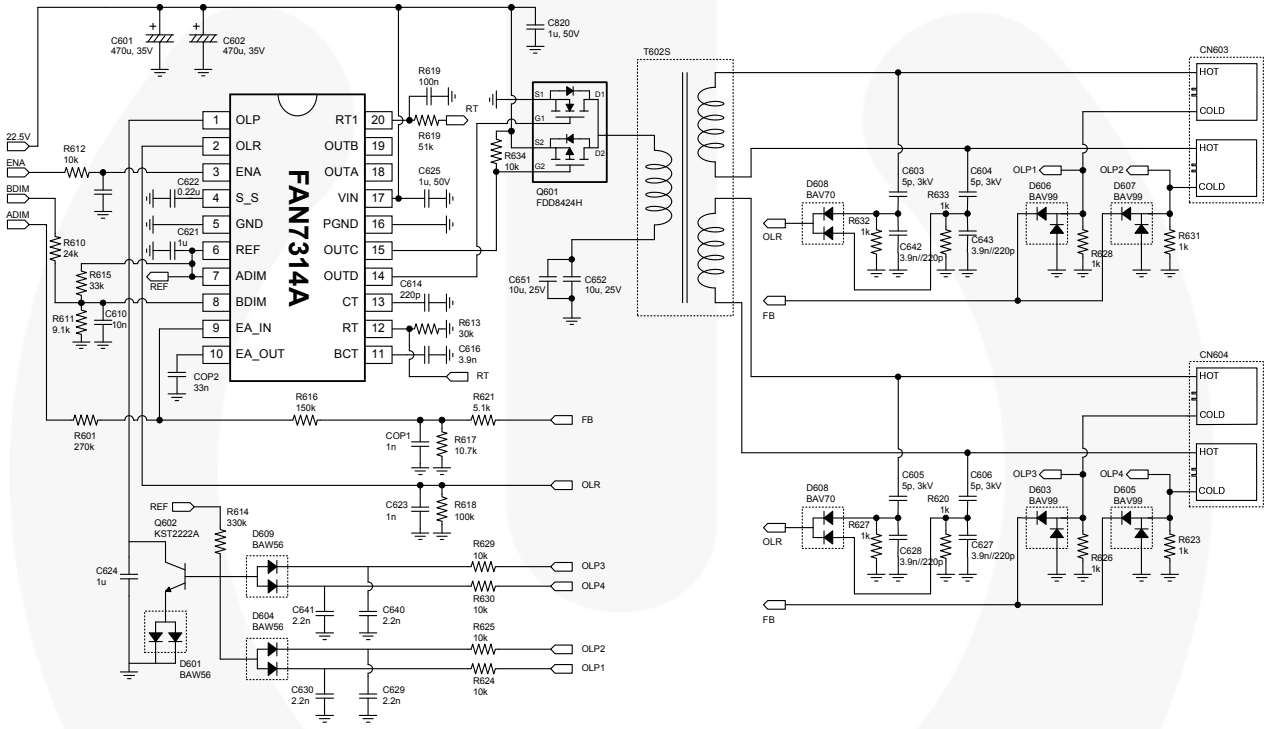


**Figure 9. Typical Application Circuit**

### 2. Transformer Specifications

- Supported by Clover Hitech (http://www.cloverhitech.com)
- PART NO : EEL-22W

| Pin No. | Wire | Turns | Inductance | Leakage Inductance | Remarks |
|---|---|---|---|---|---|
| 2 → 7 | UTSC 0.1×12 | 19 | 83.0μH | 16μH | 1kHz, 1V |
| 3 → 6 | | | | | |
| 1 → 8 | 1 UEW 0.04Ω | 2300 | 1.4H | 280mH | |
| 4 → 5 | | | | | |

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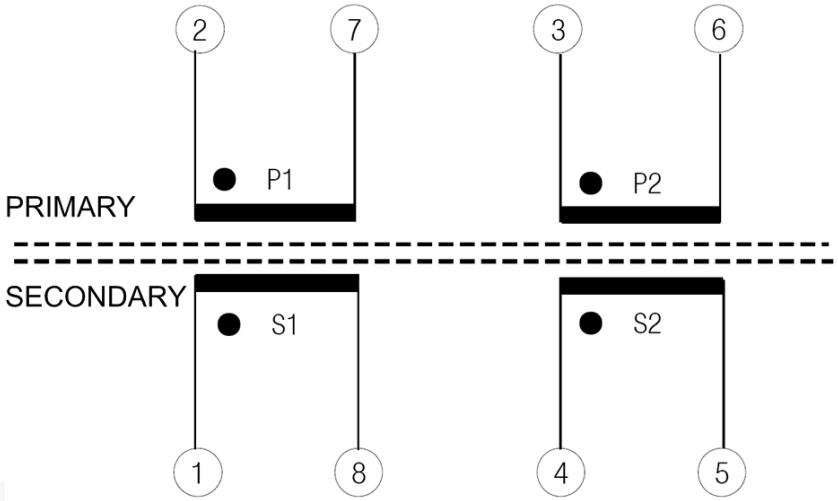


**Figure 10. Schematic Diagram**

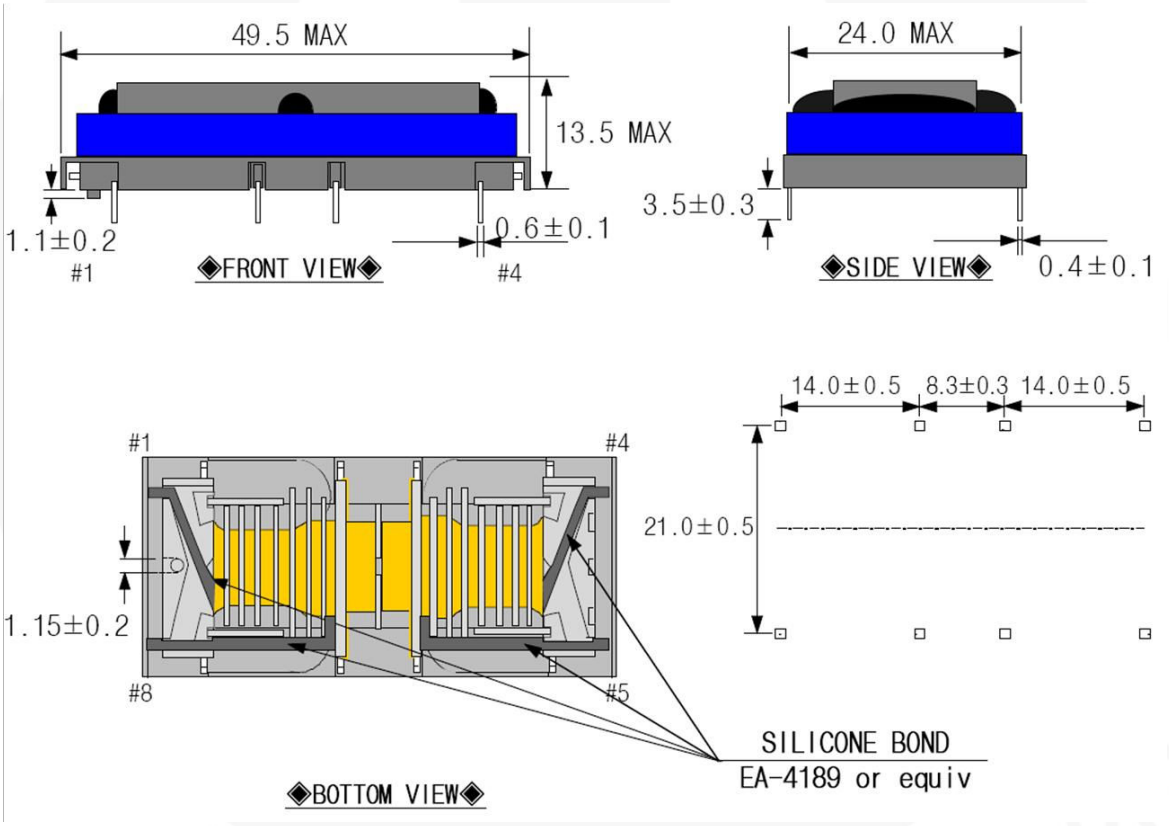


**Figure 11. Dimensions**

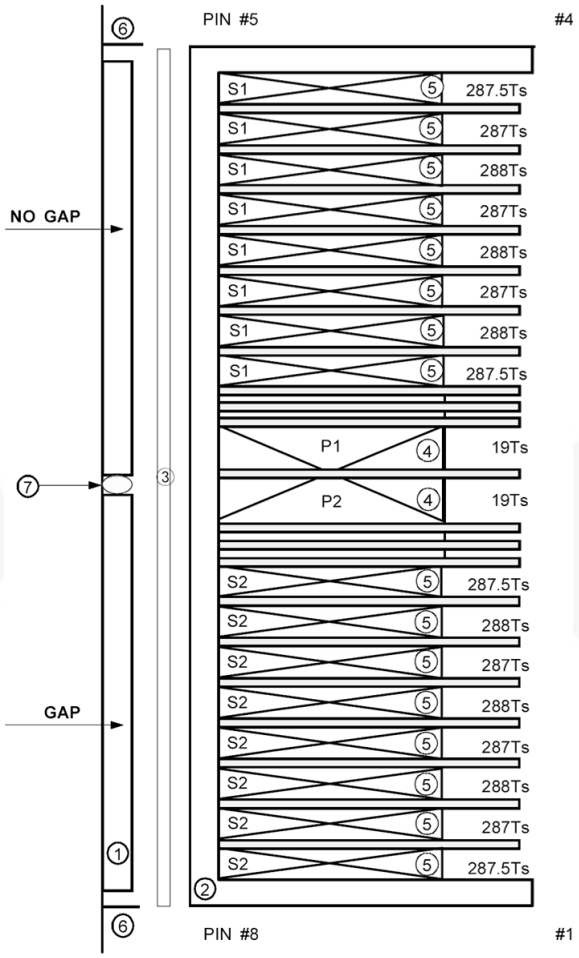


**Figure 12. Section Diagram**

## Physical Dimensions

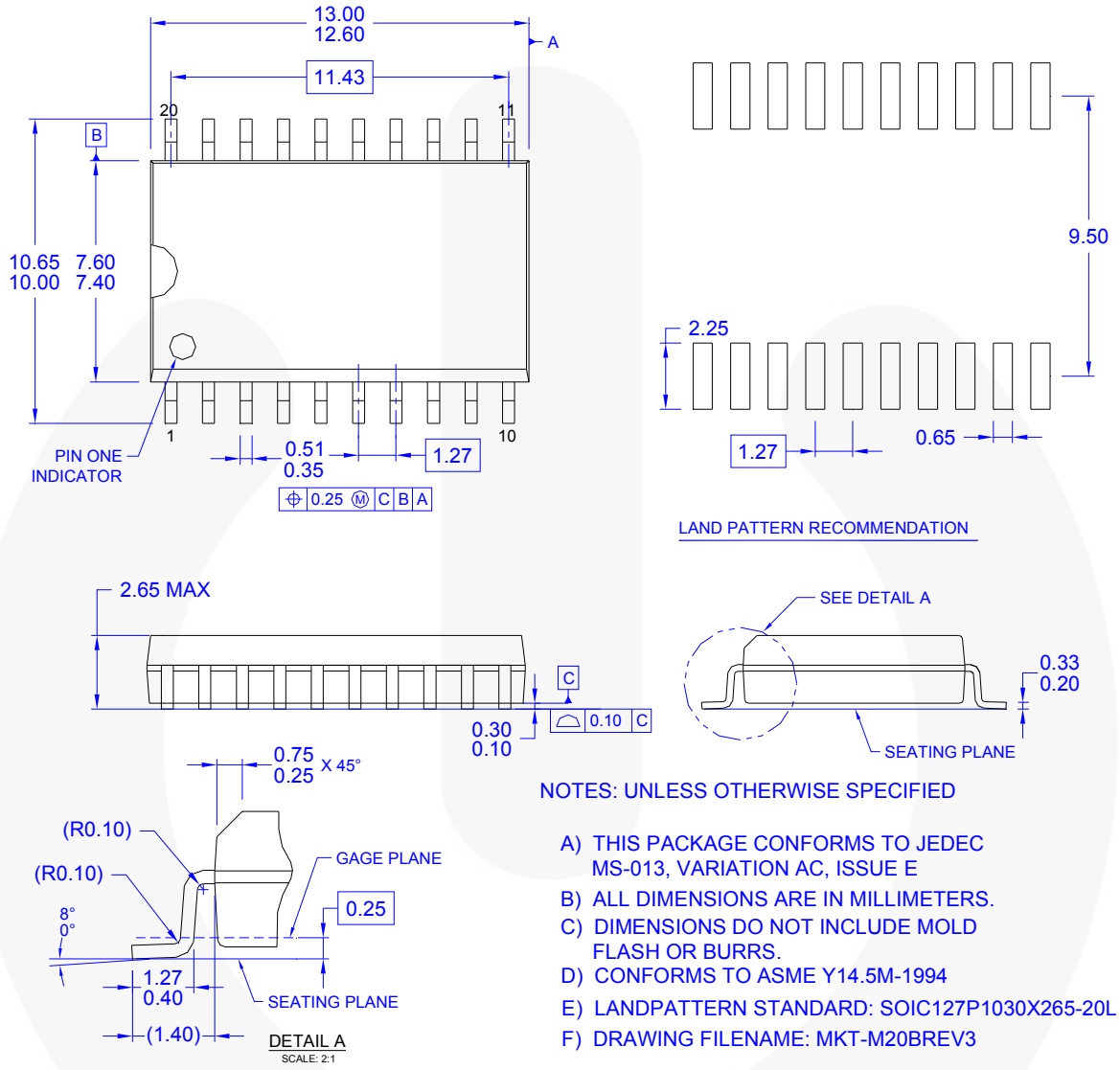


**Figure 13. 20-SOIC Package**

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## ANTI-COUNTERFEITING POLICY

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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

## PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
| No Identification Needed | Full Production | Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design. |
| Obsolete | Not In Production | Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only. |

Rev. I54

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