

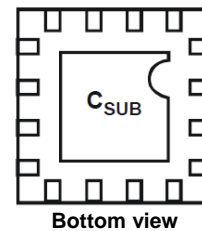
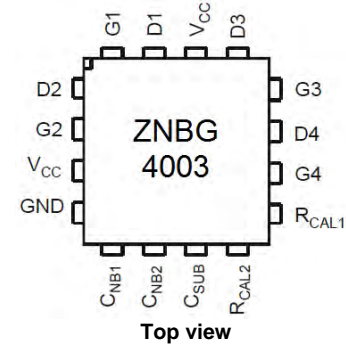
Description

The ZNBG4003 is a four stage depletion mode FET bias controller intended primarily for satellite Low Noise Block's (LNB's), but its also suitable for other LNA applications such as those in found in PMR's and microwave links. The ZNBG4003 provides each FET with a negative gate voltage and positive drain voltage with user programmable drain current.

Features

- Four stage FET bias controller
- Operating range of 4.75V to 8.0V
- FET drain voltages set at 2.0V
- FET drain current selectable from 0 to 15mA
- Allows first and second stage FETs to be run at different (optimum) drain currents
- FET drain voltages and currents stable over temperature
- FETs protected against overstress during power-up and power-down.
- Internal negative supply generator allowing single supply operation (available for external use)
- Low external component count
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments

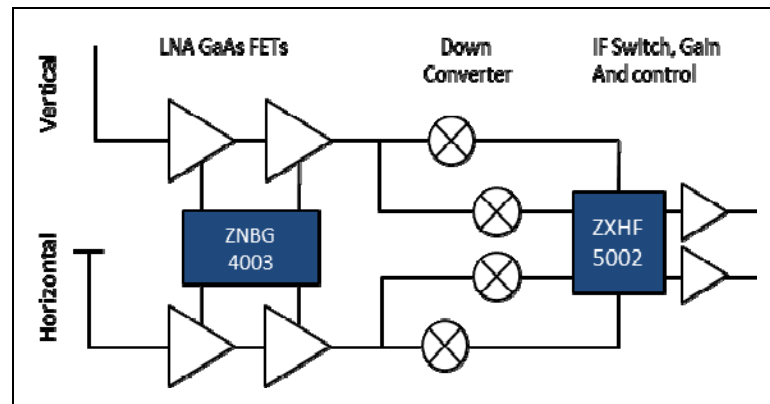


Applications

- Two single type Twin LNB's
- Twin LNB's
- Quad LNB's
- Microwave links
- PMR and Cellular telephone systems

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Twin Universal LNB System Diagram



Device Description

The ZNBG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBS with a minimum of external components.

The ZNBG4003 provides four FET bias stages, arranged in two pairs of two. Resistors connected to pins R_{CAL1} and R_{CAL2} set the FET drain currents of each pair over the range of 0 to 15mA, allowing input FETs to be biased for optimum noise and amplifier FETs for optimum gain.

Drain voltages of all stages are set at 2.0V. The drain supplies are current limited to approximately 5% above the operating currents set by the R_{cal} resistors.

Depletion mode FETs require a negative voltage bias supply when operated in grounded source circuits. The ZNBG4003 includes an integrated switched capacitor DC-DC converter generating a regulated output of -2.5V to allow single supply operation.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the

recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

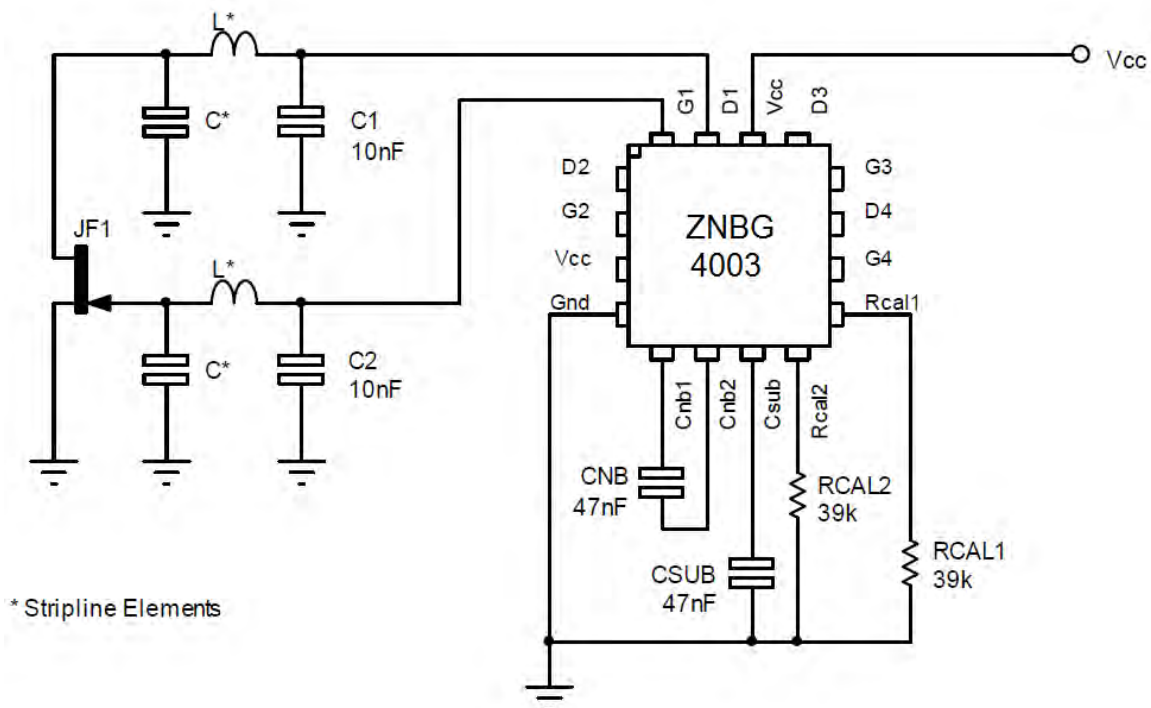
It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

To protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed -3V. Additionally each stage has its own individual current limiter. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

To minimise PCB space ZNBG4003 is packaged in the 16 pin 3mm x 3mm QFN package.

Device operating temperature is -40°C to +85°C to suit a wide range of environmental conditions.

Typical Application Circuit



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 5)

Parameter	Rating	Unit
Supply Voltage	-0.6 to +10	V
Supply Current	80	mA
Power Dissipation	500	mW
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-40 to +150	°C

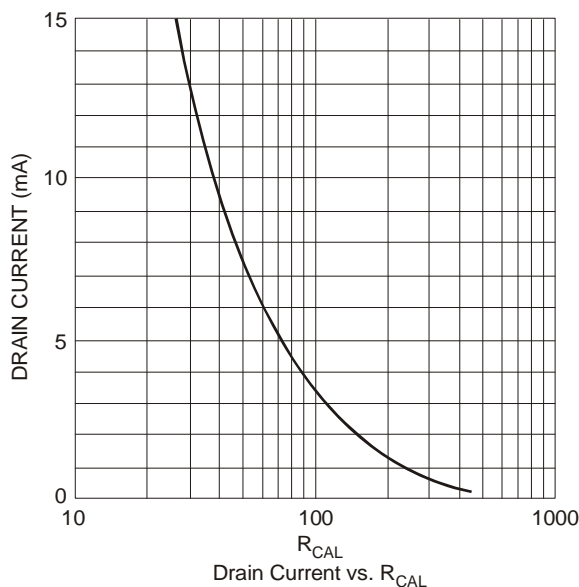
Electrical Characteristics

(@ T_{AMB} = +25°C, V_{CC} = 5.0V (Note 1), R_{CAL1} = R_{CAL2} = 39k (setting I_D to 10mA) unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	Operating Voltage Range (Note 4)		4.75		8.0	V
I _{CC}	Supply Current	I _{D1} = I _{D2} = I _{D3} = I _{D4} = 0		1.8	4.5	mA
I _{CC(L)}		I _{D1} = I _{D2} = I _{D3} = I _{D4} = 10mA		43	45	
V _{CSUB}	Substrate Voltage (Note 6,7)	I _{CSUB} = 0	-3.0	-2.65	-2.0	V
V _{CSUB(L)}		I _{CSUB} = -100µA		-2.55	-1.9	V
F _{OSC}	Oscillator Frequency		150	240	600	kHz
Gate Characteristics						
Gate (G1 to G4)						
I _G	Current Range		-100		+500	µA
V _{G(L)}	Voltage Low	I _D = 12mA, I _G = 10µA	-3.0	-2.5	-2.0	V
V _{G(H)}	Voltage High	I _D = 8mA, I _G = 0	0	0.7	1.0	V
Drain Characteristics						
Drain (D1 to D4)						
I _D	Current Range		0		15	mA
I _{D(OP)}	Current Operating	Standard Application Circuit	8	10	12.5	mA
V _{D(OP)}	Voltage Operating	I _D = 10mA	1.8	2.0	2.2	V
dI _D /dV _{CC}	Δ I _D vs V _{CC}	V _{CC} = 5.0V to 8.0V		1.2		%/V
dI _D /dT _{OP}	Δ I _D vs T _{OP}	T _{OP} = -40°C to +85°C		0.09		%/°C
dI _D /dV _{CC}	Δ V _D vs V _{CC}	V _{CC} = 5.0V to 8.0V		0.08		%/V
dI _D /dT _{OP}	Δ V _D vs T _{OP}	T _{OP} = -40°C to +85°C		110		ppm/°C
Output Noise (Note 8)						
V _{D(NOISE)}	Drain Voltage	C _{GRATE-GND} = 10nF, C _{DRAIN-GND} = 10nF			0.02	Vpk-pk
V _{G(NOISE)}	Gate Voltage	C _{GRATE-GND} = 10nF, C _{DRAIN-GND} = 10nF			0.005	Vpk-pk

- Notes:
- The two V_{CC} pins are internally connected, only one of the pins needs to be powered for the device to function. See applications section for further information.
 - ESD sensitive, handling precautions are recommended.
 - The negative bias voltages are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB} of value 47nF are required for this purpose.
 - The package (QFN1633) exposed pad must either be connected to C_{sub} or left open circuit.
 - Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.

Typical Characteristics (measured @ $T_{AMB} = +25^{\circ}C$, $V_{CC} = 5.0V$)



Application Information

Above is a partial applications circuit for the ZNBG4003 showing all external components needed for biasing one of the four FET stages available. Each bias stage is provided with a gate and drain pin. The drain pin provides a regulated 2.0V supply that includes a drain current monitor. The drain current taken by the external FET is compared with a user selected level, generating a signal that adjusts the gate voltage of the FET to obtain the required drain current. If for any reason, an attempt is made to draw more than the user set drain current from the drain pin, the drain voltage will be reduced to ensure excess current is not taken. The gate pin drivers are also current limited.

The bias stages are split up into two pairs, with the drain current of each pair set by an external R_{CAL} resistor. R_{CAL1} sets the drain currents of stages 1 and 3, whilst R_{CAL2} sets the drain currents of stages 2 and 4. This allows the optimisation of drain currents for differing tasks such as input stages where noise can be critical and later amplifier stages where gain may be more important. A graph showing the relationship between the value of R_{CAL} and I_D is provided in the Typical Characteristics section of this datasheet.

The ZNBG4003 includes a switched capacitor DC-DC converter that is used to generate the negative supply required to bias depletion mode FETs used in common source circuit configuration as shown above. This converter uses two external capacitors, C_{NB} the charge transfer capacitor and C_{SUB} the output reservoir capacitor. The circuit provides a regulated -2.5V supply both for gate driver use and for external use if required (for extra discrete bias stages, mixer bias, local oscillator bias etc.). The -2.5V supply is available from the C_{SUB} pin.

If any bias stages are not required, their gate and drain pins may be left open circuit. If all bias stages associated with an R_{CAL} resistor are not required, then this resistor may be omitted.

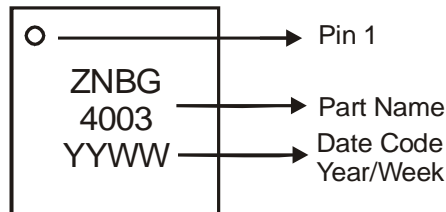
To ease PCB layout, the pinout for the ZNBG4003 includes two V_{CC} pins. These pins are internally connected so only one of the pins needs to be powered for the device to function. It is probable that the extra pin will help avoid the need for trace cross-over components or ground plane disruption from reverse side PCB links. Note that the exposed pad of the package must be either left floating or connected to C_{SUB}.

Ordering Information

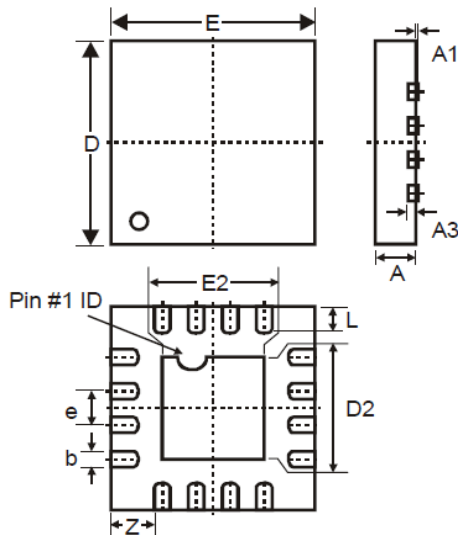
Part Number	Packaging	13" Tape & Reel	
		Quantity	Part Number Suffix
ZNBG4003JA16TC	QFN1633	3000/Tape & Reel	TC



Marking Information



Package Outline Dimensions (All dimensions in mm.)



QFN16 3x3		
Dim	Min	Max
A	0.55	0.65
A1	0.00	0.05
A3	0.15 Typ	
b	0.18	0.28
D	2.95	3.05
D2	1.40	1.60
e	0.50 BSC	
E	2.95	3.05
E2	1.40	1.60
L	0.35	0.45
Z	0.625 Typ	
All Dimensions in mm		

NEW PRODUCT

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