Photoflash Capacitor Charger with IGBT Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 10, 2012

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

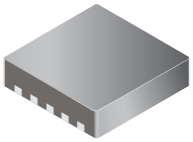
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Photoflash Capacitor Charger with IGBT Driver

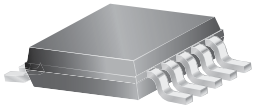
Features and Benefits

- Power with 1 Li+ or 2 Alkaline/NiMH/NiCAD batteries
- Adjustable output voltage
- >75% efficiency
- Three levels of switch current limit: 1.0, 1.2, 1.4 A
- Fast charge time
- Charge complete indication
- Integrated IGBT driver with trigger
- No primary-side Schottky diode needed
- Low-profile packages

Packages:



TDFN/MLP (suffix EJ)
10-pin, 3 mm × 3 mm
0.75 mm nominal overall height



MSOP (suffix LZ)
10-pin, 3 mm × 3 mm
1.10 mm maximum overall height

Approximate Scale 1:1

Description

The A8436 is a highly integrated IC that charges photoflash capacitors for digital and film cameras. It also features an integrated IGBT driver that facilitates the flash discharge function and saves board space.

To charge the photoflash capacitor, the A8436 integrates a 40 V, DMOS switch that drives the transformer in a flyback topology, allowing optimized design with tight coupling and high efficiency. A proprietary control scheme optimizes the capacitor charging time. Low quiescent current and low shutdown current further improve system efficiency and extend battery life.

Three levels of switch current limit are provided: 1.0, 1.2, and 1.4 A. The level is determined by configuring the ILIM pin as grounded, floating, or pulled up to IC supply voltage, respectively.

The CHARGE pin enables the A8436 and starts the charging of the output capacitor. When the designated output voltage is reached, the A8436 stops the charging until the CHARGE pin is toggled again. Pulling the CHARGE pin low stops charging. The $\overline{\text{DONE}}$ pin is an open-drain indicator of when the designated output voltage is reached.

The A8436 can be used with two Alkaline/NiMH/NiCAD or one single-cell Li+ battery connected to the transformer primary. Connect the VIN pin to a 3.0 to 5.5 V supply, which can be either the system rail or the Li+ battery, if used.

The A8436 is available in a very low profile (0.75 mm) 10-terminal 3 mm ×3 mm MLP/TDFN package, making it ideal for space-constrained applications, as well as an MSOP. They are lead (Pb) free, with 100% matte-tin leadframe plating.

Typical Applications

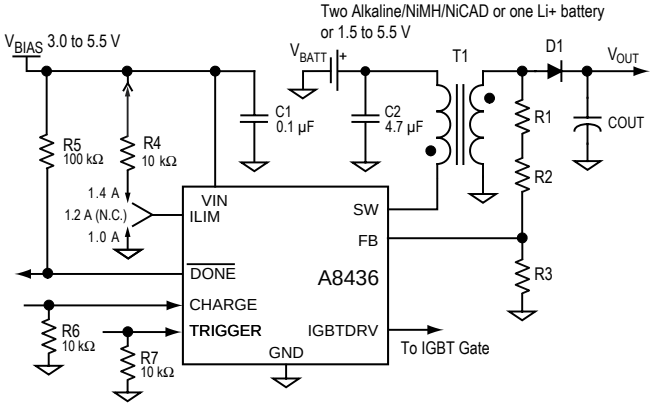


Figure 1. Typical circuit with separate power supply to transformer

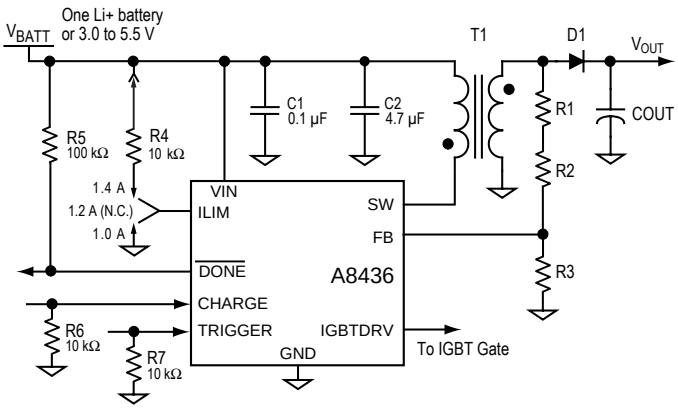


Figure 2. Typical circuit with single power supply

Description (continued)

Applications include:

- Digital camera flash
- Film camera flash
- Cell phone flash
- Emergency strobe light

Selection Guide

Part Number	Package	Packing*
A8436EEJTR-T	10-pin TDFN/MLP	1500 pieces per 7-in. reel
A8436ELZTR-T	10-pin MSOP	4000 pieces per 13-in. reel

*Contact Allegro for additional packing options

Absolute Maximum Ratings

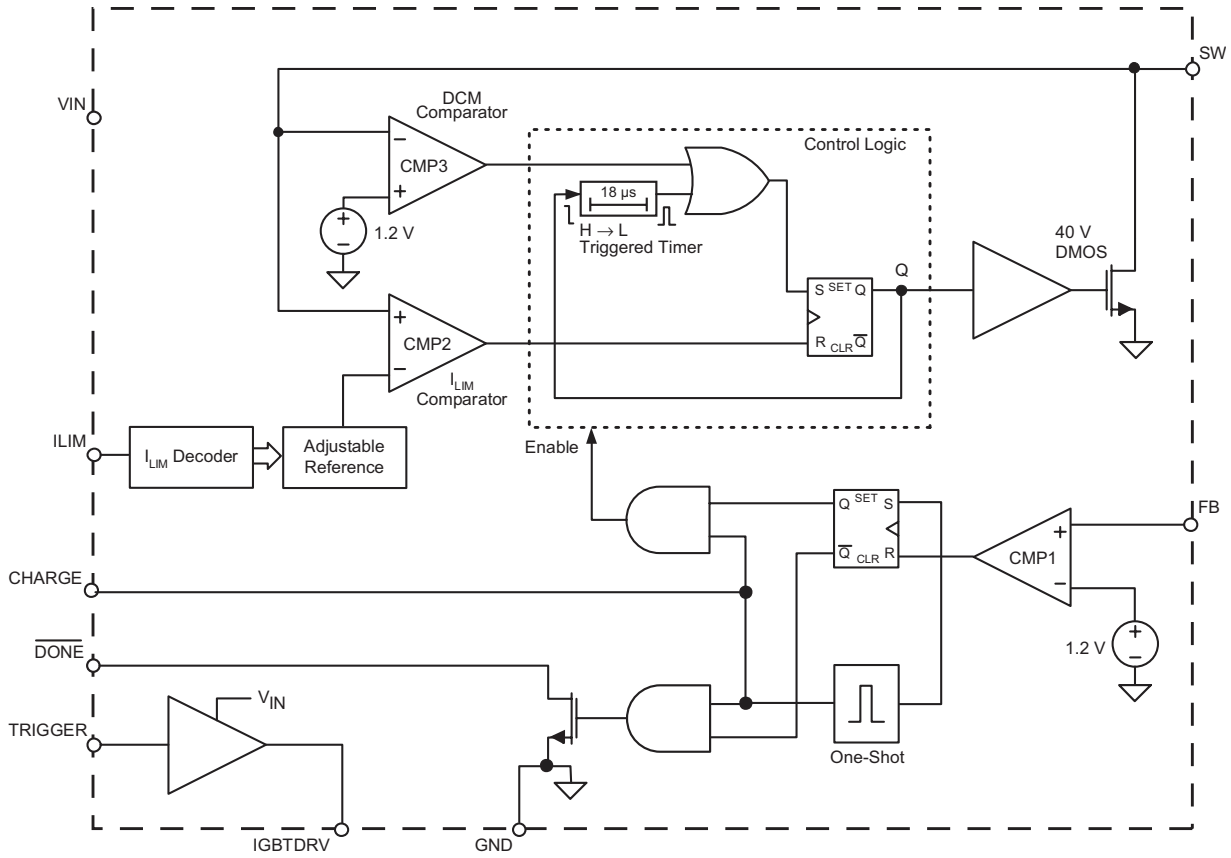
Characteristic	Symbol	Notes	Rating	Units
SW pin	V_{SW}		–0.3 to 40	V
IGBTDRV pin	$V_{IGBTDRV}$		–0.3 to V_{IN} + 0.3	V
FB pin	V_{FB}		–0.3 to V_{IN}	V
All other pins	V_X		–0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Package Thermal Characteristics

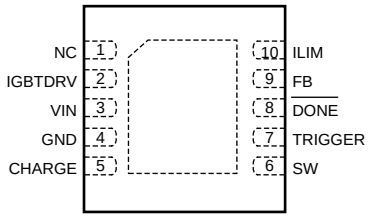
Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	Package EJ, 4 layer PCB, based on JEDEC standard	45	ºC/W
		Package LZ, 4 layer PCB, based on JEDEC standard	103	ºC/W

*Additional information is available on the Allegro website.

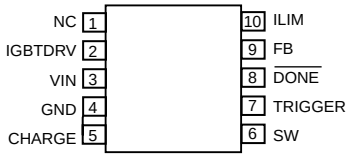
Functional Block Diagram



Device Pin-out Diagrams



Package EJ



Package LZ

(Top Views)

Terminal List Table

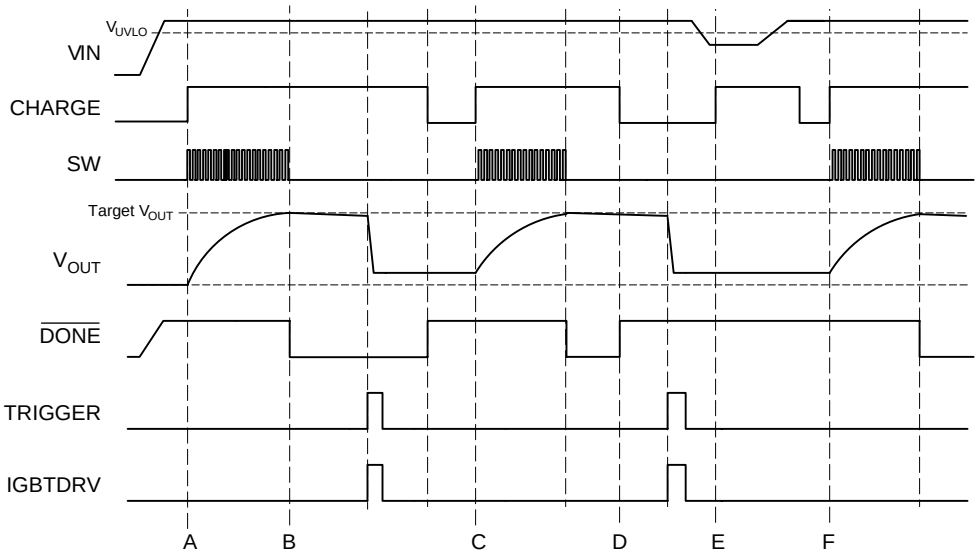
Number	Name	Function
1	NC	No connection
2	IGBTDRV	IGBT driver gate drive output
3	VIN	Power supply input
4	GND	Device ground
5	CHARGE	Charging enable; set to low to power-off the A8436
6	SW	Switch, internally connected to the DMOS power FET drain
7	TRIGGER	Strobe signal input
8	$\overline{\text{DONE}}$	Open drain, when pulled low by internal MOSFET, indicates that charging target level has been reached
9	FB	Output voltage feedback
10	ILIM	Switch current limit setting; sets three discreet levels

ELECTRICAL CHARACTERISTICS Typical values at T_A = 25°C and V_{IN} = 3.3 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage*	V_{IN}		3	–	5.5	V
Supply Current	I_{IN}	Charging	–	1.3	–	mA
		Charging done	–	1	10	µA
		Shutdown (V_{CHARGE} = 0 V, $V_{TRIGGER}$ = 0 V)	–	0.01	1	µA
Primary Side Current Limit	I_{SWLIM}	V_{ILIM} < 1.0 V	–	1.0	–	A
		ILIM pin floating	1.08	1.2	1.32	A
		V_{ILIM} > V_{IN} – 1.3 V	–	1.4	–	A
SW On Resistance	$R_{DS(On)SW}$	V_{IN} = 3.3 V, I_D = 800 mA, T_A = 25°C	–	0.27	–	Ω
SW Leakage Current*	I_{SWLKG}	V_{SW} = 35 V	–	–	1	µA
SW Maximum Off-Time	$t_{OFF(Max)}$		–	18	–	µs
SW Maximum On-Time	$t_{ON(Max)}$		–	18	–	µs
CHARGE Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}	–	–	1	µA
CHARGE Input Voltage*	$V_{CHARGE(H)}$		2	–	–	V
	$V_{CHARGE(L)}$		–	–	0.8	V
$\overline{\text{DONE}}$ Output Leakage Current*	$I_{DONELKG}$		–	–	1	µA
$\overline{\text{DONE}}$ Output Low Voltage*	$V_{DONE(L)}$	32 µA into $\overline{\text{DONE}}$ pin	–	–	100	mV
FB Voltage Threshold*	V_{FB}		1.187	1.205	1.223	V
FB Input Current	I_{FB}	V_{FB} = 1.205 V	–	–120	–	nA
UVLO Enable Threshold	V_{UVLO}	V_{IN} rising	2.55	2.65	2.75	V
UVLO Hysteresis	$V_{UVLOHYS}$		–	150	–	mV
IGBT Driver						
IGBTDRV On Resistance to VIN	$R_{DS(On)I-V}$	V_{IN} = 3.3 V, $V_{IGBTDRV}$ = 1.5 V	–	5	–	Ω
IGBTDRV On Resistance to GND	$R_{DS(On)I-G}$	V_{IN} = 3.3 V, $V_{IGBTDRV}$ = 1.5 V	–	6	–	Ω
TRIGGER Input Current	$I_{TRIGGER}$	$V_{TRIGGER}$ = V_{IN}	–	–	1	µA
TRIGGER Input Voltage*	$V_{TRIGGER(H)}$		2	–	–	V
	$V_{TRIGGER(L)}$		–	–	0.8	V
Propagation Delay, Rising	t_{Dr}	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V	–	30	–	ns
Propagation Delay, Falling	t_{Df}	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V	–	70	–	ns
Output Rise Time	t_r	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V	–	125	–	ns
Output Fall Time	t_f	R_{gate}=12 Ω, C_{LOAD} = 6500 pF, V_{IN} = 3.3 V	–	125	–	ns

*Guaranteed by design and characterization over operating temperature range, –40°C to 85°C.

Operation Timing Diagram



Explanation of Events:

A. Start charging by pulling CHARGE to high, provided that V_{IN} is above the V_{UVLO} level.

B. Charging stops when V_{OUT} reaches the target voltage. $\overline{DONE}$ goes low, to signal the completion of the charging process.

C. Start a new charging process with a low-to-high transition at the CHARGE pin.

D. Pull CHARGE to low, to put the controller in low-power standby mode.

E. Charging does not start, because V_{IN} is below V_{UVLO} level when CHARGE goes high.

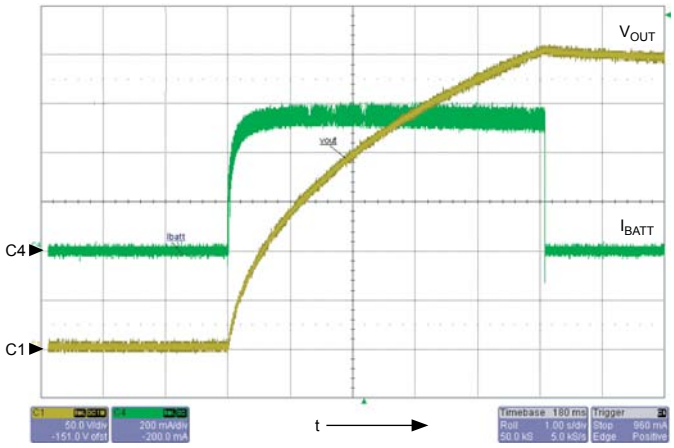
F. After V_{IN} goes above V_{UVLO}, another low-to-high transition at the CHARGE pin is required to start charging.

Performance Characteristics

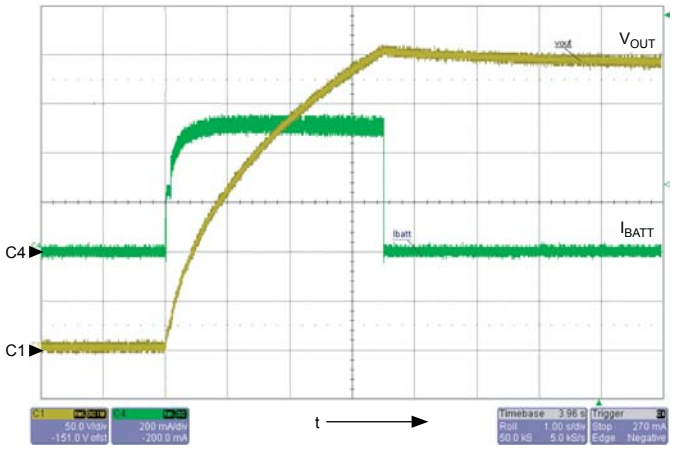
Tests performed using application circuit shown in figure 6 (unless otherwise noted)

Charging Waveforms

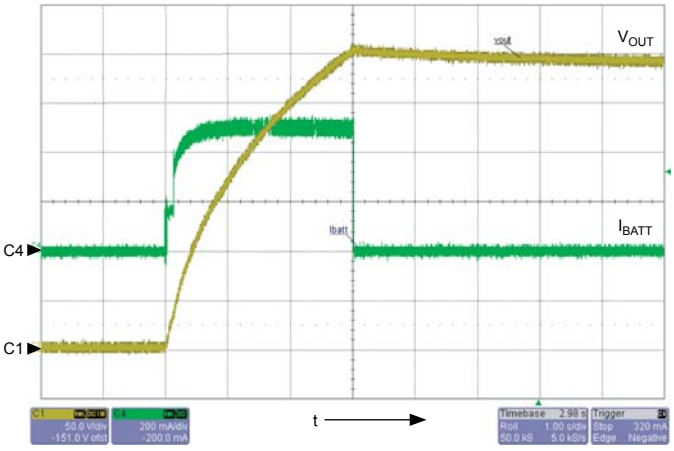
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C4	$I_{BATT(Avg)}$	200 mA
t	time	1 s
Conditions	**Parameter**	**Value**
	V_{BATT}	2.5 V
	V_{BIAS}	3.3 V
	C_{OUT}	100 µF



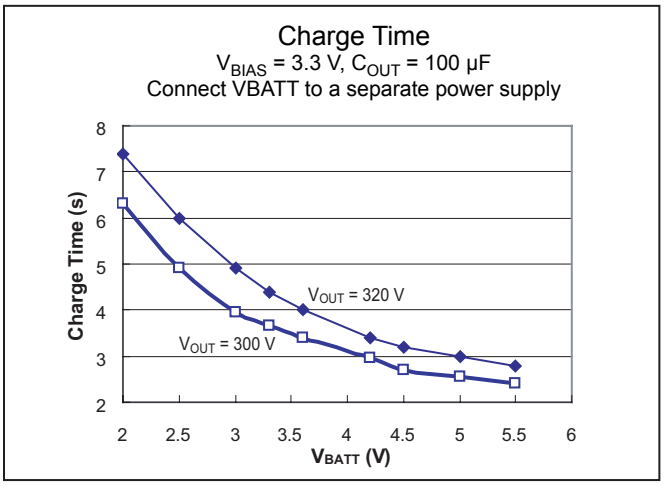
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C4	$I_{BATT(Avg)}$	200 mA
t	time	1 s
Conditions	**Parameter**	**Value**
	V_{BATT}	3.6 V
	V_{BIAS}	3.3 V
	C_{OUT}	100 µF

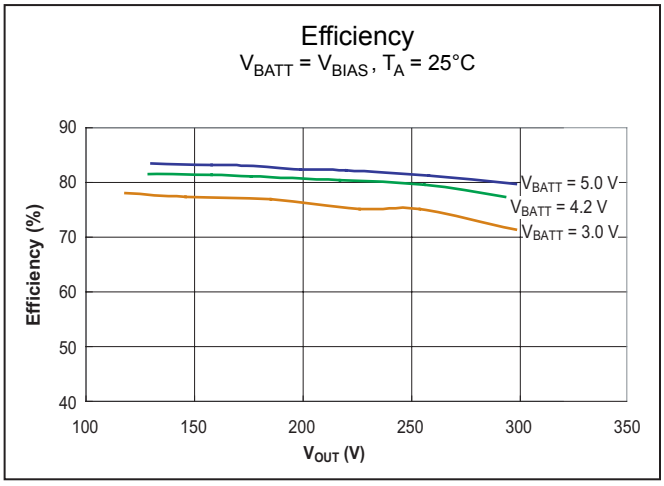


Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C4	$I_{BATT(Avg)}$	200 mA
t	time	1 s
Conditions	**Parameter**	**Value**
	V_{BATT}	4.2 V
	V_{BIAS}	3.3 V
	C_{OUT}	100 µF



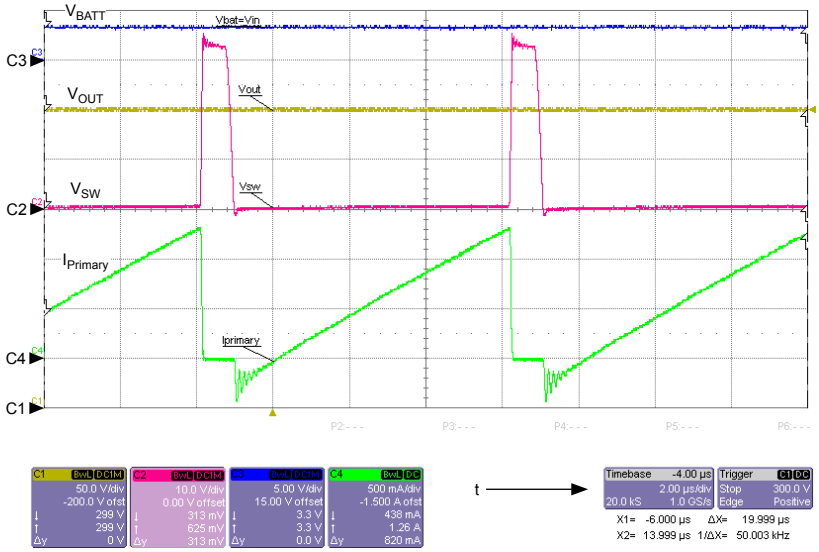
Performance Characteristics, continued
Tests performed using application circuit shown in figure 6 (unless otherwise noted)



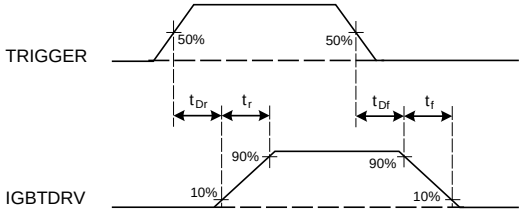


Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	V_{SW}	10 V
C3	V_{BATT}	5 V
C4	$I_{Primary}$	500 mA
t	time	2 µs
Conditions	**Parameter**	**Value**
	V_{OUT}	300 V
	V_{BATT}	V_{IN}

Typical Switching Waveform



IGBT Drive Timing Definition

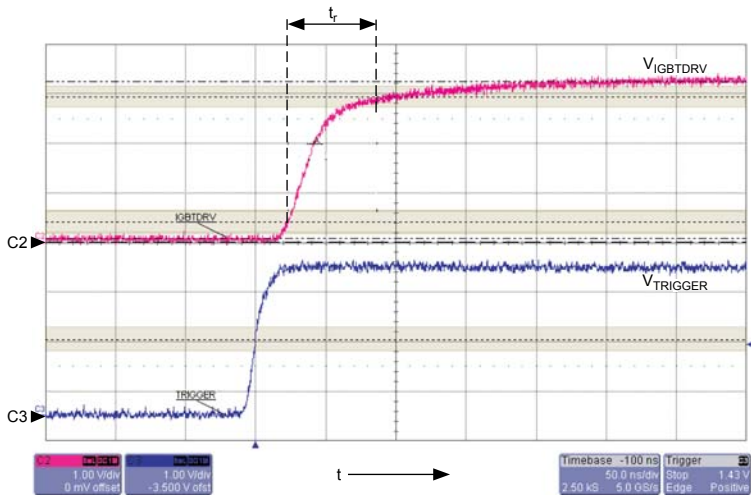


Performance Characteristics, continued
IGBT Drive waveforms are measured with R-C load (12 Ω, 6800 pF)

IGBT Drive Performance

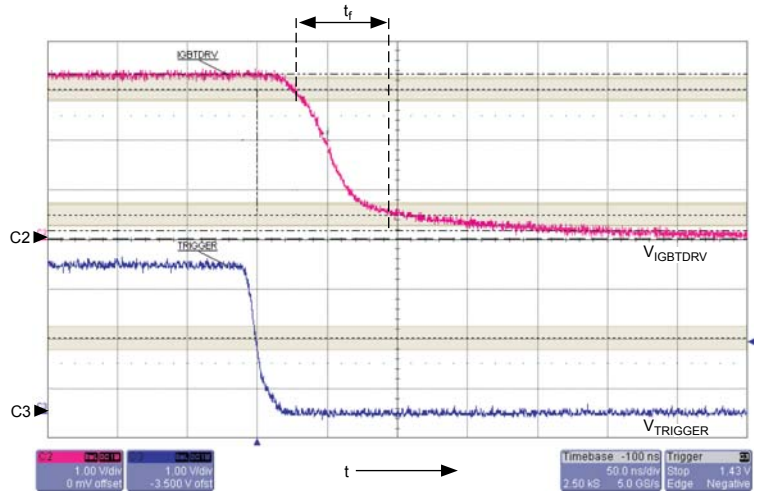
Rising Signal

Symbol	Parameter	Units/Division
C2	$V_{IGBTDRV}$	1 V
C3	$V_{TRIGGER}$	1 V
t	time	50 ns
Conditions	**Parameter**	**Value**
	t_{Dr}	22.881 ns
	t_r	63.125 ns
	C_{LOAD}	6800 pF
	R_{gate}	12 Ω



Falling Signal

Symbol	Parameter	Units/Division
C2	$V_{IGBTDRV}$	1 V
C3	$V_{TRIGGER}$	1 V
t	time	50 ns
Conditions	**Parameter**	**Value**
	t_{Df}	27.427 ns
	t_f	65.529 ns
	C_{LOAD}	6800 pF
	R_{gate}	12 Ω



Functional Description

Overview

The A8436 is a photoflash capacitor charger control IC with adjustable input current limiting. It also integrates an IGBT driver for strobe operation of the flash tube, dramatically saving board space in comparison to discrete solutions for strobe flash operation. The control logic is shown in the functional block diagram.

The charging operation of the A8436 is started by a low-to-high signal on the CHARGE pin, provided that V_{IN} is above V_{UVLO} level. If CHARGE is already high before V_{IN} reaches V_{UVLO}, another low-to-high transition on the CHARGE pin is required to start the charging. When a charging cycle is initiated, the transformer primary side current, $I_{Primary}$, ramps up linearly at a rate determined by the combined effect of the battery voltage, V_{BATT}, and the primary side inductance, $L_{Primary}$. When $I_{Primary}$ reaches the current limit, I_{SWLIM}, set by configuring the ILIM pin, the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor, C_{OUT}, from the secondary winding. The secondary side current drops linearly as C_{OUT} charges.

While the internal MOSFET switch is turned off, the output voltage, V_{OUT}, is sensed by a resistor string, R_1 through R_3, connected between the anode of the output diode, D1, and ground. This resistor string forms a voltage divider that feeds back to the FB pin. The resistors must be sized to achieve a desired output voltage level based on a typical value of 1.205 V at the FB pin. As soon as V_{OUT} reaches the desired value, the charging process is terminated. The user may toggle the CHARGE pin to refresh the photoflash capacitor.

Switch On-Time and Off-Time Control

The A8436 implements an adaptive on-time/off-time control. (For circuit details, please refer to the the Control Logic block in the simplified Functional Block Diagram on page 2.) On-time duration, t_{ON}, is determined by input voltage, V_{IN}, transformer primary inductance, $L_{Primary}$, and the set current limit, I_{SWLIM}. Off-time duration, t_{OFF}, depends on the operating conditions during switch off-time. The A8436 applies its two charging modes, Fast Charging mode and Timer mode, according to those conditions.

Fast Charging and Timer Modes

The IC operates in the Fast Charging mode when the photoflash capacitor, C_{OUT}, is only partially discharged. In Fast Charging mode, the converter operates near the discontinuous boundary, and a sensing circuit tracks the fly-back voltage at the SW node. As soon as this voltage swings below 1.2 V, the internal MOSFET switch is turned on again, starting the next charging cycle.

The IC operates in the Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 10 to 20 V. Timer mode is a fixed 18 µs off-time control. One advantage of the A8436 watchdog timer control scheme is that it limits the initial current surge and thus acts as a "soft-start." As shown in figure 3, the timer mode only lasts a small fraction of a second (usually < 100 ms). It can be recognized by its lower initial input charging current as a result of a lower duty cycle. As output voltage rises to more than 10 to 20 V, the adaptive Fast Charging mode takes over the control, raising the average input current level.

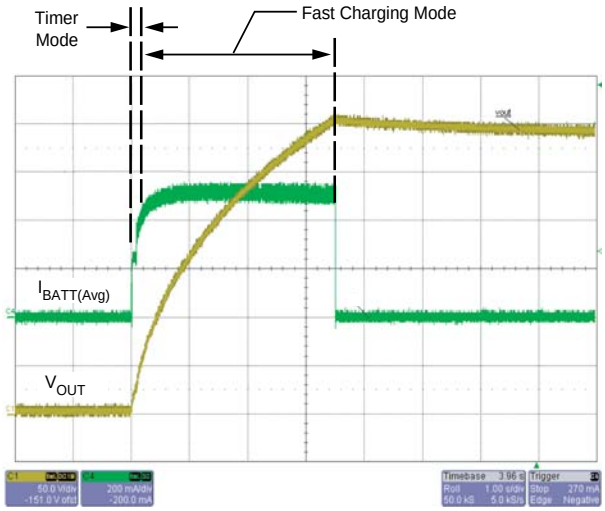


Figure 3. Sequencing of Timer mode and Fast Charging mode (time axis scale is 1 s per division)

Charging Cycles for a Completely Discharged Photoflash Capacitor

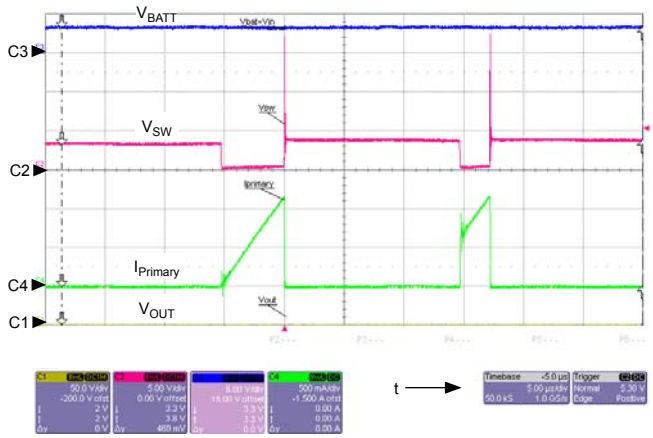


Figure 4A. Initial two cyles of charging a completely discharged photoflash capacitor. In these two cycles, off-time (V_{SW} low) is controlled by the internal 18 µs timer (Timer mode). Note that, in the first cycle, $I_{Primary}$ starts near 0 A, but in the second cycle, it starts at a higher level. This indicates that the transformer core did not reset during the first cycle.

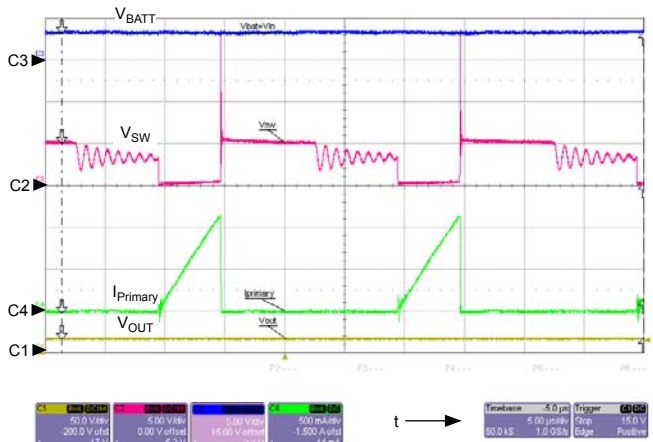


Figure 4B. During the intermediate cycles, the output voltage, V_{OUT}, has increased. $I_{Secondary}$ goes discontinuous, leading to the ringing of V_{SW}. The amplitude of the ringing is not great enough, however, to pull V_{SW} below 1.2 V, so the A8436 remains in Timer mode.

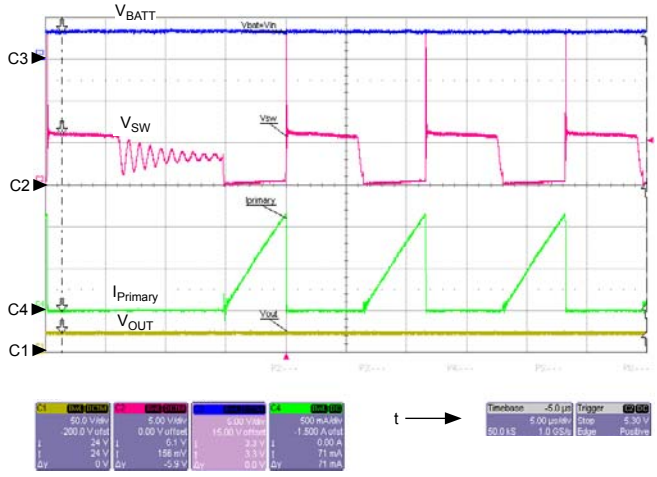


Figure 4C. The final cycle of Timer mode is shown, followed by a series of cycles in Fast Charging mode. V_{SW} is able to ring down below 1.2 V in every cycle as a result of increased V_{OUT}, triggering the turn-on of the main MOSFET switch.

Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	V_{SW}	10 V
C3	V_{BATT}	5 V
C4	$I_{Primary}$	500 mA
t	time	5 µs
Conditions	**Parameter**	**Value**
	V_{BATT}	V_{IN}

To understand the Timer mode, it is noted that the secondary winding charge current, $I_{Secondary}$, decreases linearly at a rate of:

$$\frac{dI_{Secondary}}{dt} = \frac{V_{OUT}}{L_{Primary} \times N^2} \quad (1)$$

where:

$I_{Secondary}$ is the secondary side current,
$L_{Primary}$ is the primary side inductance, and
N is the transformer turns ratio ($N_{Secondary}/N_{Primary}$).

As shown in the three panels of figure 4, when the A8436 charges a fully-discharged photoflash capacitor, $I_{Secondary}$ decreases very slowly due to the low initial V_{OUT}. The A8436 internal timer (Timer mode) sets a maximum timeframe of 18 µs for the off-time as long as the SW node voltage is greater than 1.2 V. When the off-time passes 18 µs, the internal MOSFET switch is turned on, initiating the next charging cycle .

Input Current Limiting

The peak input current, I_{SWLIM}, can be set to three levels by configuring the ILIM pin:

I_{SWLIM} Setting (A)	ILIM Pin Connection
1.0	External ground
1.2	Float
1.4	Pull up to IC supply voltage with a 1 to 10 kΩ resistor

Lower input current offers the advantage of a longer battery lifetime. For faster charging time, however, use the highest current limit.

I_{SWLIM} may be adjusted during charging. Figure 5 shows a waveform of I_{SWLIM} being adjusted during charging. I_{SWLIM} is lowered from 1.4 to 1.2 A, and charging slows slightly at the lower current level.

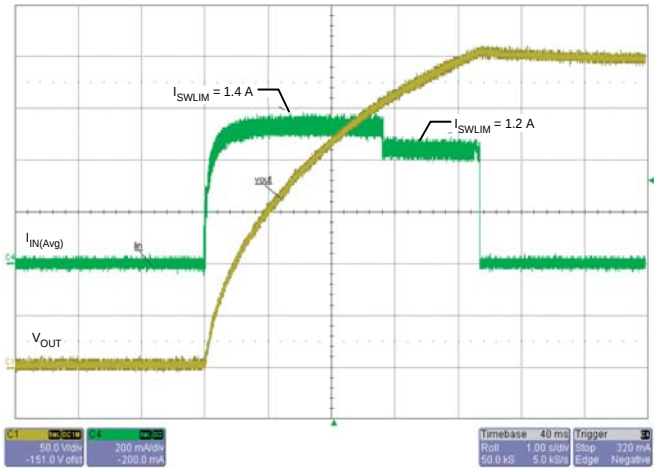


Figure 5. Reducing I_{SWLIM} during charging

Applications Information

Transformer Design

Turns Ratio. The minimum transformer turns ratio, N, (Secondary:Primary) should be chosen based on the following formula:

$$N \geq \frac{V_{OUT} + V_{D\_Drop}}{40 - V_{BATT}} \qquad (2)$$

where:

V_{OUT} (V) is the required output voltage level,
V_{D_Drop} (V) is the forward voltage drop of the output diode(s),
V_{BATT} (V) is the transformer battery supply, and
40 (V) is the rated voltage for the internal MOSFET switch, representing the maximum allowable reflected voltage from the output to the SW pin.

For example, if V_{BATT} is 3.5 V and V_{D_Drop} is 1.7 V (which could be the case when two high voltage diodes were in series), and the desired V_{OUT} is 320 V, then the turns ratio should be at least 8.9.

In a worst case, when V_{BATT} is highest and V_{D_Drop} and V_{OUT} are at their maximum tolerance limit, N will be higher. Taking V_{BATT} = 5.5 V, V_{D_Drop} = 2 V, and V_{OUT} = 320 V × 102 % = 326.4 V as the worst case condition, N can be determined to be 9.5.

In practice, always choose a turns ratio that is higher than the calculated value to give some safety margin. In the worst case example, a minimum turns ratio of N = 10 is recommended.

Primary Inductance. The A8436 has a minimum switch off-time, $t_{OFF(min)}$, of 300 ns, to ensure correct SW node voltage sensing. As a loose guideline when choosing the primary inductance, $L_{Primary}$ (µH), use the following formula:

$$L_{Primary} \geq \frac{300 \times 10^{-9} \times V_{OUT}}{N \times I_{SWLIM}} \quad . \qquad (3)$$

Ideally, the charging time is not affected by transformer primary inductance. In practice, however, it is recommended that a primary inductance be chosen between 10 µH and 20 µH. When $L_{Primary}$ is much lower than 10 µH, the converter operates at higher frequency, which increases switching loss proportionally. This leads to lower efficiency and longer charging time. When $L_{Primary}$ is greater than 20 µH, the rating of the transformer must be dramatically increased to handle the required power density, and the series resistances are usually higher. A design that is optimized to achieve a small footprint solution would have an $L_{Primary}$ of 12 to 14 µH, with minimized leakage inductance and secondary capacitance, and minimized primary and secondary series resistance. Please refer to the table Recommended Components for more information.

Leakage Inductance and Secondary Capacitance. The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the 40 V limit. An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by N^2 when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

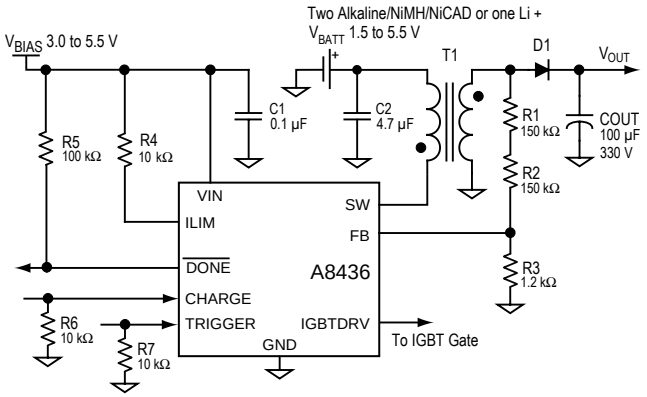


Figure 6. Typical circuit for photoflash application. Configured for I_{SWLIM} of 1.4 A.

Symbol	Rating
C1	0.1 µF, X5R or X7R, 10 V
C2	4.7 µF, X5R or X7R, 10 V
D1	Fairchild Semiconductor BAV23S (dual diode connected in series)
T1	Tokyo Coil Engineering T-16-024A, $L_{Primary}$ = 12 µH, N = 10.2
R1, R2	1206 resistors, 1 %
R3	0603 resistor, 1 %
R4, R5	Pull-up resistors
R6, R7	Pull-down resistors

Adjusting Output Voltage

The A8436 senses output voltage during switch off-time. This allows the voltage divider network, R1 through R3 (see figure 6), to be connected at the anode of the high voltage output diode, D1, eliminating power loss due to the feedback network when charging is complete. The output voltage can be adjusted by selecting proper values of the voltage divider resistors. Use the following equation to calculate values for Rx (Ω):

$$\frac{R_1 + R_2}{R_3} = \frac{V_{OUT}}{V_{FB}} - 1 \, . \qquad (4)$$

R1 and R2 together need to have a breakdown voltage of at least 300 V. A typical 1206 surface mount resistor has a 150 V breakdown voltage rating. It is recommended that R1 and R2 have similar values to ensure an even voltage stress between them. Recommended values are:

R1 = R2 = 150 kΩ (1206)
R3 = 1.2 kΩ (0603)

which together yield a stop voltage of 303 V.

Using higher resistance values for R1, R2, and R3 does not offer significant efficiency improvement, because the power loss of the feedback network occurs mainly during switch off-time, and because the off-time is only a small fraction of each charging cycle.

Output Diode Selection

Choose the rectifying diode(s), D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements.

The peak reverse voltage of the diode, V_{D_Peak}, occurs when the internal MOSFET switch is closed, and the primary-side current starts to ramp-up. It can be calculated as:

$$V_{D\_Peak} = V_{OUT} + N \times V_{BATT} \, . \qquad (5)$$

The peak current of the rectifying diode, ID_Peak, is calculated as :

$$I_{D\_Peak} = I_{Primary\_Peak} / N \, . \qquad (6)$$

Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor, C2. It should be rated at least 4.7 µF/6.3 V to decouple the battery input, V_{BATT}, at the primary of the transformer. When using a separate bias, V_{BIAS}, for the A8436 VIN supply, connect at least a 0.1 µF/6.3 V bypass capacitor to the VIN pin.

Layout Guidelines

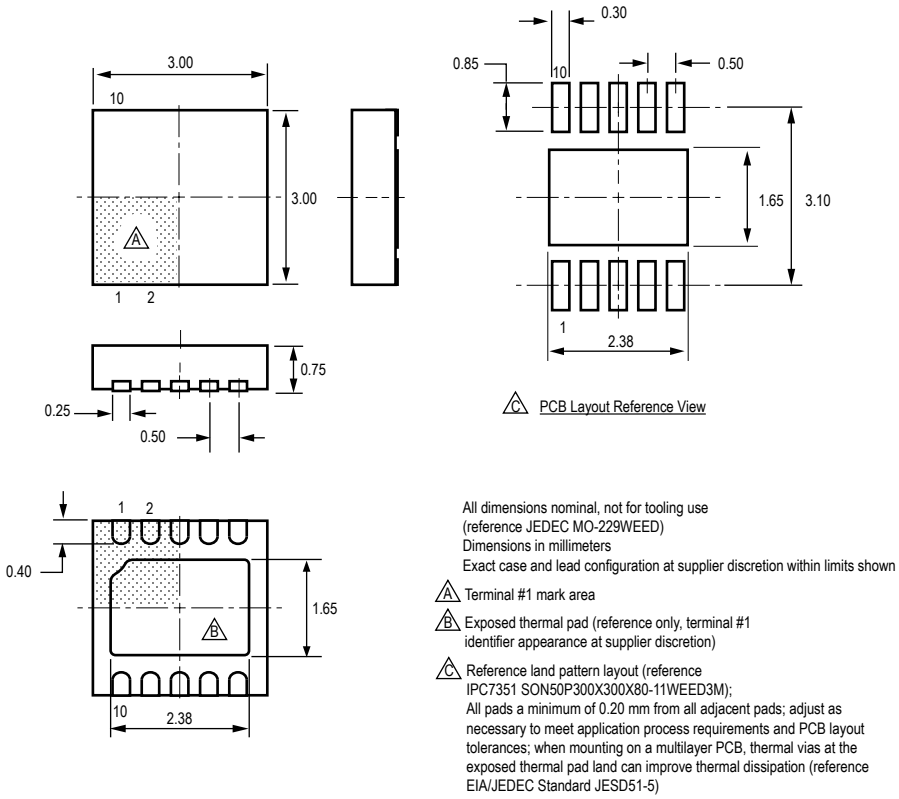
Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin.

Output voltage sensing circuit elements must be kept away from switching nodes such as SW pin. Make sure that there is no GND plane underneath R1 and R2, because parasitic capacitance to ground will affect sensing accuracy. It is important that the $\overline{DONE}$ signal trace be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

Recommended Components Table

Component	Rating	Part Number	Source
C1 Input Capacitor	0.1 µF, ± 10%, 16 V X7R ceramic capacitor (0603)	GRM188R71C104KA01D	Murata
C2 Input Capacitor	4.7 µF, ± 10%, 10 V, X5R ceramic capacitor (0805)	LMK212BJ475KG	Taiyo Yuden
COUT Photoflash Capacitor	330 V, 100 µF (or 19 to 180 µF)	EPH-331ELL101B131S	Chemi-Con
D1 Output Diode	2 x 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor
	2 x 300 V, 225 mA, 5 pF	GSD2004S	Vishay
R1 and R2 FB Resistors	150 kΩ, $^1/_4$ W ± 1% (1206)	9C12063A1503FKHFT	Yageo
R3 FB Resistors	1.20 kΩ $^1/_{10}$ W ± 1% (0603)	9T06031A1201FBHFT	Yageo
T1 Transformer	1:10.2, $L_{Primary}$ = 14.5 µH	LDT565630T-002	TDK
	1:10.2, $L_{Primary}$ = 12 µH	T-16-024A	Tokyo Coil Engineering
	1:10, $L_{Primary}$ = 10.8 µH	ST-532517A	Asatech
	1:10.2, $L_{Primary}$ = 9.8 µH	SBL-5.6-1	Kijima-Musen

Package EJ, 10-Contact TDFN/MLP



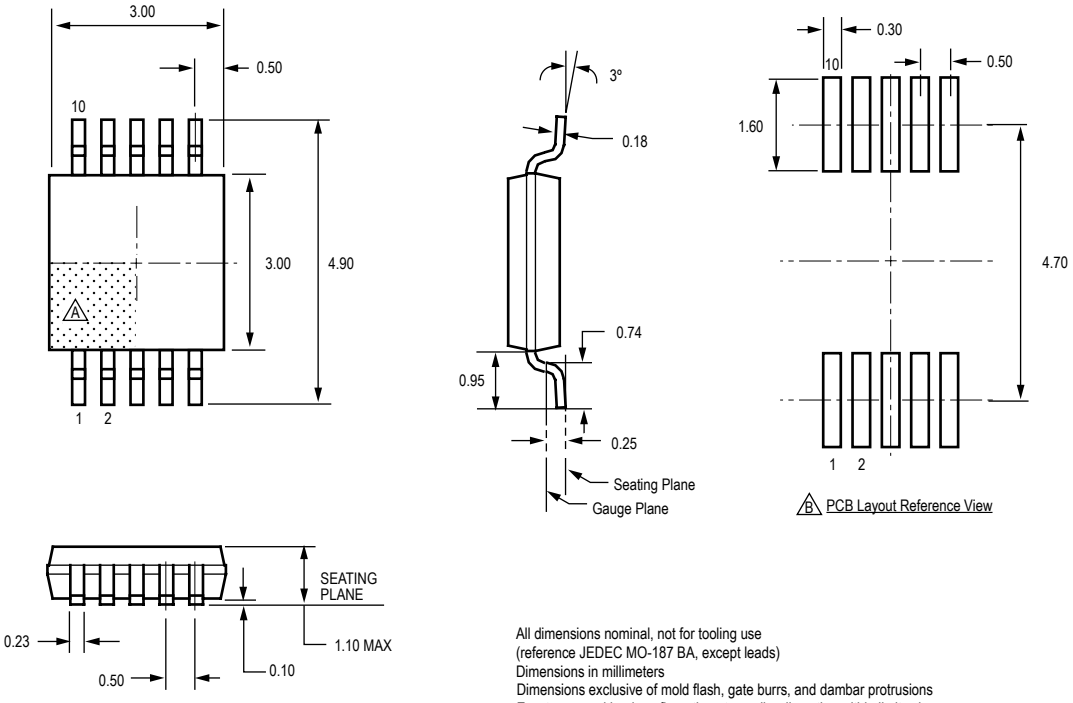
All dimensions nominal, not for tooling use
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Package LZ, 10-Contact MSOP



All dimensions nominal, not for tooling use
(reference JEDEC MO-187 BA, except leads)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference land pattern layout
(reference IPC7351 TSSOP50P490X110-10M);
All pads a minimum of 0.20 mm from all adjacent pads;
adjust as necessary to meet application process
requirements and PCB layout tolerances

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