SSL5251T

Mains dimmable buck-boost LED driver IC

Rev. 2.1 — 26 January 2016 Product data sheet

1. General description

The SSL5251T is a highly integrated, high-precision dimmable controller with an external MOSFET. It is intended to drive LED lamps in dimmable lighting applications up to 25 W. The SSL5251T is designed for high power factor, phase-dimmable applications.

The SSL5251T operates in Boundary Conduction Mode (BCM) with on-time control. It provides a constant output current control with good LED output current accuracy. Adaptive switching frequency gives freedom to choose the inductor, which enables the optimization of inductor size, efficiency and EMI.

The SSL5251T can start up and operate in switching mode directly from an external resistor without capacitor charge pump supply or auxiliary supply. This feature simplifies the V_{CC} supply. So, a low-cost off-the-shelf inductor can be used, which provides flexibility in application design.

2. Features and benefits

- Supports most available dimming solutions
- Deep dimming level
- Flicker-free dimming
- Low component count ensuring a compact solution and small, single layer Printed-Circuit Board (PCB) footprint
- Excellent line regulation and load regulation and good LED output current accuracy
- Efficient BCM operation with:
  - Minimal reverse recovery losses in freewheel diode
  - Zero Current Switching (ZCS) and Valley switching for turn-on of switch
  - Minimal inductance value and size required
  - High efficiency (up to 88 %)
  - Ultra low IC current during operation (< 200 μA)
- Auto-recovery protections:
  - UnderVoltage LockOut (UVLO)
  - Cycle-by-cycle OverCurrent Protection (OCP)
  - Internal OverTemperature Protection (OTP)
  - Output OverVoltage Protection (OVP)
  - Output Short Protection (OSP)
- Extended IC lifetime

3. Applications

- The SSL5251T is intended for low-cost, non-isolated dimmable lighting applications that work from single mains voltage.

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	operating range [1]	9.9	-	16	V
R_{DSon}	on-state resistance	source-switch				
		T_j = 25 °C	-	0.87	-	Ω
		T_j = 125 °C	-	1.2	-	Ω
$I_{I(SW)}$	input current on pin SW	duty cycle < 20 %	–2	-	+2	A
$V_{I(SW)}$	input voltage on pin SW	current limited at 8.8 mA; internal switch-off	–0.4	-	+22	V
$V_{I(ISNS)}$	input voltage on pin ISNS	operating range in application	0	-	1.2	V
$V_{IO(COMP)}$	input/output voltage on pin COMP	operating range in application	2	-	4	V
$V_{I(DIM)}$	input voltage on pin DIM	operating range in application	0	-	2	V

[1] An internal clamp sets the supply voltage. The current into the VCC pin must not exceed the maximum I_{VCC} value (see Table 4).

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SSL5251T	SO8	plastic surface-mounted package; 8 leads	SOT96-1

6. Block diagram

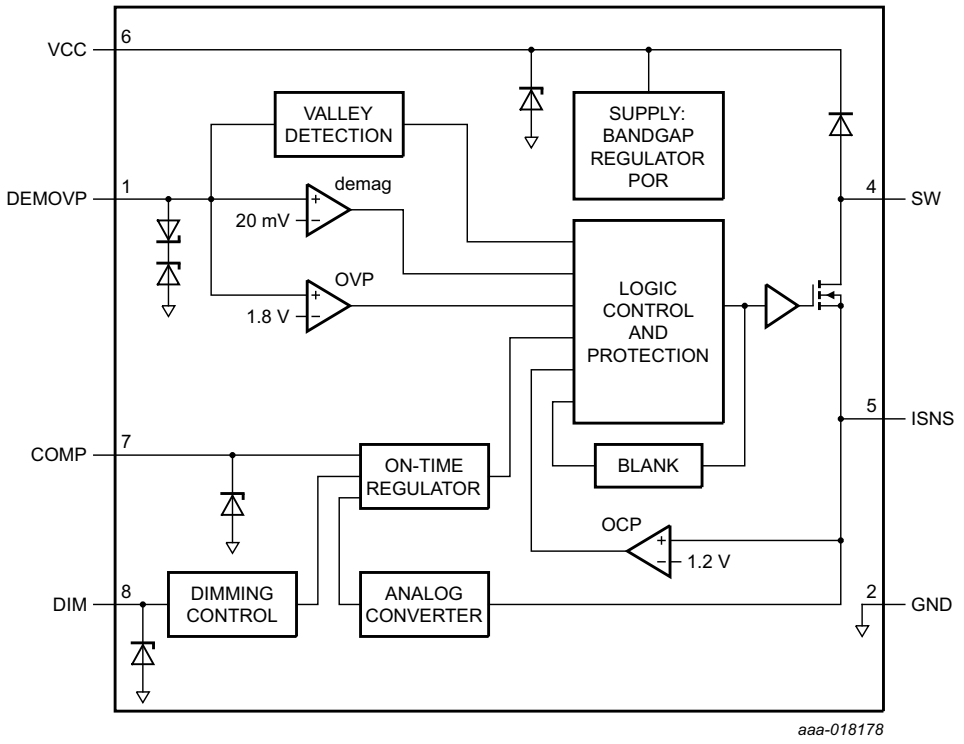


Fig 1. SSL5251T block diagram

7. Pinning information

7.1 Pinning

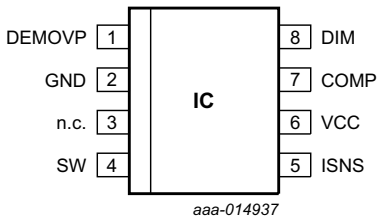


Fig 2. SSL5251T pin configuration (SO8 package)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
DEMOVP	1	input from LED output for demagnetization timing, valley detection, and OVP
GND	2	ground
n.c.	3	not connected
SW	4	internal source-switch drain
ISNS	5	current sense input
VCC	6	supply voltage
COMP	7	loop compensation to provide stable response
DIM	8	dimming control input

8. Functional description

8.1 Converter operation

The converter in the SSL5251T is a source-switch, BCM, on-time controlled buck-boost system. Figure 3 shows the basic application diagram. To save IC supply current, an integrated source-switch topology is used. It enables that even in switching mode only an external resistor is used as supply.

The converter operates at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Figure 5 shows the waveforms.

When the internal source-switch is switched on at t0, the inductor current I_L proportionally to V_{in} builds up from zero during the source-switch on-time (t0 to t1). Energy is stored in the inductor. When the internal source-switch switches off at t1, I_L flows through the freewheeling diode and the output capacitor. The inductor current drops proportionally to the V_{out} value (t2 to t3). When I_L reaches zero at t3, a new switching cycle is started after a short delay (t3 to t00) from valley detection.

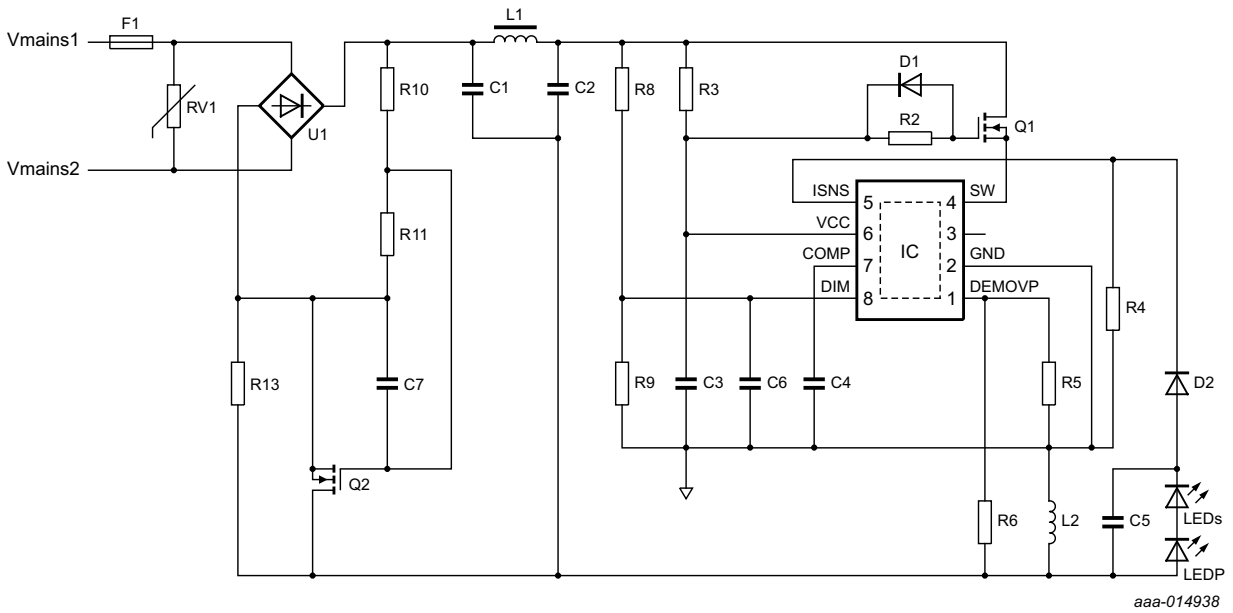


Fig 3. SSL5251T basic application diagram

8.2 On-time control

When measuring the inductor current I_L using sense resistor R4, the on-time is regulated so that the average ISNS voltage ($V_{intregd(AV)ISNS}$) is regulated to $V_{intregd(max)ISNS}$ (155 mV typical) during the off-time of the main switch. The average output current I_{out} can be calculated with Equation 1:

$$I_{out} = \frac{V_{intregd(AV)ISNS}}{R4} \quad (1)$$

8.3 Dimming control

When measuring the phase-cut mains voltage using the DIM pin, the DIM voltage modulates the internal reference voltage. The dimmed output current $I_{O(dim)}$ can be calculated with Equation 2:

$$I_{O(dim)} = \frac{V_{dim(itg)AV(ISNS)}}{R4} \quad (2)$$

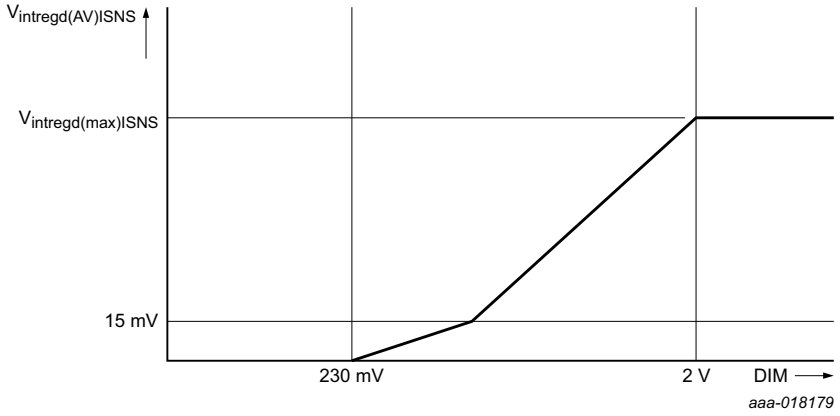


Fig 4. Dimming control transfer function

8.4 Valley detection

When I_L has decreased to zero at t3, the LEDP voltage starts to oscillate around the 0 V level, with amplitude V_{OUT} and frequency (f_{ring}). A special circuit called valley detection is integrated in the SSL5251T. It senses when the LEDP voltage reaches its lowest level (valley) at the DEMOVP pin. The internal source-switch is switched on again when the valley is detected. As a result, the switch-on switching losses are reduced.

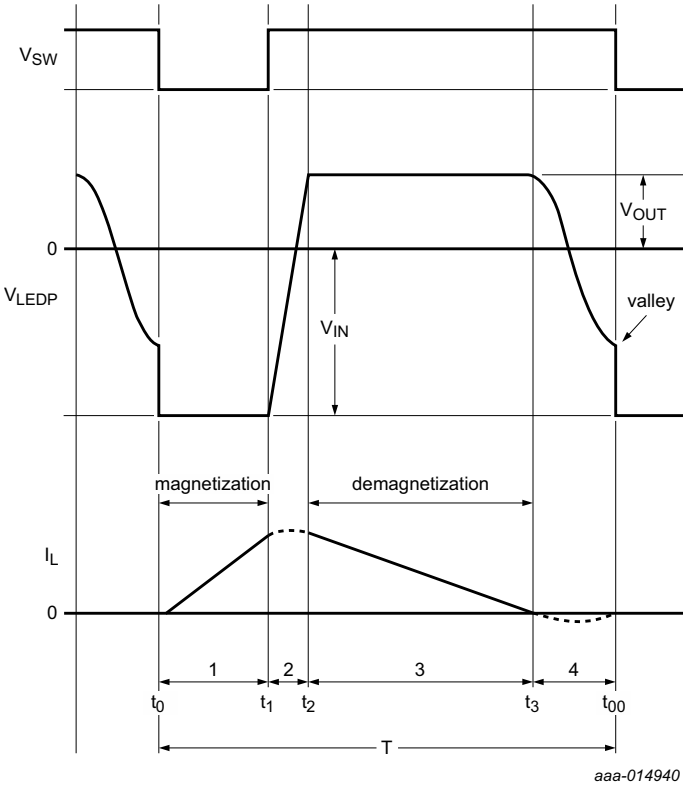


Fig 5. Buck-boost waveforms and valley detection

8.5 Start-up current

The supply current for the IC is supplied by resistor R_{VCC}. Just before V_{CC} reaches the start-up voltage level ($V_{startup}$), the IC draws an additional start-up current ($I_{CC(startup)}$). So the supply current in operation is lower than the supply current during start-up conditions. It prevents lamp flicker when the mains voltage increases or decreases slowly.

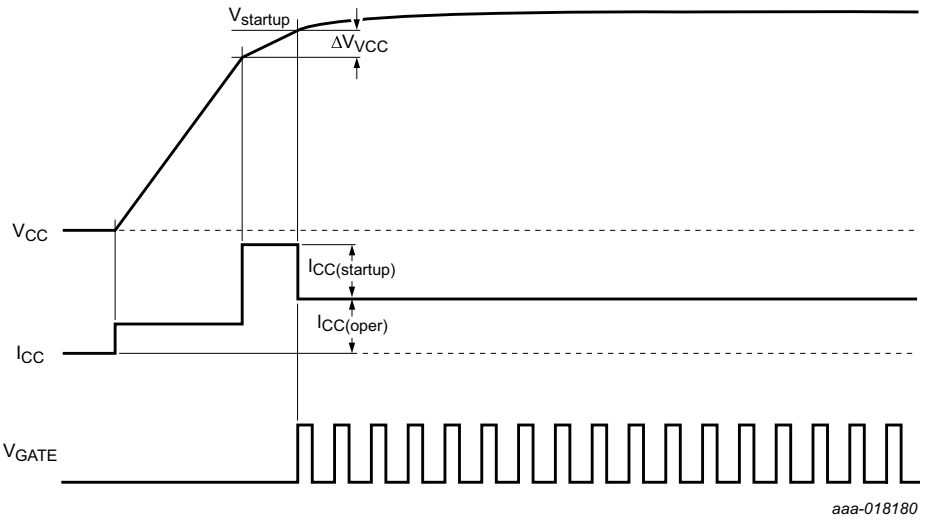


Fig 6. Start-up current waveform

8.6 Leading-Edge Blanking (LEB)

To prevent false detection of overcurrent, a blanking time following switch-on is implemented. When the internal source-switch turns on, a short current spike can occur because of the capacitive discharge of voltage over the drain and the source. It is disregarded during the LEB time (t_{leb}).

8.7 Magnetization switching

When the mains voltage is very low, during dimming or around the zero crossings of the mains, the system hardly delivers any energy to the LED. To improve the efficiency, maximum off-time ($t_{off(max)}$) switching limits the switching frequency to < 25 kHz. A peak voltage on the ISNS pin below the $V_{I(min)ISNS}$ voltage indicates a low mains voltage.

8.8 Protections

The IC incorporates the following protections:

- UnderVoltage LockOut (UVLO)
- Cycle-by-cycle OverCurrent Protection (OCP)
- Internal OverTemperature Protection (OTP)
- Cycle-by-cycle maximum on-time protection
- Output OverVoltage Protection (OVP)
- Output Short Protection (OSP)

8.8.1 UnderVoltage LockOut (UVLO)

When the voltage on the VCC pin drops to below $V_{th(UVLO)}$, the IC stops switching. An attempt is made to restart IC when the $V_{CC} > V_{startup}$.

8.8.2 Cycle-by-cycle OverCurrent Protection (OCP)

The SSL5251T contains a built-in peak current detector. It triggers when the voltage at the ISNS pin reaches the peak level $V_{I(max)ISNS}$. A resistor connected to the ISNS pin senses the current through the inductor I_L. The maximum current in inductor $I_{L(max)}$ can be calculated with Equation 3:

$$I_{L(max)} = \frac{V_{I(max)ISNS}}{R4 + R_{bond} \times \delta_{swon}} \quad (3)$$

Where:

- R_{bond} is the ISNS bond wire resistance
- δ_{swon} is the switch-on duty cycle

The sense circuit is activated after the LEB time (t_{leb}). It automatically provides protection for maximum LED current during operation. A propagation delay exists between overcurrent detection and the actual source-switch switch-off. Due to this delay, the actual peak current is slightly higher than the OCP level set by the resistor in series with the ISNS pin.

8.8.3 OverTemperature Protection (OTP)

When the internal OTP function is triggered at IC junction temperature $T_{pl(IC)}$, the converter stops switching. The IC resumes switching when the IC temperature drops to below $T_{pl(IC)rst}$.

8.8.4 Cycle-by-cycle maximum on-time protection

Measuring the inductor current I_L using sense resistor R_{sense} regulates the on-time. The on-time is limited to a fixed value ($t_{on(max)}$). It protects the system and the IC when the ISNS pin is shorted or the system works at very low mains.

8.8.5 Output OverVoltage Protection (OVP)

Measuring the voltage at the DEMOVP pin during the secondary stroke gives an accurate output OVP. The resistive divider connected between the LEDP node and the DEMOVP pin sets the maximum LED voltage.

An internal counter prevents false OVP detection because of noise on the DEMOVP pin. After three continuous cycles with a DEMOVP pin voltage exceeding the OVP level, OVP is triggered.

OVP triggers a restart sequence: A discharge current ($I_{CC(dch)}$) is enabled and discharges V_{CC} to below $V_{rst(latch)}$. When $V_{rst(latch)}$ is reached, the system restarts.

8.8.6 Output Short Protection (OSP)

The converter operates in Discontinuous Conduction Mode (DCM). A new cycle is only started after the previous cycle has ended. Measuring the voltage on the DEMOVP pin detects the end of the cycle. When the DEMOVP pin voltage drops to below the demagnetization level ($V_{det(demag)}$) and a valley is detected, a new cycle starts. The converter regulates the adjusted output current and the on-time is reduced to a safe value by this feedback. The reduced on-time in combination with a very long demagnetization period prevents the converter from any damage or excessive dissipation.

To prevent false demagnetization detection, a blanking time ($t_{sup(xfmr\_ring)}$) is implemented at the start of the secondary stroke.

8.9 Supply management

The IC starts up when the voltage at the VCC pin exceeds $V_{startup}$. The IC locks out (stops switching) when the voltage at the VCC pin drops to below $V_{th(UVLO)}$. The hysteresis between the start and stop levels allows the VCC capacitor to supply the IC during zero-crossings of the mains.

The SSL5251T incorporates an internal VCC clamping circuit. The clamp limits the voltage on the VCC supply pin to the maximum value $V_{clamp(VCC)}$. If the maximum current of the external resistor minus the current consumption of the IC is lower than the limiting value of I_{VCC} in Table 4, no external Zener diode is required.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage	current limited [1][2]	–0.4	+18	V
$V_{I(SW)}$	input voltage on pin SW	current limited [1][2]	–0.4	+22	V
$V_{I(ISNS)}$	input voltage on pin ISNS		–0.4	+5	V
$V_{IO(COMP)}$	input/output voltage on pin COMP		–0.4	+5.3	V
$V_{I(DEMOVP)}$	input voltage on pin DEMOVP		–6	+6	V
$V_{I(DIM)}$	input voltage on pin DIM		–0.4	+5	V
Currents					
$I_{I(VCC)}$	input current on pin VCC		-	+8.8	mA
$I_{I(SW)}$	input current on pin SW	RMS current	-	380	mA
		duty cycle < 20 %	–2	+2	A
$I_{I(ISNS)}$	input current on pin ISNS	duty cycle < 20 %	–2	+2	A
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.28	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–40	+160	°C
ESD					
V_{ESD}	electrostatic discharge voltage	class 1			
		human body model [3]	–2000	+2000	V
		charged device model [4]	–500	+500	V

[1] The current into the VCC pin must not exceed the maximum I_{VCC} value.

[2] An internal clamp sets the supply voltage and current limits.

[3] Equivalent to discharge a 100 pF capacitor through a 1.5 kΩ series resistor.

[4] Charged device model: equivalent to charging the IC up to 1 kV and the subsequent discharging of each pin down to 0 V over a 1 Ω resistor.

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; PCB; 2 cm × 3 cm; 2-layer; 35 μm copper/layer	159	K/W
		in free air; SO8 package; PCB; JEDEC 2s2p	89	K/W
Ψ_{j-top}	thermal resistance from junction to top	top package temperature measured at the warmest point on top of the case	4	K/W

11. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground pin (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply (pin VCC)						
$V_{startup}$	start-up voltage		14.55	15	15.45	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		9.7	10	10.3	V
ΔV_{VCC}	voltage difference on pin VCC		0.18	0.31	0.44	V
$V_{clamp(VCC)}$	clamp voltage on pin VCC	$I_{I(VCC)}$ = 2.6 mA [1]	15.4	16	16.6	V
$V_{rst(latch)}$	latched reset voltage		5.8	6.2	6.6	V
$I_{CC(oper)}$	operating supply current	switching at 100 kHz	160	180	200	μA
$I_{CC(startup)}$	start-up supply current		110	135	160	μA
$I_{CC(dch)}$	discharge supply current	$V_{CC} = V_{rst(latch)}$	3.7	-	-	mA
Loop compensation (pin COMP)						
$V_{IO(COMP)}$	input/output voltage on pin COMP	operating range in application	2	-	4	V
$V_{ton(zero)}$	zero on-time voltage		1.9	2.0	2.1	V
$V_{ton(max)}$	maximum on-time voltage		3.8	4.0	4.2	V
$V_{clamp(COMP)}$	clamp voltage on pin COMP	$I_{I(COMP)}$ = 1 mA	4.4	4.8	5.2	V
$t_{on(max)}$	maximum on-time	$V_{IO(COMP)}$ = 4 V	11.5	14.5	17.5	μs
$I_{O(COMP)}$	output current on pin COMP	$V_{I(ISNS)}$ = 0 V; $V_{I(DIM)}$ > 2 V	–3.6	–3.0	–2.4	μA
$I_{dch(COMP)}$	Discharge current on pin COMP	$V_{I(DIM)}$ = 0 V	280	480	680	nA
Valley detection and overvoltage detection (pin DEMOVP)						
$I_{prot(DEMOVP)}$	protection current on pin DEMOVP	open pin current; $V_{I(DEMOVP)}$ = 0 V	–250	–180	–50	nA
$V_{th(ovp)}$	overvoltage protection threshold voltage		1.75	1.82	1.89	V

Table 6. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground pin (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{cy(ovp)}$	number of overvoltage protection cycles		-	3	-	-
$(dV/dt)_{vrec}$	valley recognition voltage change with time	[2]	-	−3.8	-	V/µs
$V_{det(demag)}$	demagnetization detection voltage		6	20	34	mV
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time		1.13	1.45	1.77	µs
Current sensing (pin ISNS)						
$V_{I(ISNS)}$	input voltage on pin ISNS	operating range in application	0	-	1.2	V
$V_{I(min)ISNS}$	minimum input voltage on pin ISNS		15	25	35	mV
$V_{I(max)ISNS}$	maximum input voltage on pin ISNS		1.1	1.2	1.3	V
$t_{on(min)}$	minimum on-time	[3]	280	380	480	ns
t_d	delay time	[3]	-	100	-	ns
$g_{m(ISNS)}$	ISNS transconductance	$V_{I(ISNS)}$ to $I_{O(COMP)}$	18	19.3	20.6	µA/V
$V_{intregd(max)ISNS}$	maximum regulated voltage on pin ISNS	$V_{I(DIM)}$ > 2 V	0.15	0.155	0.16	V
Dimming control (pin DIM)						
$V_{I(DIM)}$	input voltage on pin DIM	operating range in application	0	-	2	V
$V_{intregd(AV)}/V_{dim}$	average internal regulated voltage ratio to dimming voltage	0.65 V < V_{DIM} < 2 V	95	100	105	mV/V
		0.25 V < V_{DIM} < 0.6 V	25	35	45	mV/V
$V_{clamp(DIM)}$	clamp voltage on pin DIM	$I_{I(DIM)}$ = 200 µA	4.3	4.5	4.7	V
Driver (pin SW)						
R_{DSon}	on-state resistance	T_j = 25 °C	-	0.87	0.94	Ω
		T_j = 125 °C	-	1.2	-	Ω
$t_{off(max)}$	maximum off-time		30	40	50	µs
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		140	150	165	°C
$T_{pl(IC)rst}$	reset IC protection level temperature		106	118	130	°C

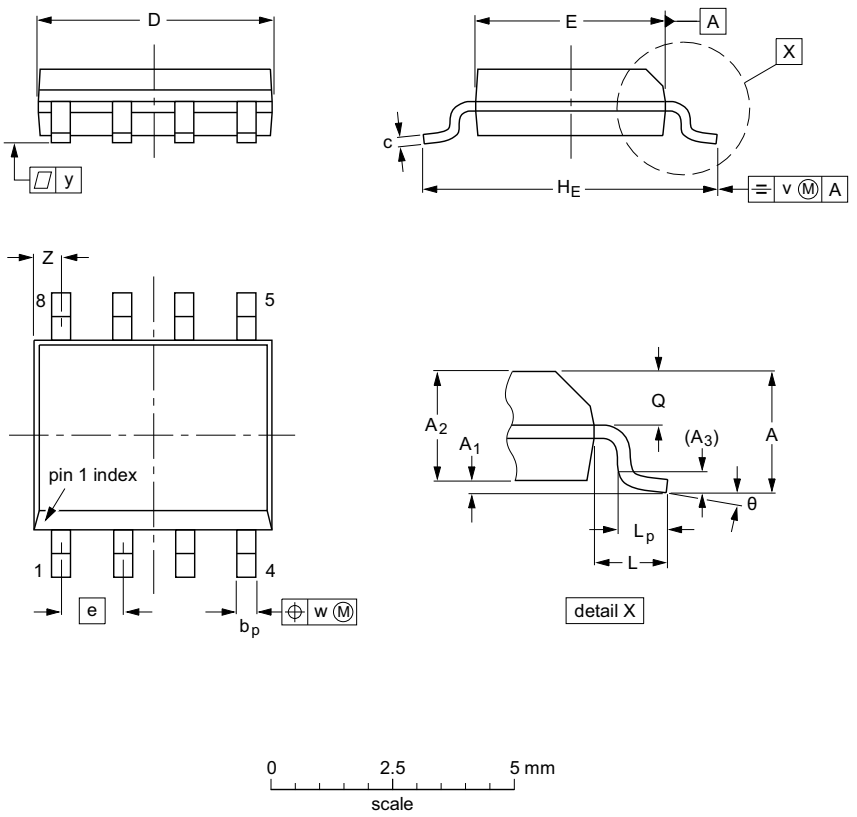
[1] The start-up voltage and the clamp voltage are correlated.

[2] Guaranteed by design.

[3] $t_{leb} = t_{on(min)} - t_d$; $t_{on(min)}$ is only effective when OCP is triggered.

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT96-1 (SO8)

13. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSL5251T v.2.1	20160126	Product data sheet	-	SSL5251T v.2
Modifications:	• Section 8.8.6 “Output Short Protection (OSP)” has been updated.			
SSL5251T v.2	20150911	Product data sheet	-	SSL5251T v.1
SSL5251T v.1	20150720	Preliminary data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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15. Contact information

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16. Contents

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